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## **Instruction Set Architecture (ISA)**

### **Overview:**

This code is a simple Instruction Set Architecture (ISA) simulation with registers and an instruction set. The processor executes instructions, and the code includes functionalities to print both decoded and encoded forms of the instructions, display the result of the registers, calculate clock cycles and simulate a pipelined execution.

The number of registers that are used in this simulation includes r0, r1, r2, r3, r4, r5, r6 and r7 is used exclusively for storing remainder.

The operations include “mov” which load number or register to a particular register, “add” is to plus a number to the register or plus register with another register, “mul” is to multiply a number to the register or multiply register with another register, “sub” is to subtract a number to the register or subtract register with another register, lastly “div” is to divide a number to the register or divide register with another register.

### **Class Structure:**

1. Registers Class:
  - Attributes:
    - reg\_val: Represents the value stored in the register.
    - reg\_adr: Represents the address of the register.
  - Methods:
    - set\_reg\_adr: Sets the register address.
    - get\_reg\_adr: Retrieves the register address.
    - set\_reg\_val: Sets the register value.
    - get\_reg\_val: Retrieves the register value.
    - to\_32bit\_val: Converts the register value to a 32-bit binary string.
    - to\_3bit\_adr: Converts the register address to a 3-bit binary string.
2. InstructionSet class:
  - Attributes:
    - step: Represents the step in the execution.
    - opcode: Represents the operation code of the instruction.
    - register: Represents the register involved in the instruction.
    - clkcy: Represents the number of clock cycles the instruction takes.
    - operand: Represents an operand for some instructions.
    - value: Represents a value associated with the instruction.
  - Methods:
    - five\_bit\_opcode: Converts the opcode to a 5-bit binary string.
    - encode\_instruction: Encodes the instruction in a specific format.
    - to\_32bit\_val: Converts the value to a 32-bit binary string.
    - \_\_str\_\_: Provides a string representation of the instruction.

**Main Functionality:**

1. main Function:
  - Initializes a list of registers ("regs") and an empty list of instructions ("instructions")
  - Accepts input from user until "end 0 0" is entered.
  - Processes instructions, updates register values, and creates "InstructionSet" objects.
  - Calls "print\_output" to display the results.
2. print\_output Functions:
  - Prints decoded and encoded forms of each instruction along with clock cycles.
  - Displays the state of registers after execution.
  - Calculates and prints Clocks Per Instruction (CPI).
  - Simulates a pipelined execution and prints the result.

**User input:**

The user enters (opcode) (operand1) (operand2).

- Opcodes are the operations code.
- Operand1 are registers (r0 to r6).
- Operand2 can be registers or numbers.

**Here is the code:**

```
1 class Registers:
2     def __init__(self, reg_val, reg_adr):
3         self.reg_val = reg_val
4         self.reg_adr = reg_adr
5
6     def set_reg_adr(self, reg_adr):
7         self.reg_adr = reg_adr
8
9     def get_reg_adr(self):
10        return self.reg_adr
11
12    def set_reg_val(self, reg_val):
13        self.reg_val = reg_val
14
15    def get_reg_val(self):
16        return self.reg_val
17
18    def to_32bit_val(self):
19        if self.reg_val >= 0:
20            return f"{self.reg_val:032b}"
21        else:
22            return bin(self.reg_val & 0xFFFFFFFF)[2:]
23
24    def to_3bit_adr(self):
25        reg_map = {"r0": "000", "r1": "001", "r2": "010", "r3": "011",
26        "r4": "100", "r5": "101", "r6": "110", "r7": "111"}
27        return reg_map.get(self.reg_adr, "")
```

```

30 class InstructionSet:
31     def __init__(self, step, opcode, register, clkcy, operand="", value=None):
32         self.step = step
33         self.opcode = opcode
34         self.register = register
35         self.clkcy = clkcy
36         self.operand = operand
37         self.value = value if value is not None else register.get_reg_val()
38
39     def five_bit_opcode(self):
40         opcode_map = {
41             "mov": "00001",
42             "add": "00010",
43             "mul": "00100",
44             "sub": "00011",
45             "div": "00101",
46         }
47         return opcode_map.get(self.opcode, "00000")
48
49     def encode_instruction(self):
50         opcode = self.five_bit_opcode()
51         operand1 = self.register.to_3bit_adr()
52         operand2 = self.to_32bit_val()[-24:]
53         return f"[{opcode} {operand1} {operand2}]"
54
55     def to_32bit_val(self):
56         if self.value >= 0:
57             return f"{self.value:032b}"
58         else:
59             return bin(self.value & 0xFFFFFFFF)[2:]
60
61     def __str__(self):
62         decoded_form = f"[{self.step}] {self.opcode}{self.register.get_reg_adr()}"
63         if self.operand != "":
64             decoded_form += f" {self.operand}"
65         decoded_form = decoded_form.ljust(15)
66         encoded_form = self.encode_instruction()
67         return f"{decoded_form} {encoded_form}"
68

```

```

70 def main():
71     regs = [Registers(0, f"r{i}") for i in range(8)]
72     regs.append(Registers(0, "r7")) # Add r7 as a remainder register
73
74     instructions = []
75
76     print("Input instructions:")
77     print("Opcode: mov, add, mul, sub, and div")
78     print("Operand 1: R0 - R6")
79     print("Operand 2: R0 - R6 or a value")
80     print("r7 is used to store the remainder")
81     print("Type 'end 0 0' to start the simulation")
82     print("Type the opcode and Operand down below (for example: mov r1 345): ")
83     step = 0
84
85     while True:
86         instruction = input()
87         if instruction == "end 0 0":
88             break
89
90         opcode, operand1, operand2 = instruction.split()
91         operand2_reg = None
92         register = None
93
94         for reg in regs:
95             if reg.get_reg_adr() == operand1:
96                 register = reg
97             if reg.get_reg_adr() == operand2:
98                 operand2_reg = reg
99
100        if operand2_reg is None:
101            operand2_reg = Registers(int(operand2), operand2)
102
103        if operand1 != operand2:
104            operation_mapping = {
105                "mov": lambda dest, src: dest.set_reg_val(src.get_reg_val()),
106                "add": lambda dest, src: dest.set_reg_val(dest.get_reg_val() + src.get_reg_val()),
107                "sub": lambda dest, src: dest.set_reg_val(dest.get_reg_val() - src.get_reg_val()),
108                "mul": lambda dest, src: dest.set_reg_val(dest.get_reg_val() * src.get_reg_val()),
109                "div": lambda dest, src: dest.set_reg_val(dest.get_reg_val() // src.get_reg_val()),
110            }
111
112            # Update this section to handle r7 as a remainder
113            operation_mapping[opcode](register, operand2_reg)
114            instructions.append(InstructionSet(
115                step, opcode, register, 1, operand2_reg.get_reg_adr(), operand2_reg.get_reg_val()))
116
117            # Handle r7 as a remainder
118            if opcode == "div":
119                remainder = register.get_reg_val() % operand2_reg.get_reg_val()
120                regs[7].set_reg_val(remainder) # Save remainder to r7
121
122            step += 1
123
124
125     print_output(instructions, regs)

```

```

128 def print_output(instructions, regs):
129     print("\n Decoded Form          Encoded Form          Clock Cycles")
130     for instruction in instructions:
131         decoded_form = f"{instruction.step + 1}. {instruction.opcode} {instruction.register.get_reg_adr()}"
132         if instruction.operand != "":
133             decoded_form += f" {instruction.operand}"
134         decoded_form = decoded_form.ljust(20)
135         encoded_form = instruction.encode_instruction().ljust(47)
136         print(f"{decoded_form} {encoded_form} {instruction.clkcyc}")
137
138     # Result
139     print("\nValues of registers after the execution:")
140     for reg in regs:
141         reg_adr = reg.get_reg_adr()
142         reg_val = reg.get_reg_val()
143         if reg_adr == 'r7' and reg_val == 0:
144             continue # Skip printing r7 if its value is 0
145         print(f"{reg_adr} {reg_val:3} [{reg.to_32bit_val()}]")
146
147     # Clock cycle Calculation
148     total_clk_cycles = sum(instruction.clkcyc for instruction in instructions)
149     cpi = total_clk_cycles / len(instructions)
150     print("\nCPI value is", cpi)
151
152     clkcs_with_pipeline = len(instructions) + 3
153     print("\nThe pipelined version showing execution of the program")
154     print("*" * 65)
155     print(f"{'':15}", end="")
156     for x in range(1, clkcs_with_pipeline + 1):
157         print(f"{x:5d}", end="")
158
159     for instruction in instructions:
160         if instruction.operand == "":
161             print(
162                 f"\n{instruction.step + 1}. {instruction.opcode} {instruction.register.get_reg_adr()} {instruction.value:2}", end=" ")
163         else:
164             print(
165                 f"\n{instruction.step + 1}. {instruction.opcode} {instruction.register.get_reg_adr()} {instruction.operand}", end=" ")
166         for _ in range(instruction.step + 1):
167             print(" " * 5, end="")
168         print("IF | ID | EX | WB", end="")
169
170     print(
171         f"\n\nPipelined execution took {clkcs_with_pipeline} clock cycles to complete the program execution")
172
173 if __name__ == "__main__":
174     main()

```