DLD PROJECT REPORT

4-Bit Arithmetic Logic Unit

NUST College of E&ME
Digital Logic Design

Group # 2

DEPARTMENT OF Electrical ENGINEERING
COLLEGE OF E&ME, NUST, RAWALPINDI

EE221- Digital Logic Design
PROJECT Report:

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Lab Project:

4 Bit Arithmetic Logic Unit

Abstract:

This project presents the design and implementation of a 4-bit Arithmetic Logic Unit (ALU) using fundamental digital logic ICs. The ALU performs essential arithmetic and logical operations including addition, subtraction, OR, AND, NOR, increment, decrement, comparison, and complement functions. Various integrated circuits such as the 7483 adder, 7486 XOR, 7408 AND, 7432 OR, and 4067 multiplexers were used to construct the system. A comparator, counter, and multiple multiplexers were incorporated to expand the ALU's functionality. The final circuit was tested using Proteus simulation and validated through hardware implementation on a breadboard. This design demonstrates the integration of basic logic components to build a functional multi-operation ALU.

Apparatus:

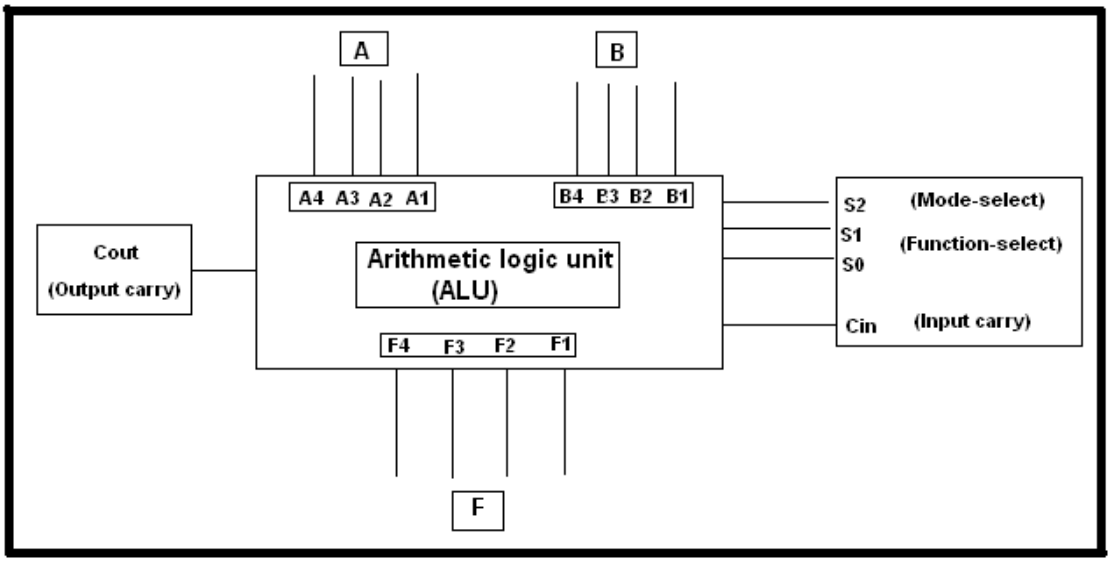
- DC Supply (5V constant input)
- Power Supply (Clock)
- Breadboard
- Jumper Wires
- Connecting Wires
- LEDs
- 7486 ic (XOR Gate)
- 7408 ic (AND Gate)
- 7432 ic (OR Gate)
- 7404 ic (NOT Gate)
- 7483 ic (4-bit full Adder)
- 74157 ic (Quad 2 to 1 Multiplexer with 1 select line)
- 7485 ic (4-bit Comparator)
- 74163 ic (4-bit Counter)
- 4067 ic (16 channel MUX)
- Proteus

4-Bit Arithmetic Logic Unit (ALU):

Introduction:

A 4-bit ALU (Arithmetic Logic Unit) is a digital circuit that performs arithmetic and logical operations on 4-bit binary numbers. It is a fundamental building block of a computer's central processing unit (CPU) and is essential for executing instructions in computer programs. The 4-bit ALU can handle operations such as addition, subtraction, and logical comparisons, making it crucial for various digital systems.

Circuit Diagram:



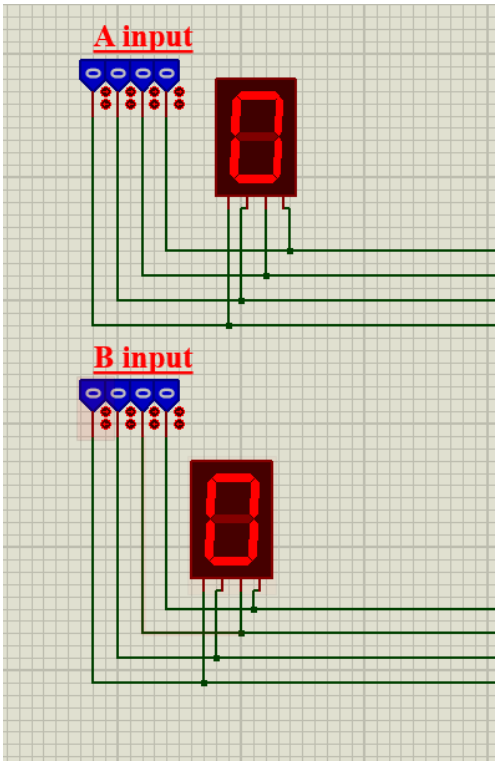
ALU Operations:

1. Addition
2. Subtraction
3. Bit wise OR
4. Bit wise AND
5. Bit wise NOR
6. 1's Complement of A & B
7. 2's Complement of A & B
8. Increment of A & B
9. Decrement of A & B
10. Counter
11. Comparator
12. Load A

ALU Functions:

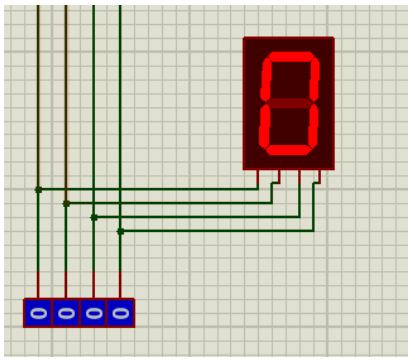
- ## Input Probs:

  Here we take input A and input B. Input A & B are 4-bit inputs. The input is Displayed by a 7 segment BCD.



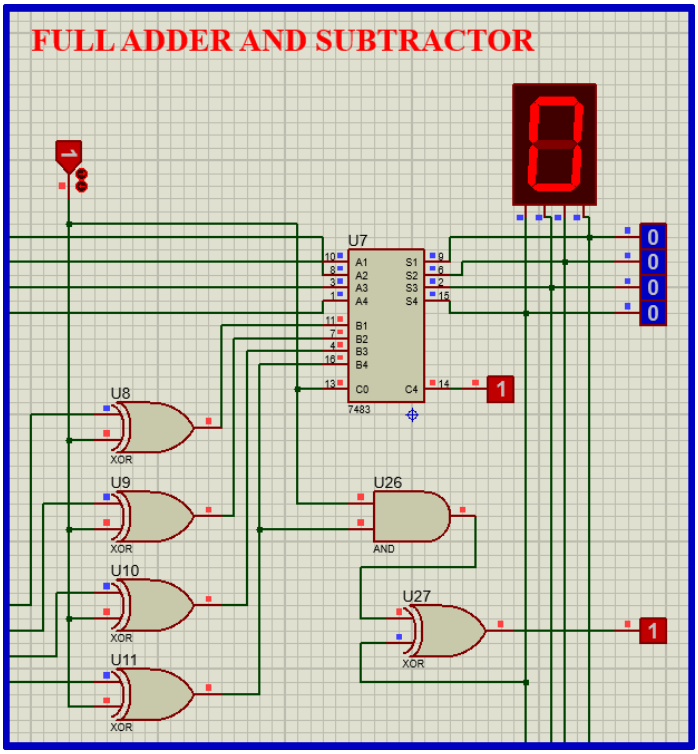
- ***Output Probes:***

The output is Displayed by the output probes and also through the 7 segment BCD. We choose the operation we want to perform by the select lines



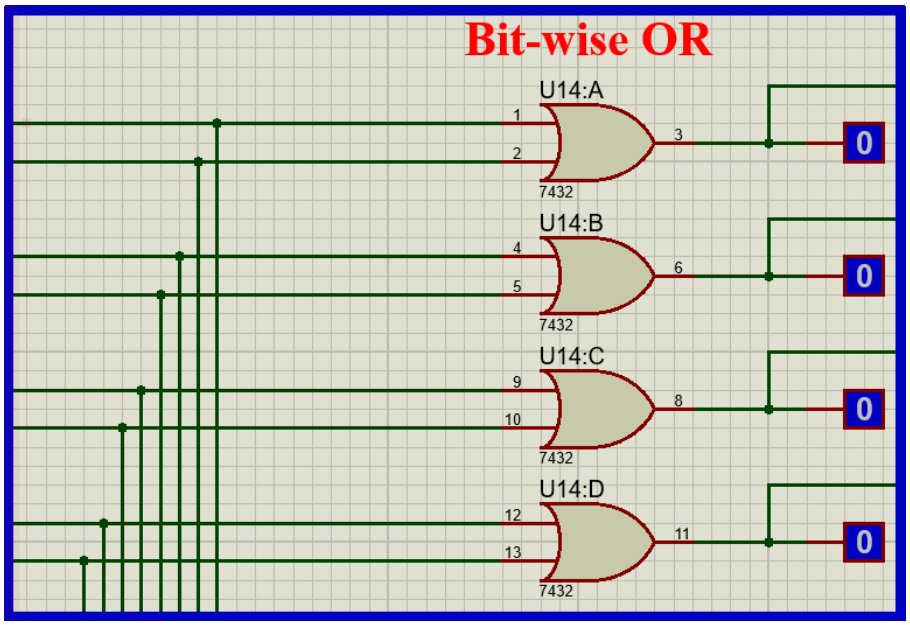
- ***Adder / Subtractor:***

Here, we are using a ripple carry adder IC that consists of four full adders. The one IC can both add and subtract our two inputs. This is achieved by connecting the B input with XOR gates and one input of all XOR gates 1 which is directed into RCA. C_0 is connected with last select line which makes RCA to perform either addition or subtraction.



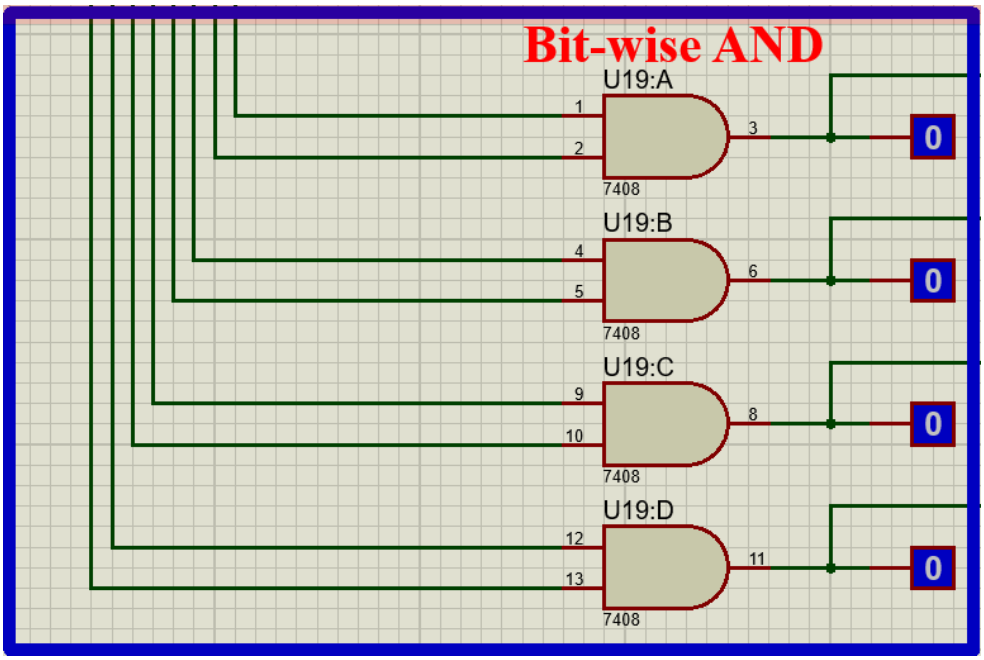
- ***Bit wise OR:***

Four OR gates are used here to find OR of individual input A's bits with B's bits.



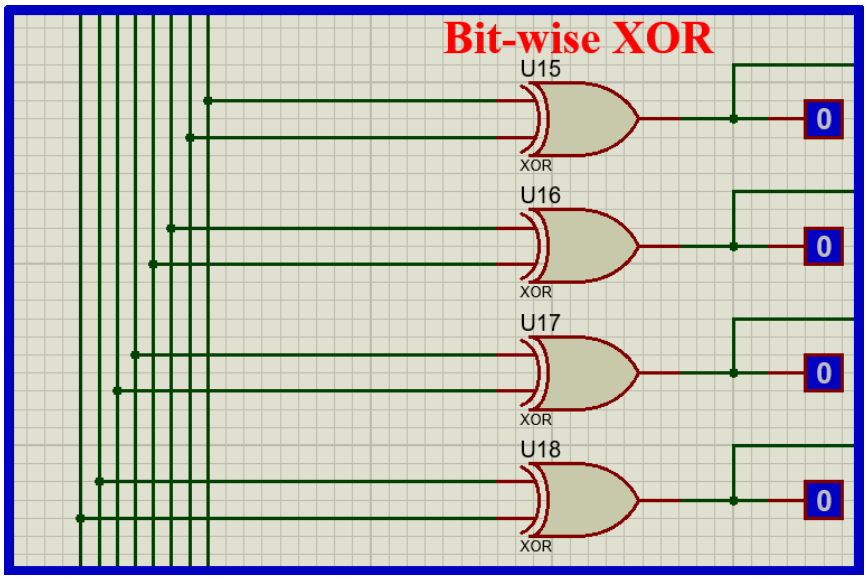
- ***Bit wise AND:***

Four AND gates are used here to find and of individual input A's bits with B's bits.



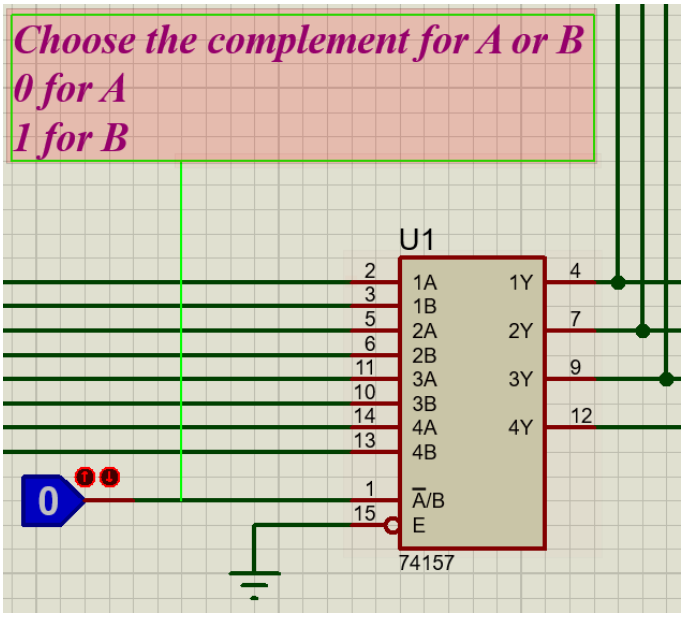
- ***Bit wise NOR:***

Four XOR gates are used here to find XOR of individual input A's bits with B's bits.

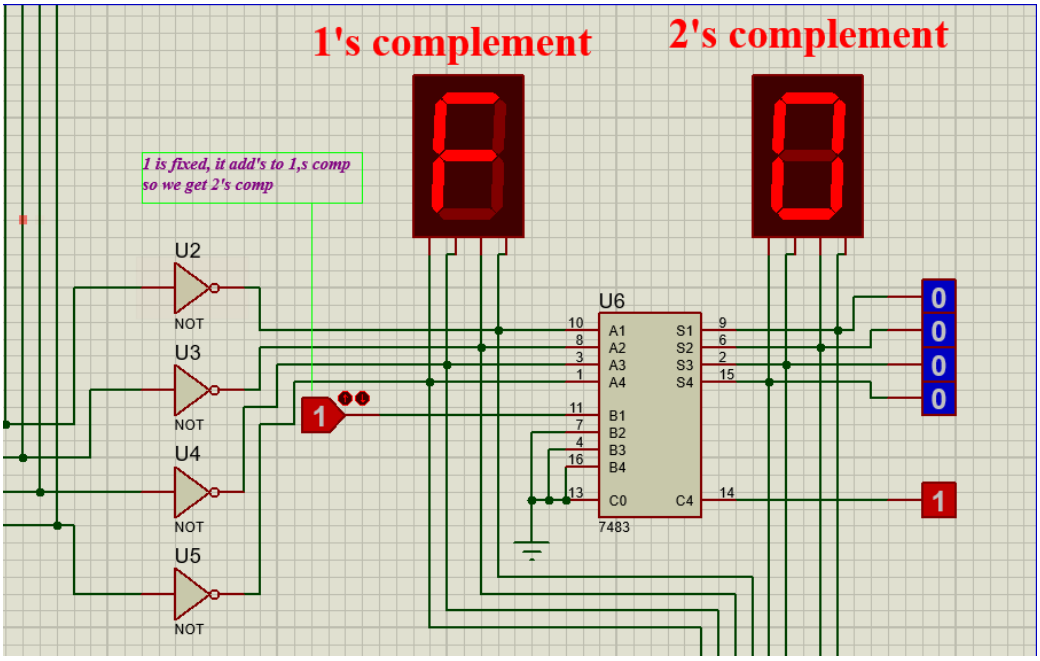


- ***Multiplexer:***

We have used 74157 ic which is a Quad 2 to 1 multiplexer with 1 select line. We give A and B to the Mux as input and based on the carry (c_{in}) either one of the inputs is displayed at the output. Here when the carry (c_{in}) is 0 A is displayed and when the carry (c_{in}) in 1 B is displayed.

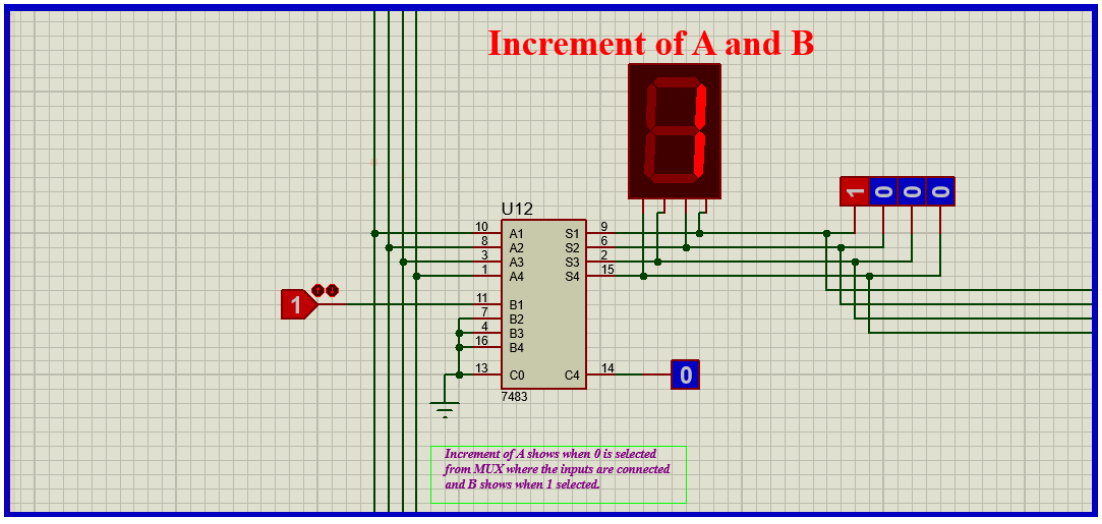


- ***1's & 2's Complement:***
  - We have used 7404 ic which performs NOT operation to take 1`s complement. This ic takes input from Mux selecting A or B.
  - 2`s complement is obtained simply by using Adder ic which takes one input from 1`s complement and other is given as 1 at the LSB and 0 at others (0001).



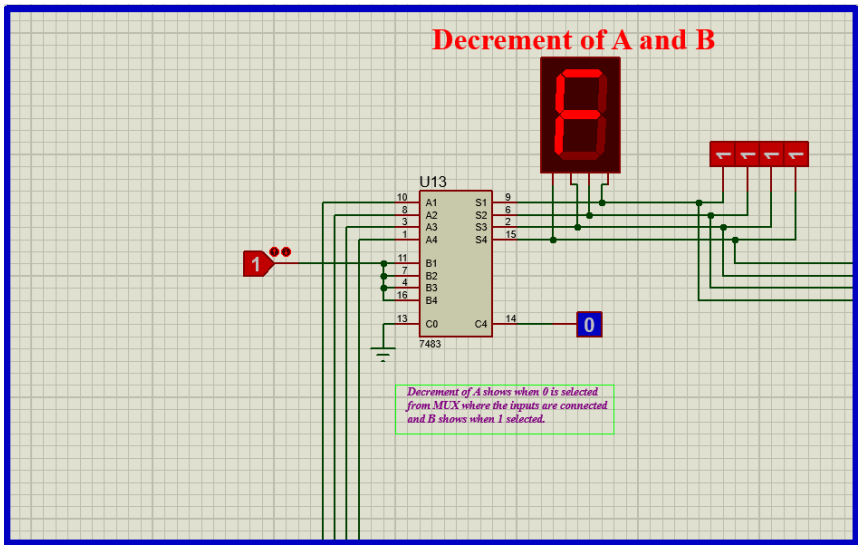
- ***Increment of A or B:***

We have used 7483 adder IC in order to increment our inputs by giving 1 at the LSB of second input of IC. Taking 1st input from previous defined MUX.



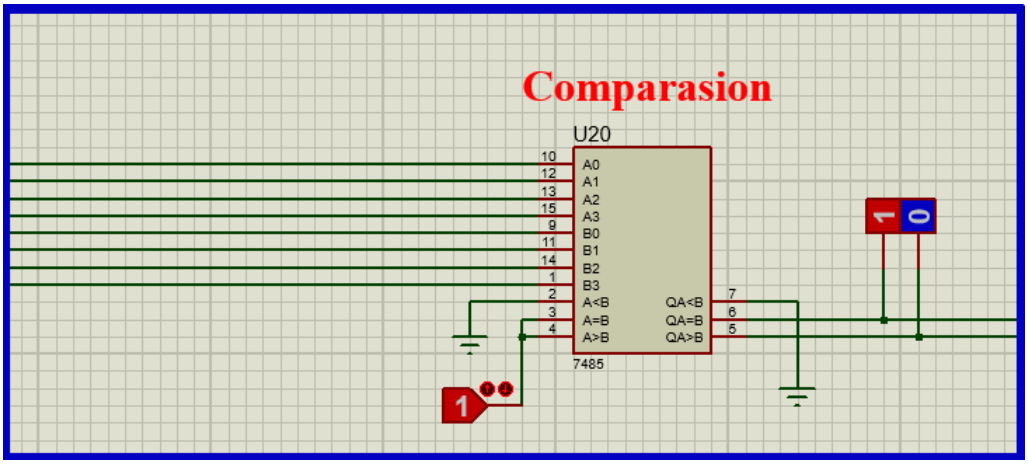
- ***Decrement of A or B:***

We have used 7483 adder IC in order to decrement our inputs by giving 1 at the second input of IC. Taking 1st input from previous defined MUX.



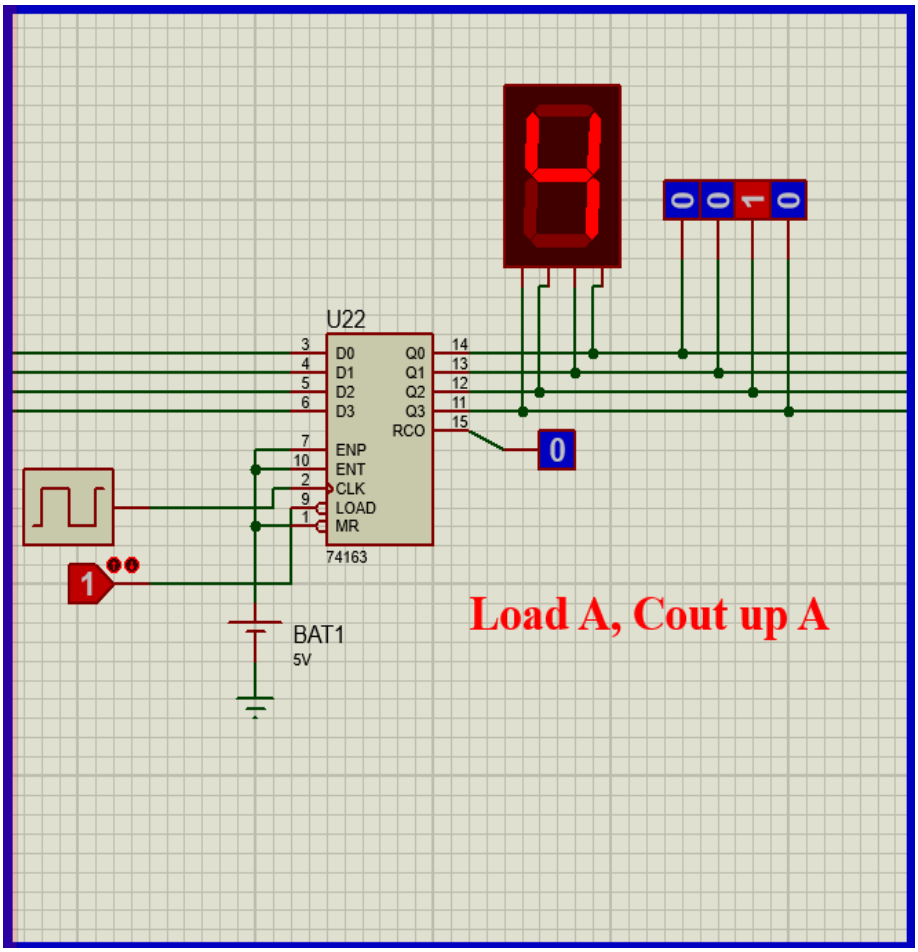
- ***Comparator:***

We make use of 7485 IC(Comparator) which takes input A and B. The pin no 6 checks if A is equal to B by checking from most significant bit to least significant bit and if it's true gives out output 1. The pin number 5 checks if A is greater than B (A > B), if it's true it gives out output 1. (Only one condition works at one time)



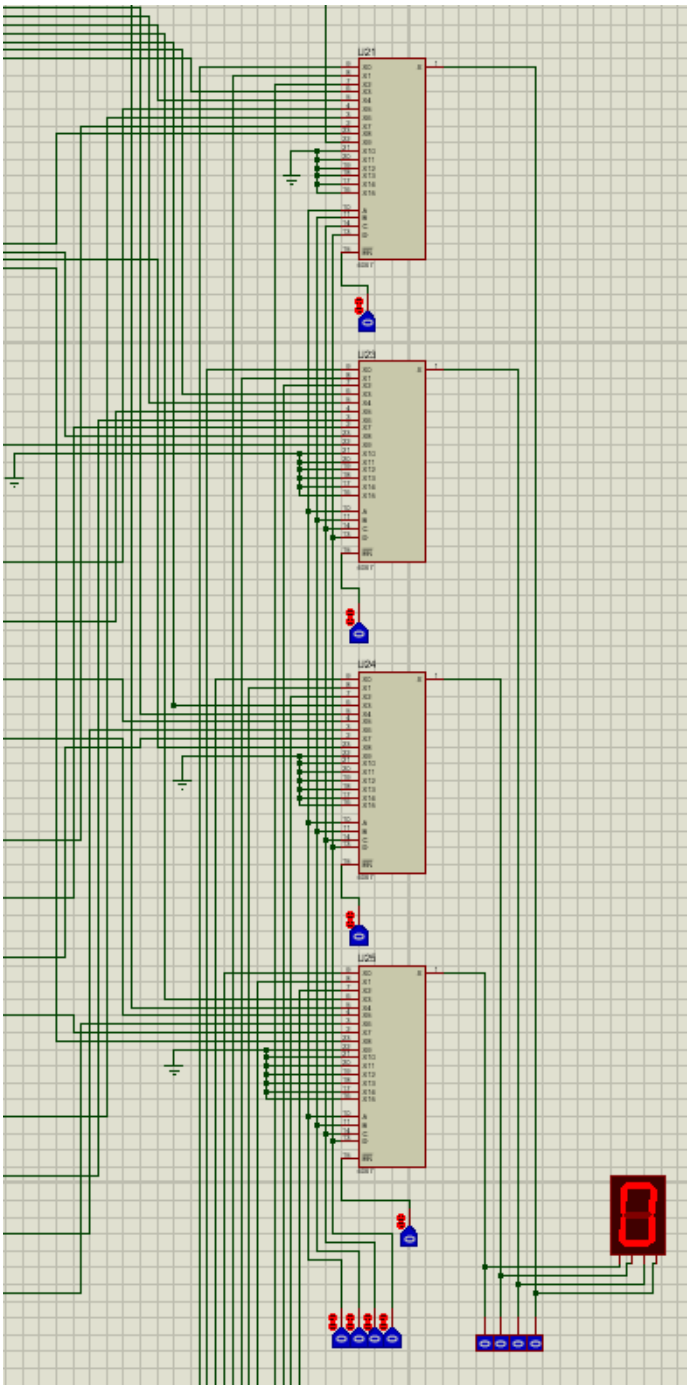
- ***Counter / Load A:***

We are using the previous multiplexer to load values into the counter ic. Clock is practically provided by Function Generator but it is an expensive way.



- ***MUX Selecting Output:***

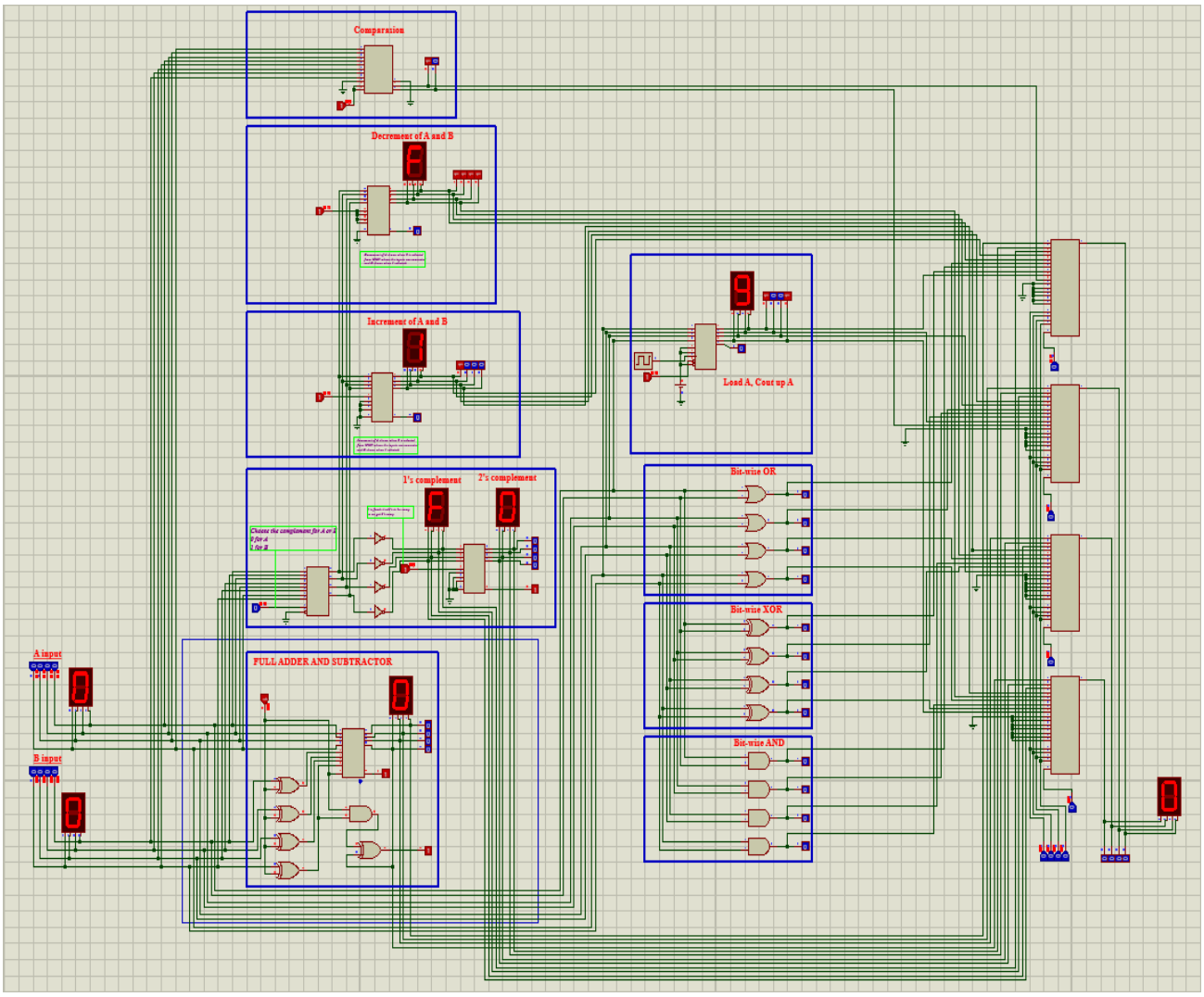
  Four 16 to 1 multiplexers (4067 ic) are used in this part. They take input from the outputs of the sixteen operations being performed in the circuit and each multiplexer's output bit is a part of the 4-bit final output and according to the selector gives out the one required output out of the sixteen.



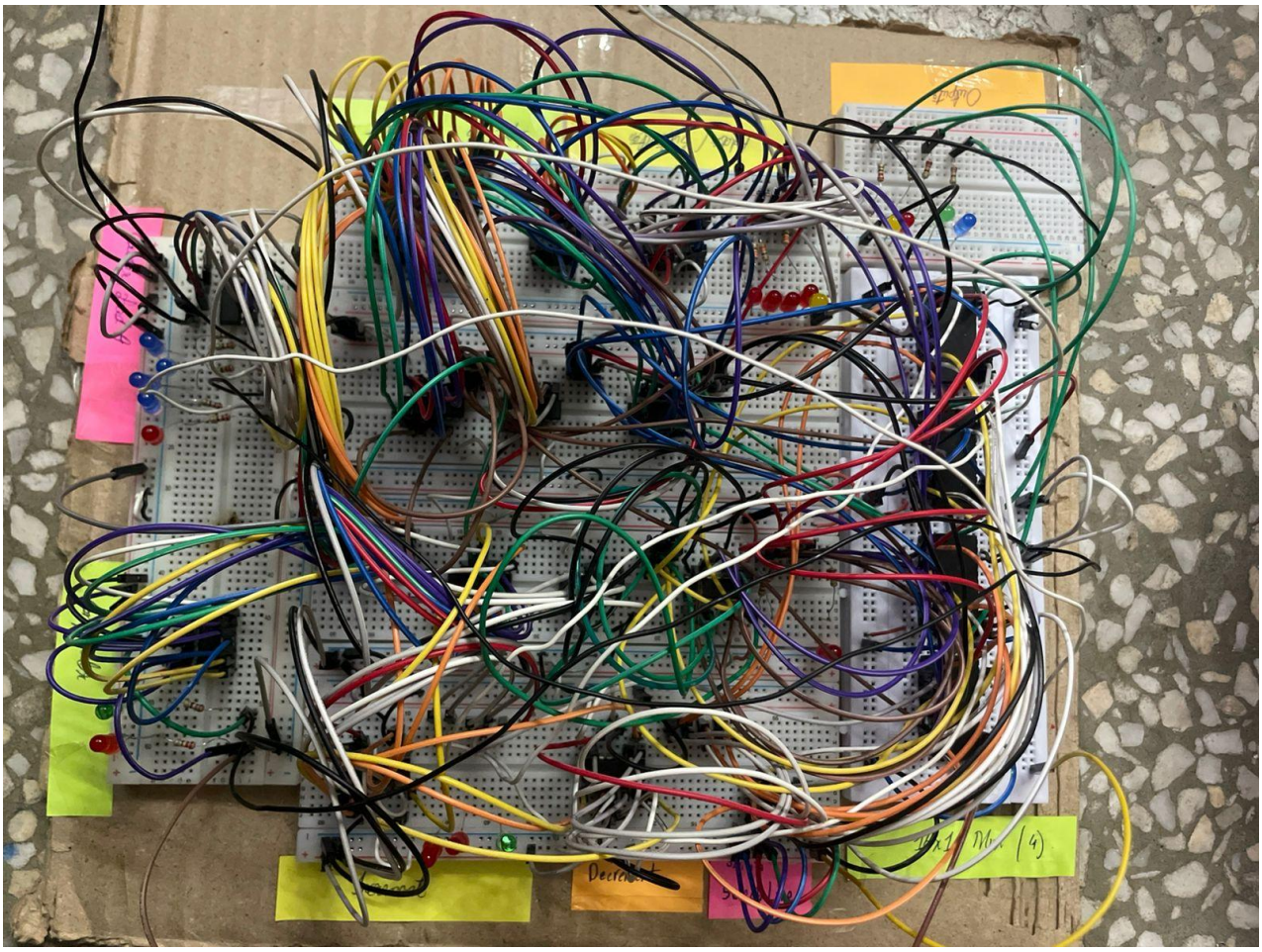
Operation Selection Table:

Select Line:	***Function***
0000	Adder / Subtractor
0001	Bit wise OR
0010	Bit wise AND
0011	Bit wise NOR
0100	1's Complement of A or B
0101	2's Complement of A or B
0110	Increment of A or B
0111	Decrement of A or B
1000	Comparator
1001	Counter
1010 → 1111	Don't Care

Final Circuit (Proteus):



Final Circuit (Hardware):



Conclusion:

The 4-bit ALU was successfully designed using standard logic ICs and implemented both in simulation and hardware. Each module performed its intended function, demonstrating the correct execution of arithmetic and logical operations. The use of multiplexers allowed efficient selection among sixteen different outputs. The comparator and counter further enhanced the versatility of the circuit. Through systematic testing on Proteus and breadboard hardware, the ALU proved to be reliable and accurate. This project strengthened our understanding of combinational and sequential circuit design and showed how small modules combine to form a complete digital processing unit.

End