# Sistemi Operativi I

Corso di Laurea in Informatica

2023-2024

Gabriele Tolomei

Dipartimento di Informatica

Sapienza Università di Roma

tolomei@di.uniroma1.it

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## A Quick Step Back: Segmentation

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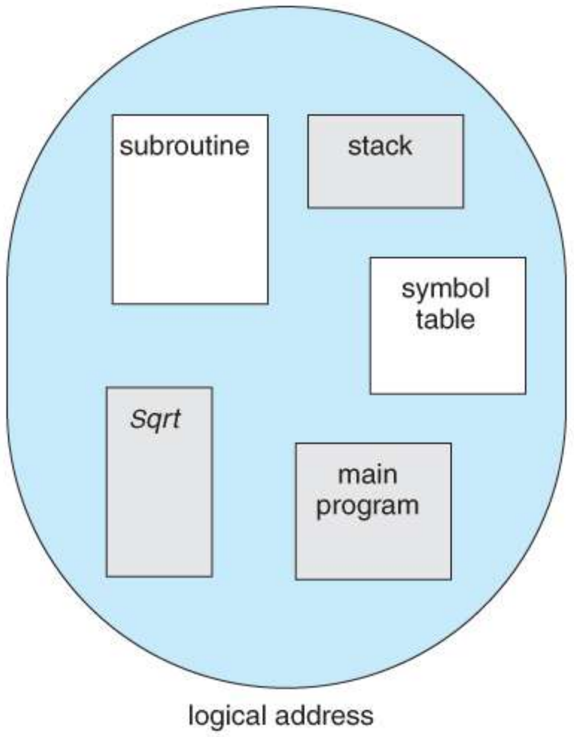
- Rather they think of memory divided in multiple **segments**, each dedicated to a specific use, such as code, data, stack, heap, etc.
- Memory segmentation supports this view by providing addresses with a **segment number** (mapped to a segment base address) and an **offset**

# Segmentation: Example

A C compiler generating 5 segments for the user code, library code, global (static) variables, the stack, and the heap



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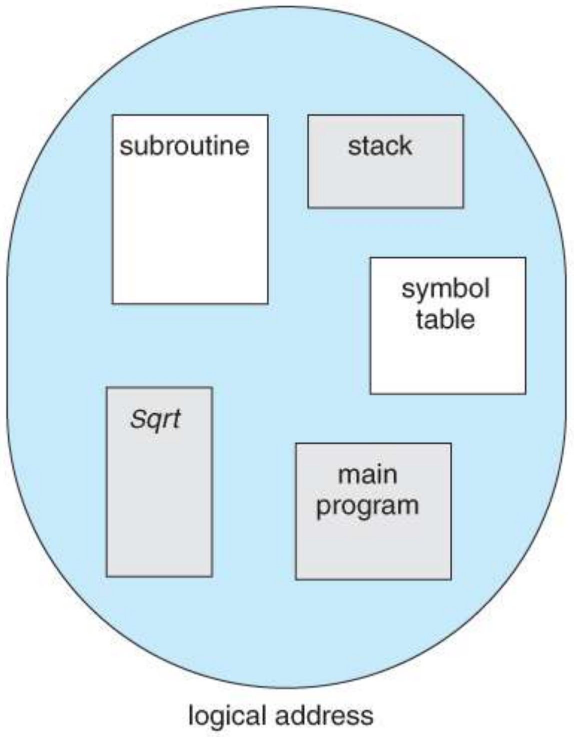
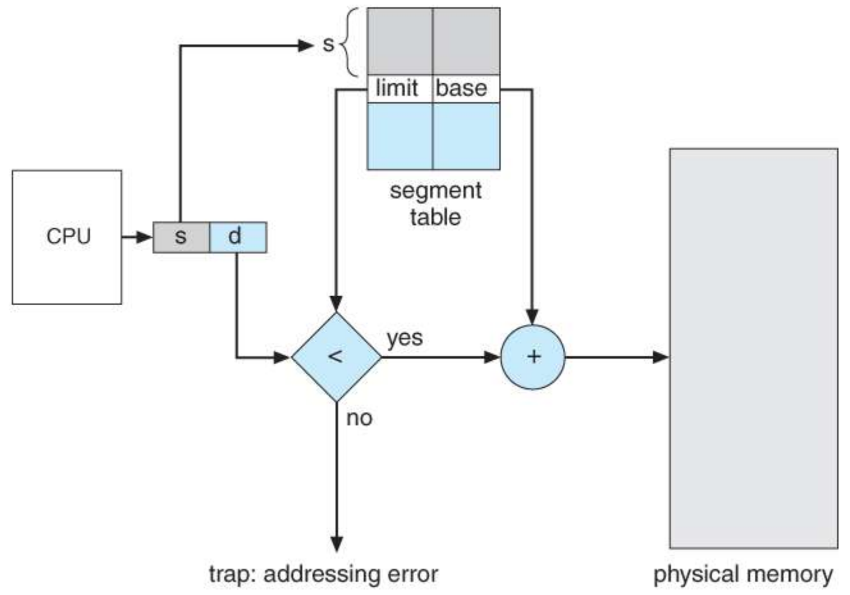


The compiler generates addresses identifying segments and offset

## Segmentation Hardware

A segment table maps segment-offset addresses to physical addresses, and simultaneously checks for invalid addresses, using a system similar to the page tables and relocation base registers discussed previously



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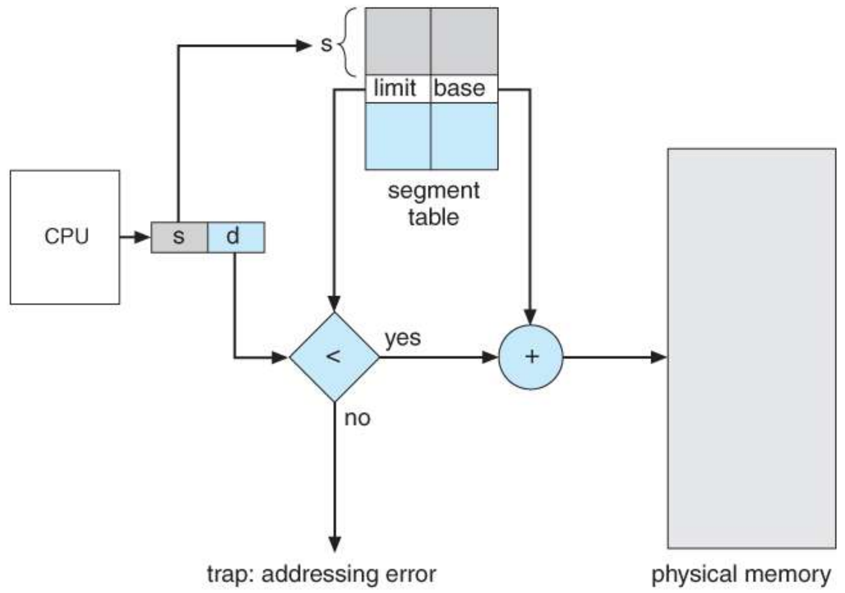
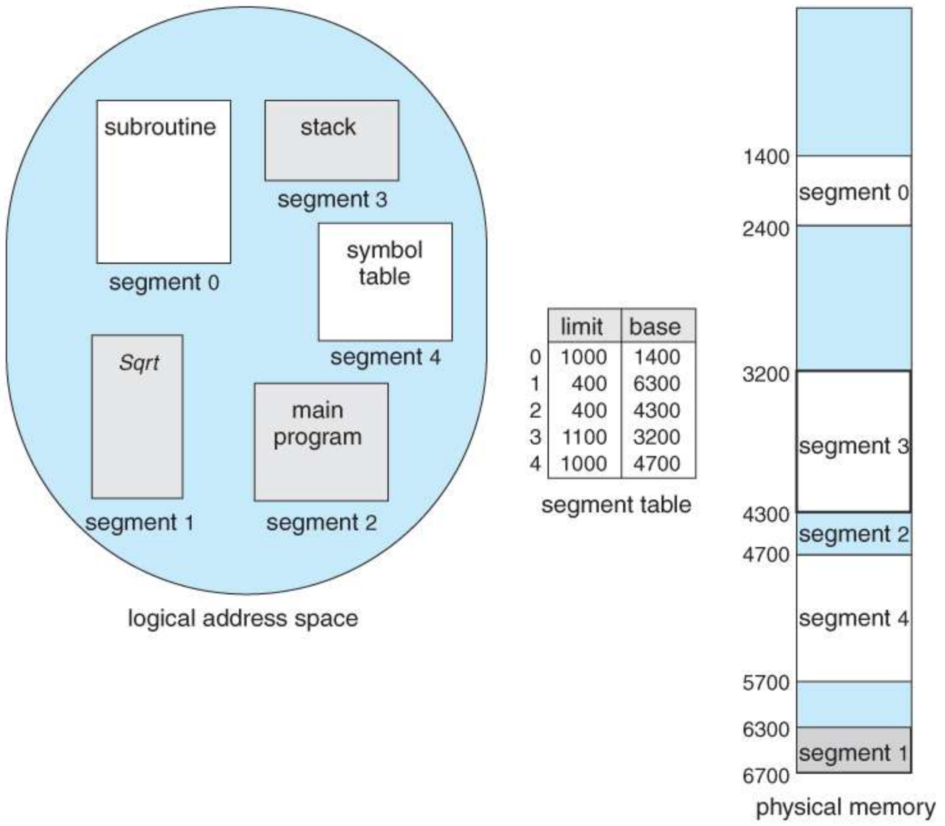


Note that we came back to the assumption that each segment is kept in contiguous memory and may be of different size…

# Segment Table

Each entry contains a base address in memory, the length of the segment, plus additional protection information (e.g., sharing, read/write permissions)



| | limit | base |
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segment table

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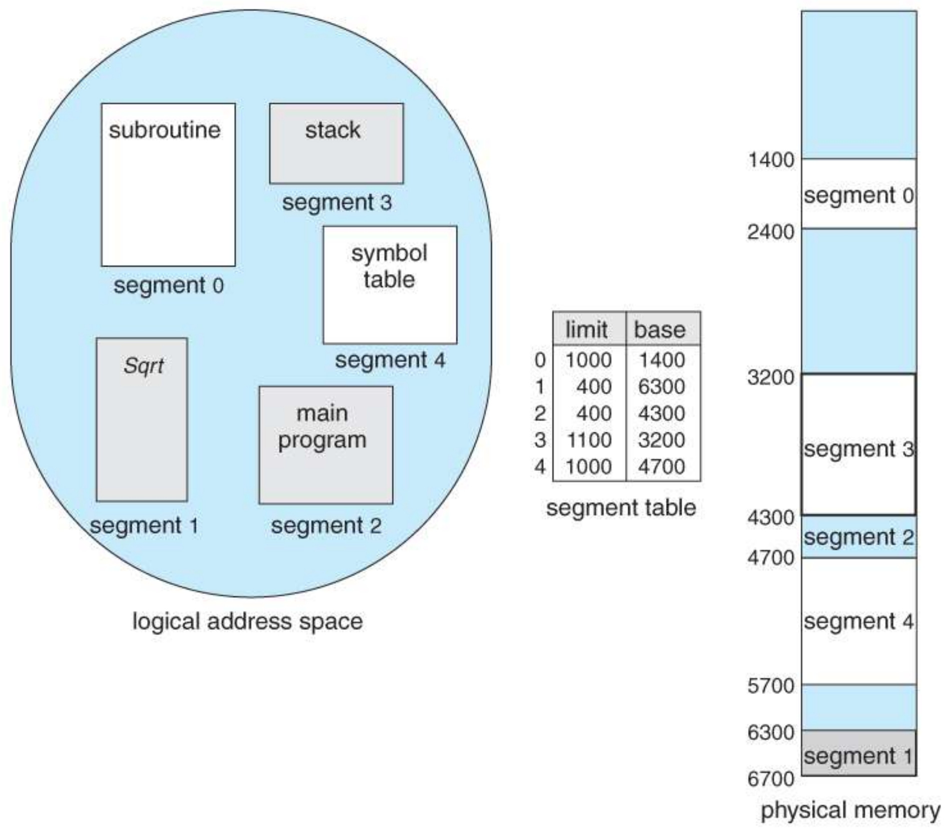

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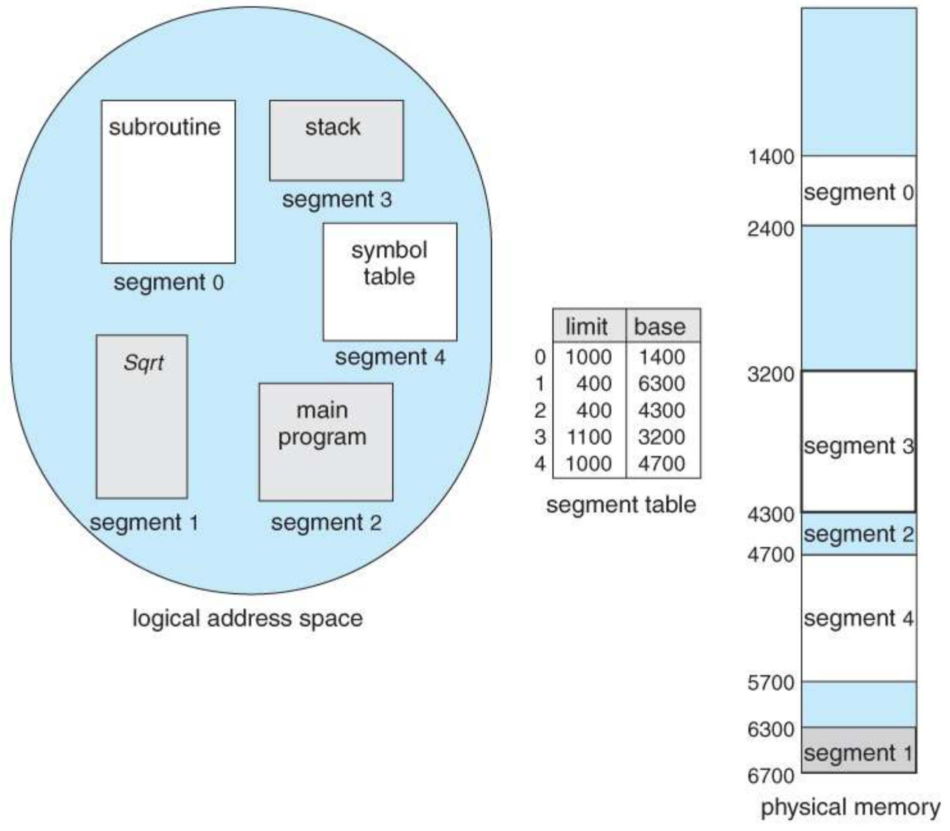

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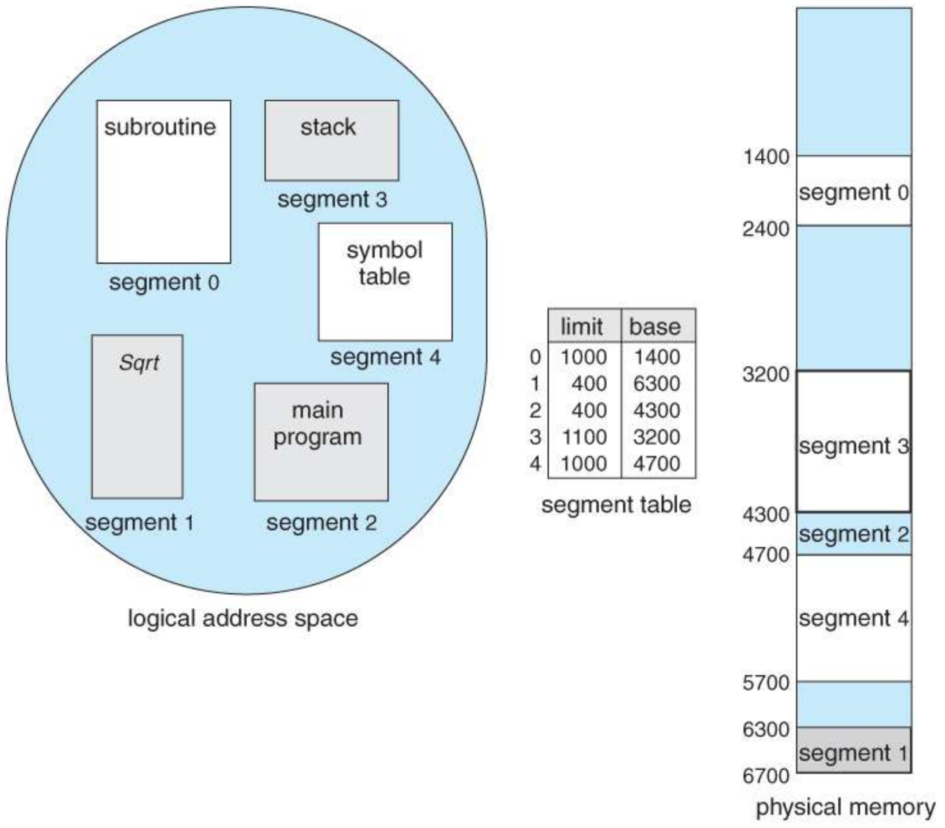

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Segment Table, instead, must store a very limited amount of segments per process (3÷5)

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- Additional HW (like TLB cache) might be needed if programs use many logical segments

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Try to get the best of both world

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Segmentation
ease of sharing

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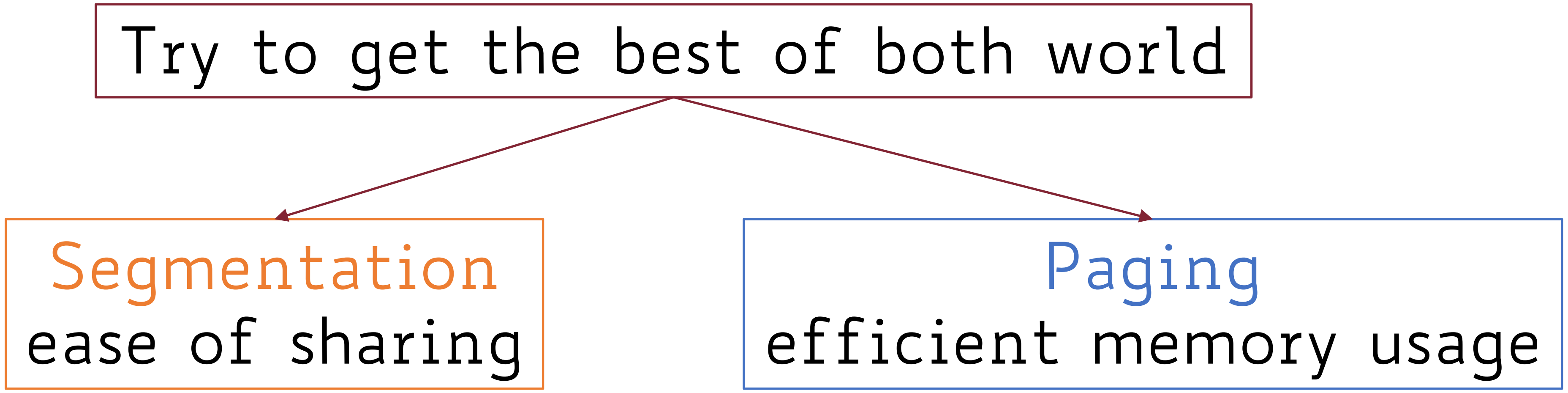

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Apply paging to segments!

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$\Downarrow$

Map a logical segment onto multiple page frames

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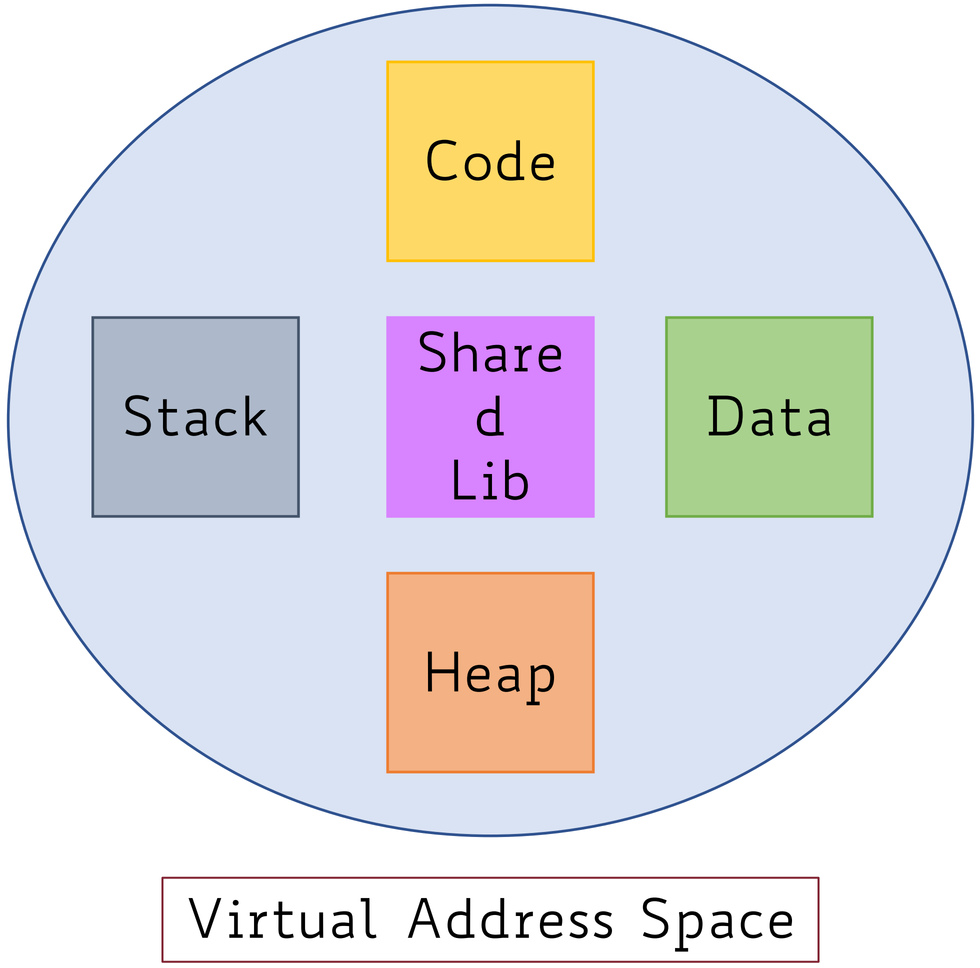

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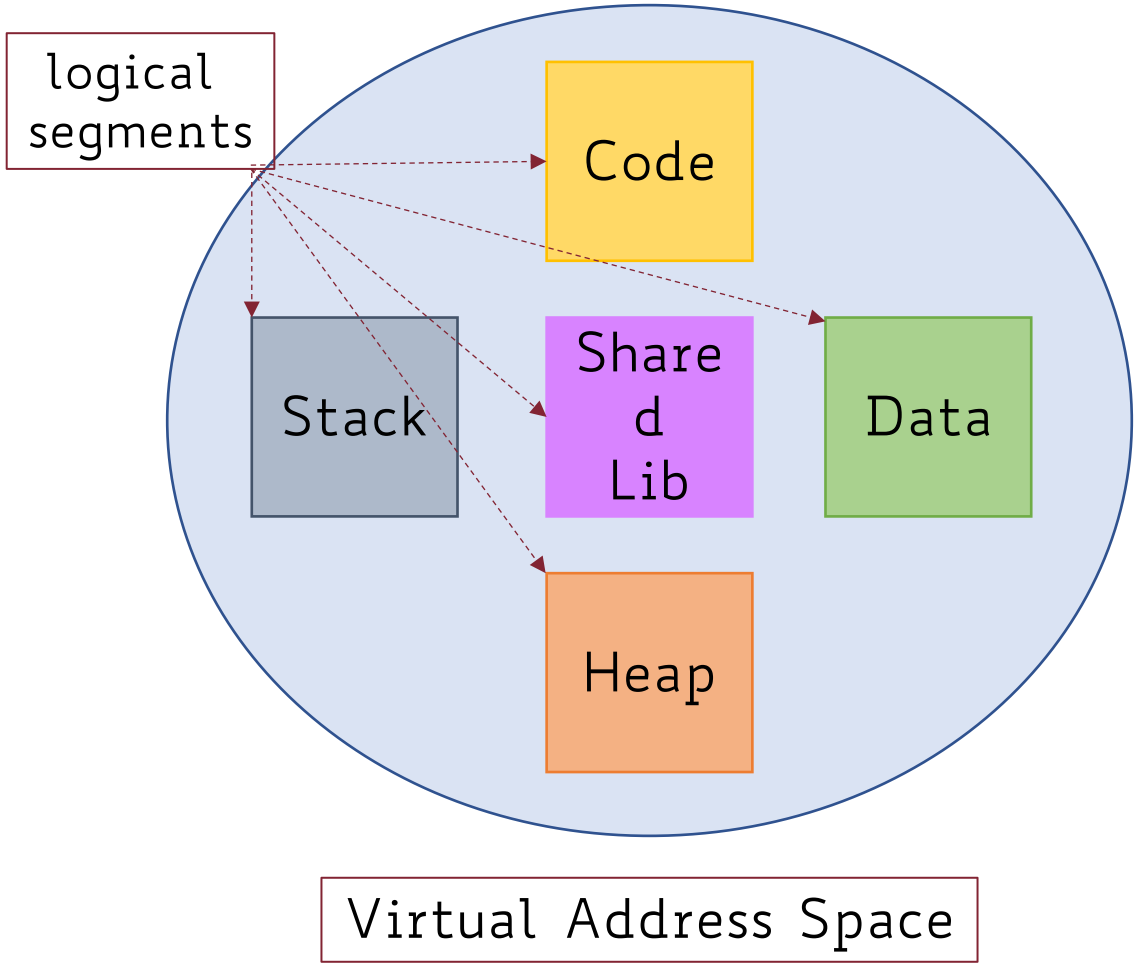

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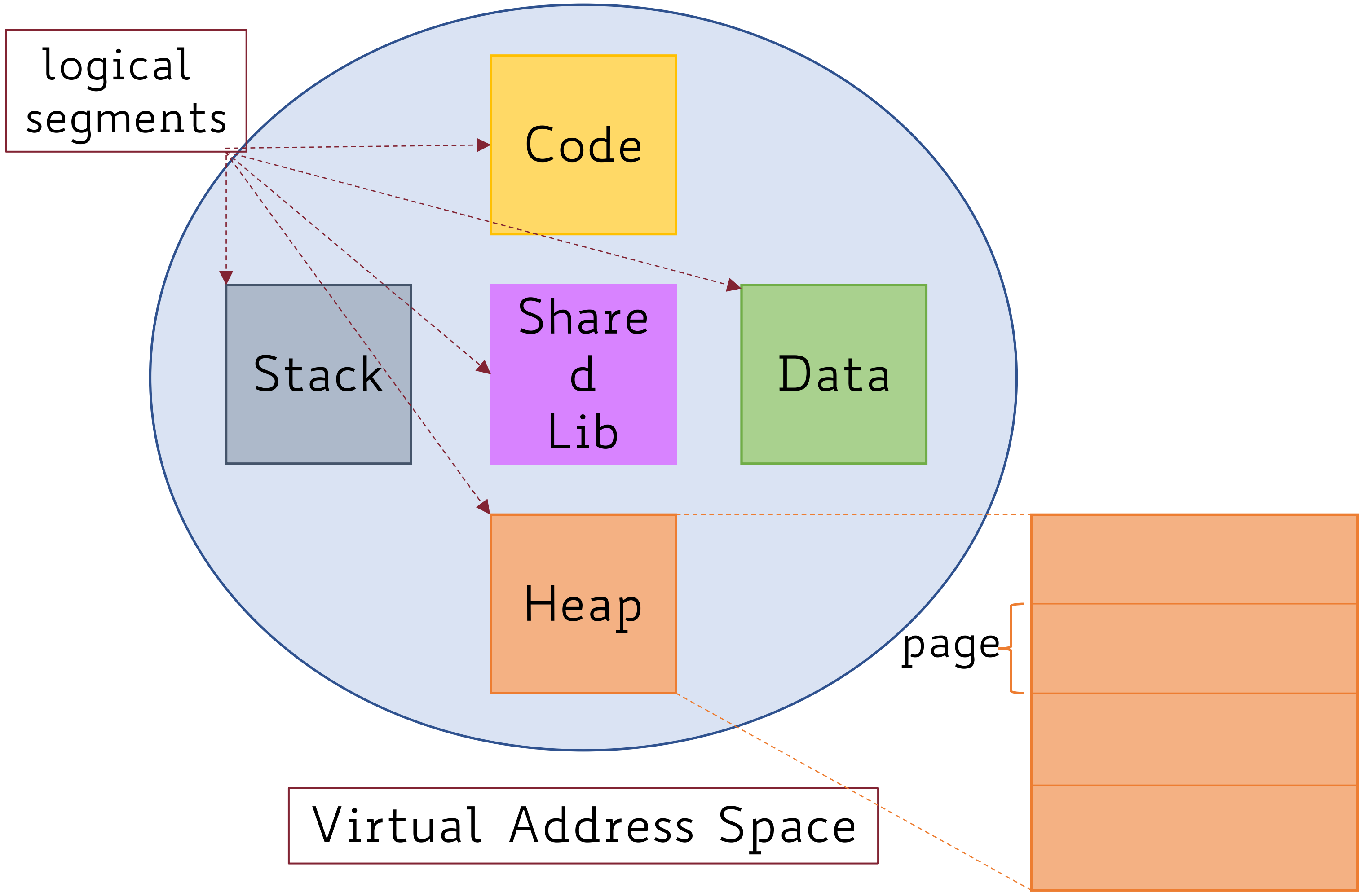

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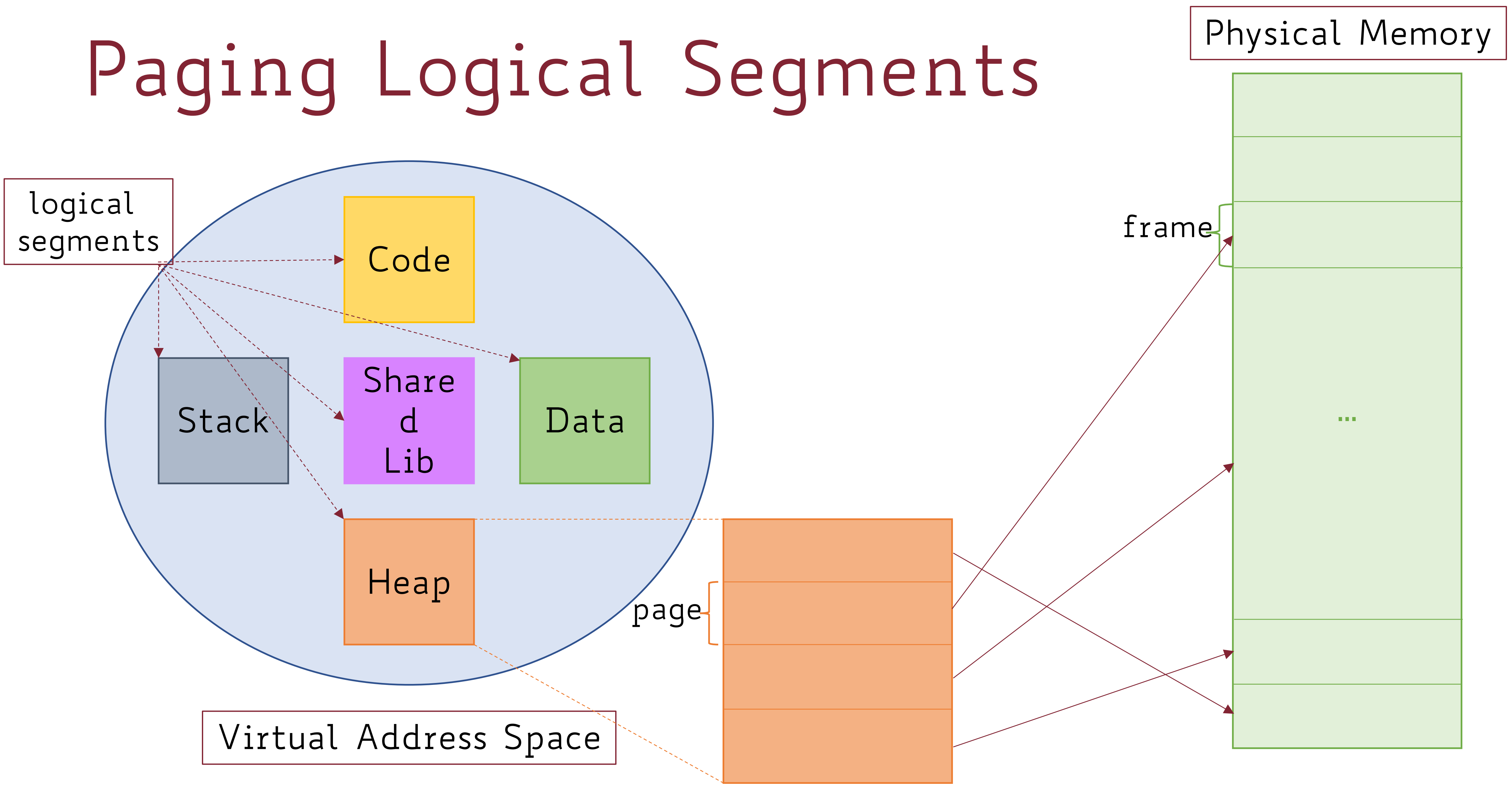

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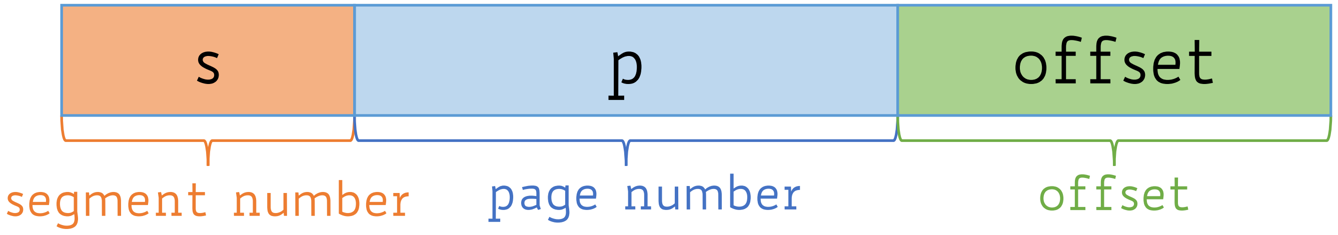

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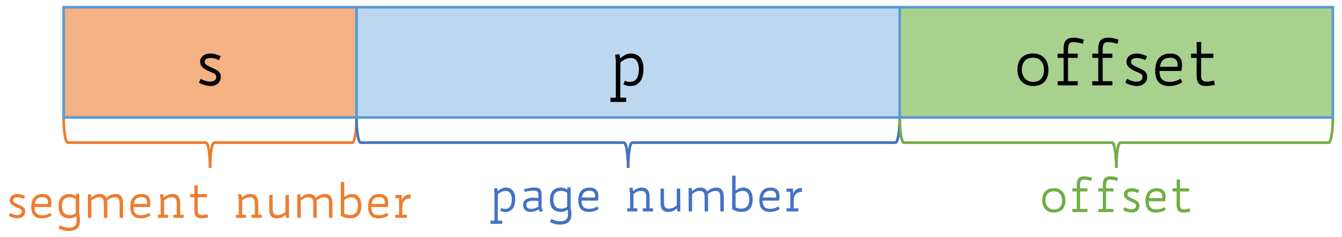

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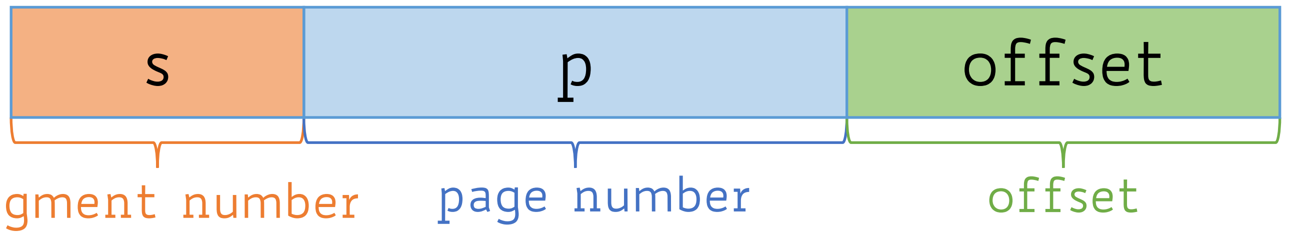

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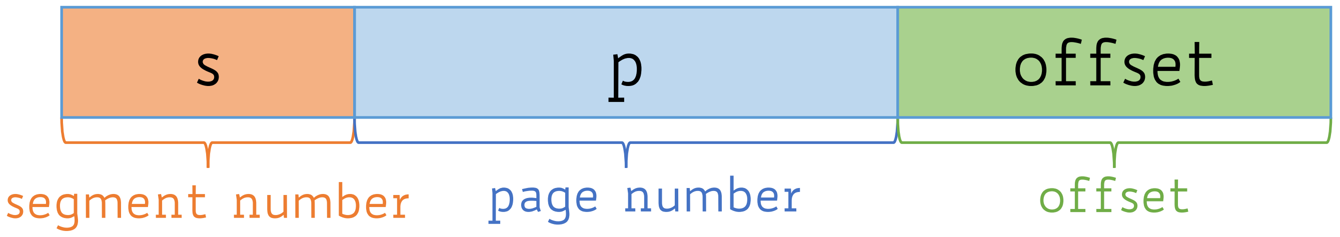

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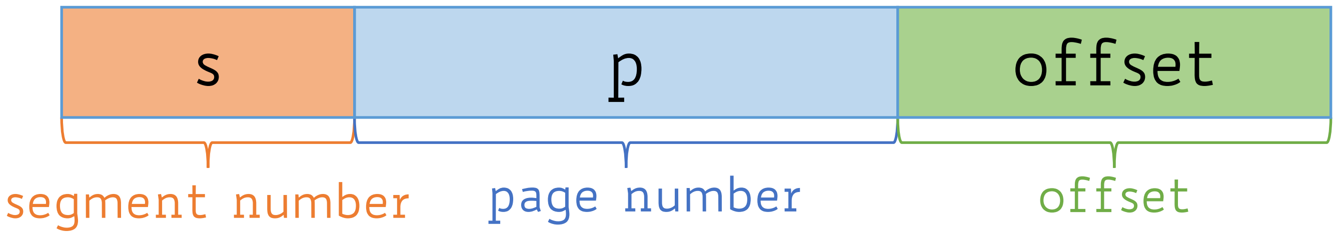

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- Add the frame number to the offset to get the physical address

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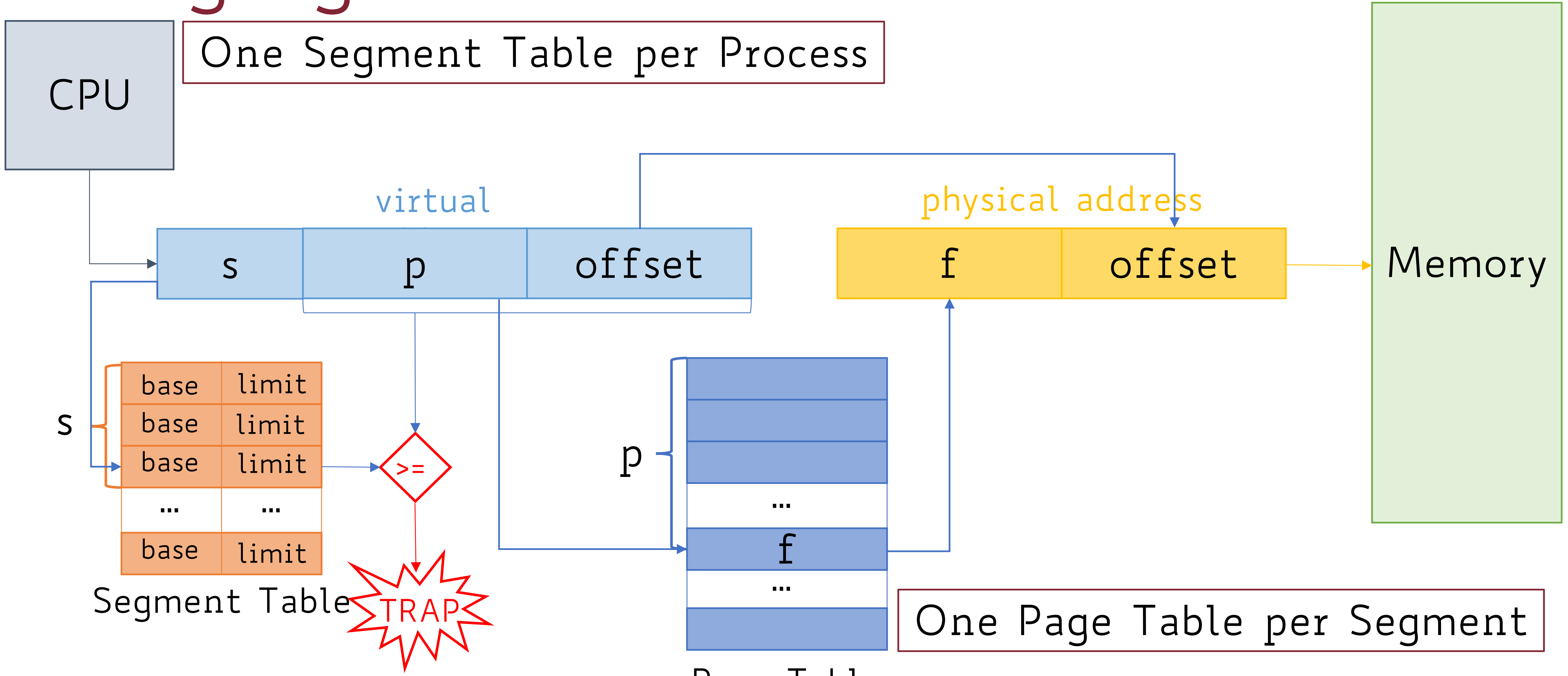

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both segment tables and page tables in main memory with TLB cache
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Slower but more flexible

## Segmented Paging Hardware: Practical Example 3

Suppose a physical memory of 1024 addressable words (assuming 1 word = 1 byte)

Frame size is 64 words (i.e., 64 bytes)

Page table size (i.e., number of entries) is thus 1024 bytes/64 bytes per frame = 16

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10 bits to address M = 1024/1 = 1024 1-byte words

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13 bits (virtual address) vs. 10 bits (physical address)

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- Even more flexible!

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  - Slower address translation (why?)

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- The larger the page size the higher the chance of internal fragmentation

## Advanced Paging

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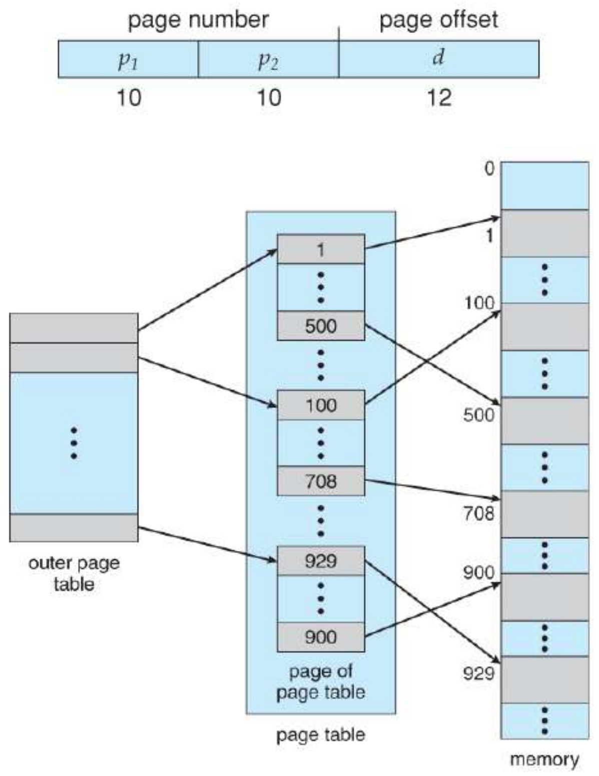
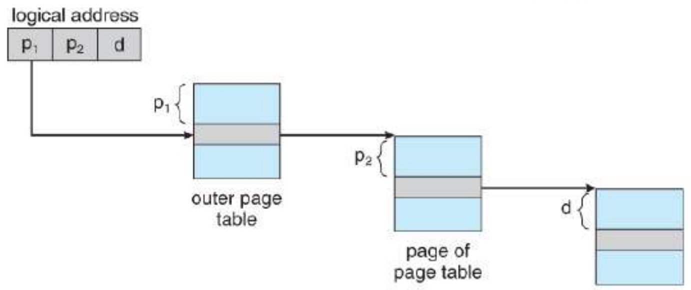
**More advanced paging structures are needed!**

# Advanced Paging: Two-Tier Page Table

Let's page the page table!





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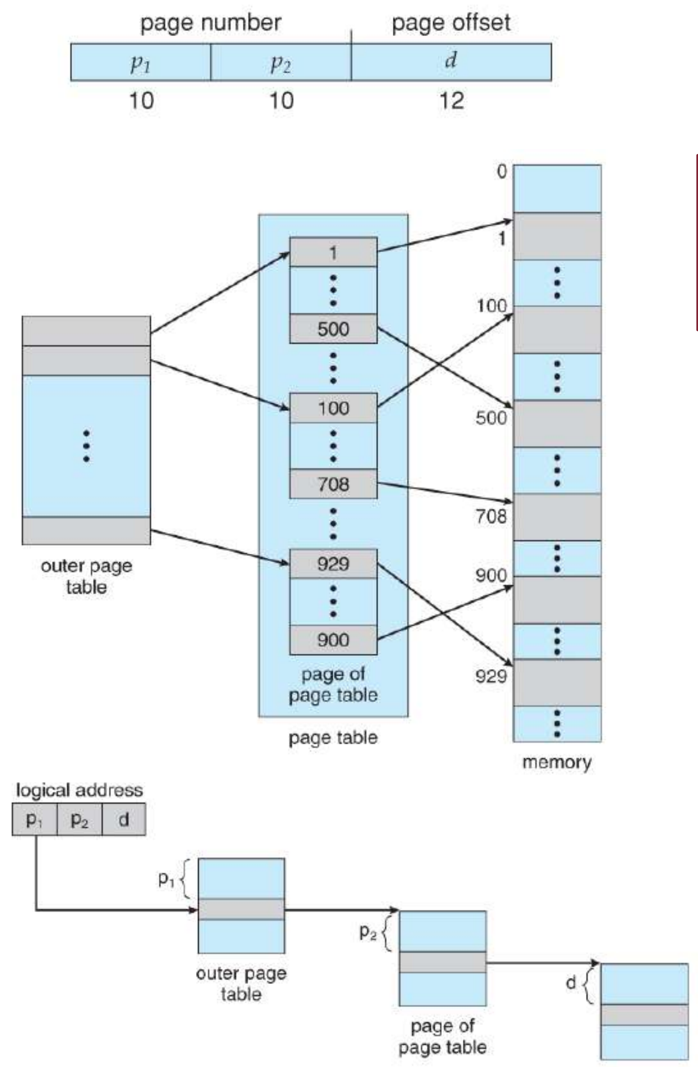

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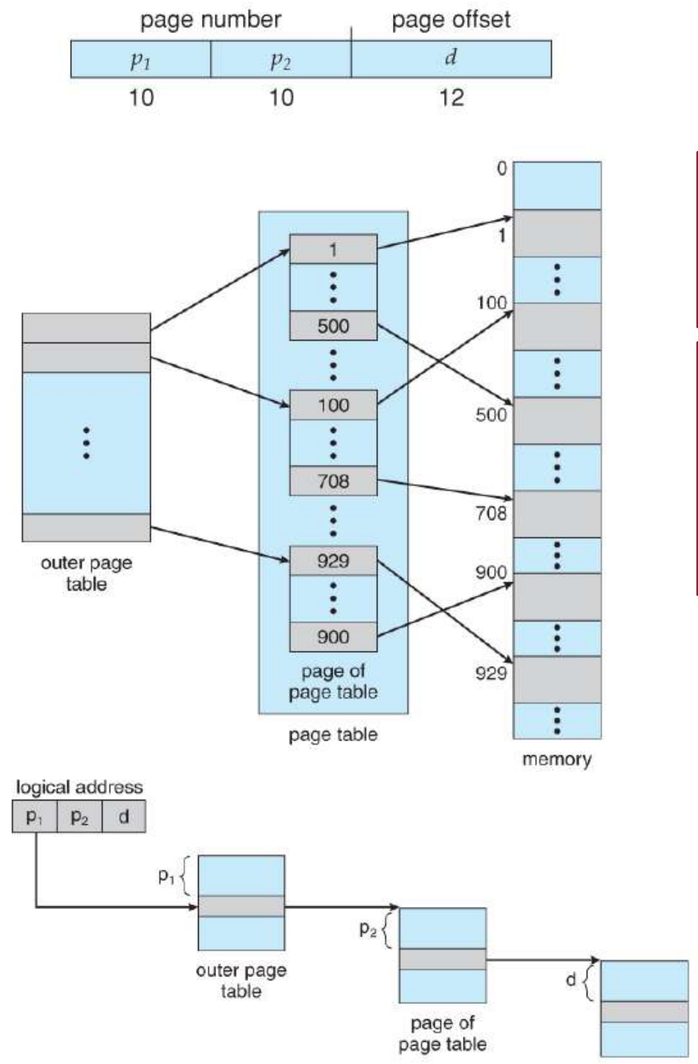

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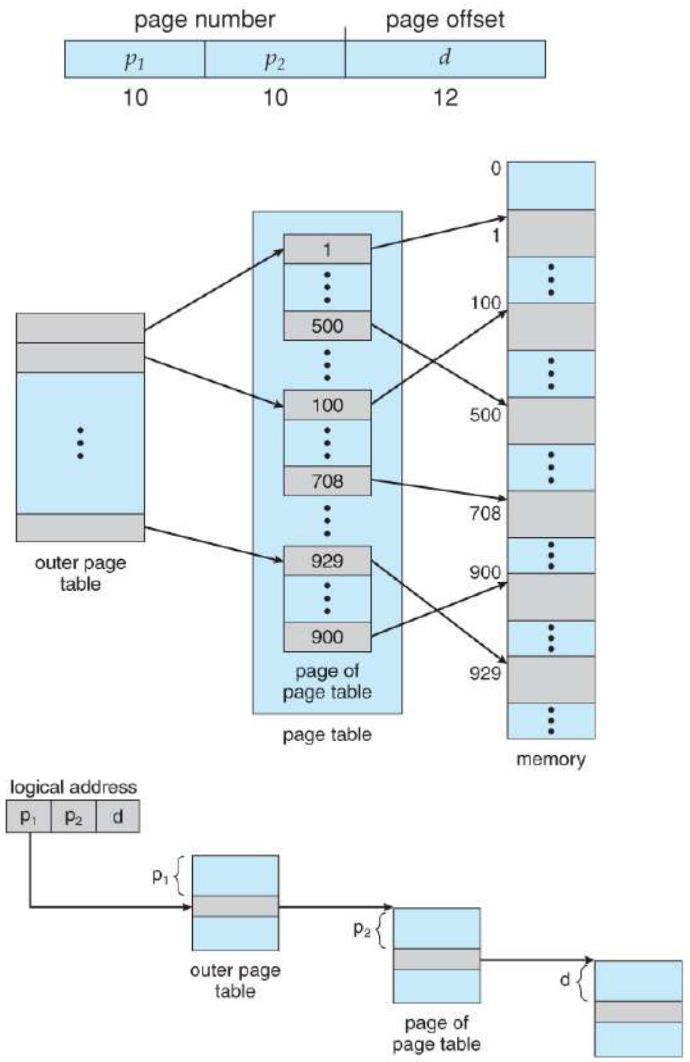

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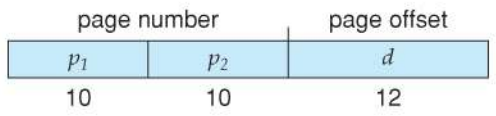

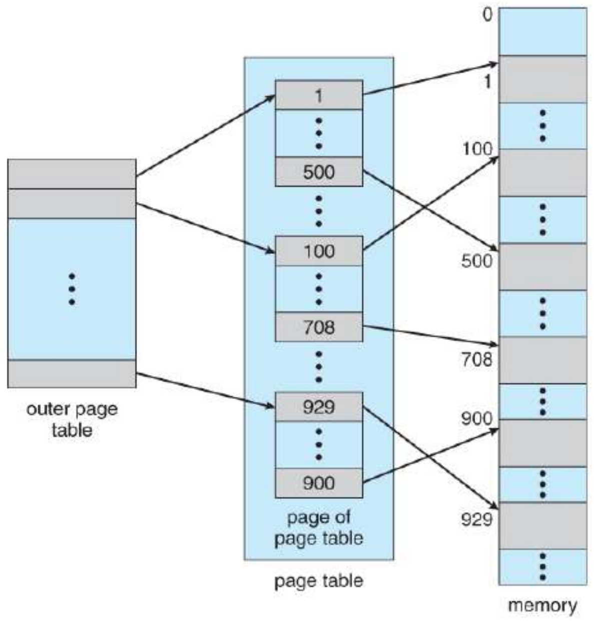

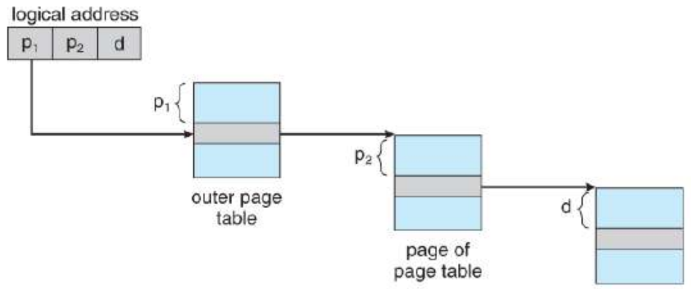

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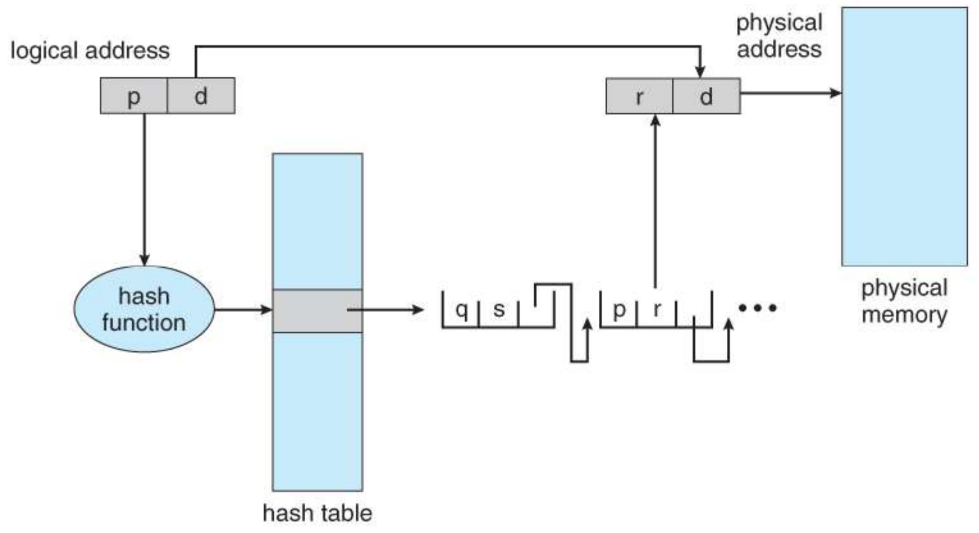
The remaining 12 bits of the 32-bit logical address are still the offset within the 4KiB frame

# Advanced Paging: Hashed Page Table



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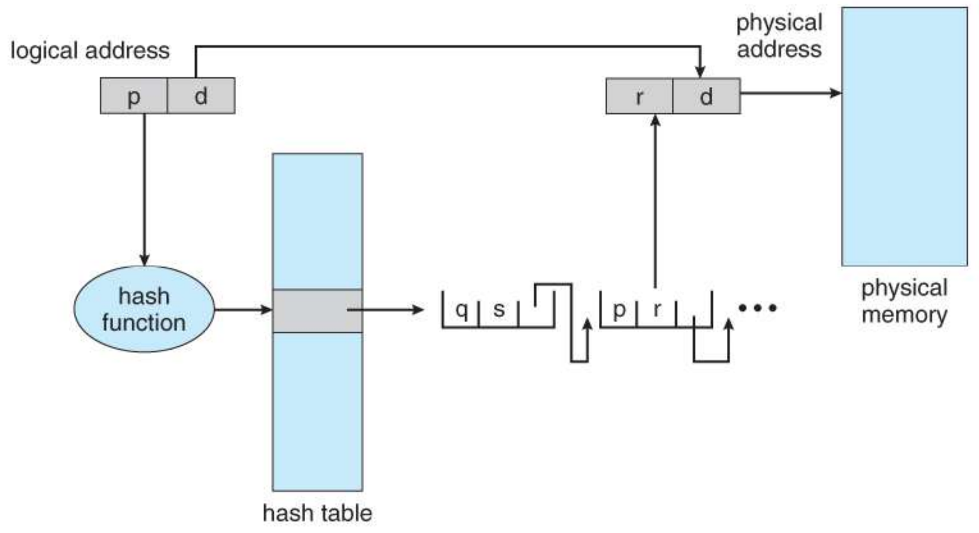

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Indexing via hash function rather than integers

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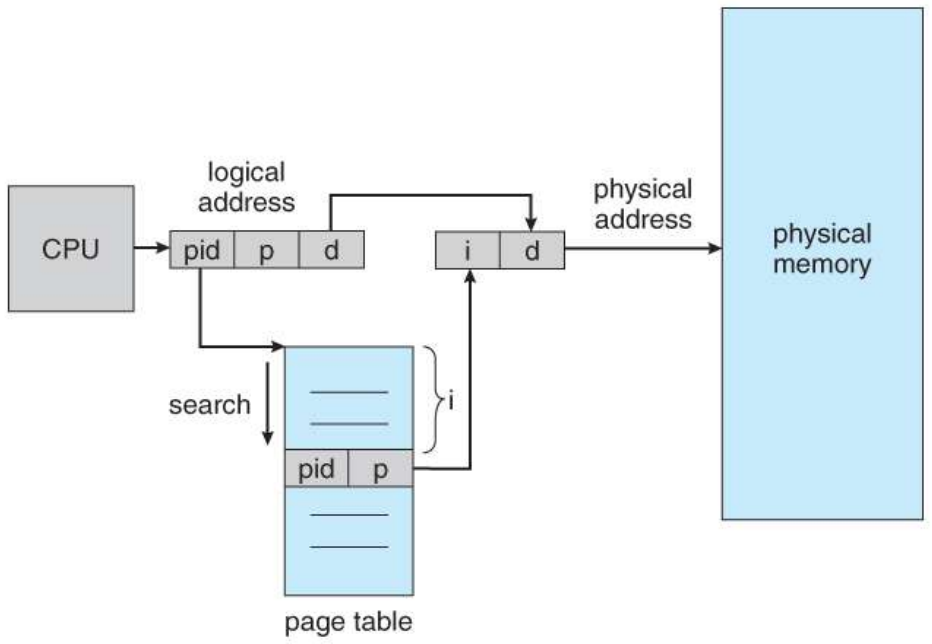
An inverted page table lists all of the frames currently loaded in memory, for all processes

Instead of a table listing all of the pages for a particular process



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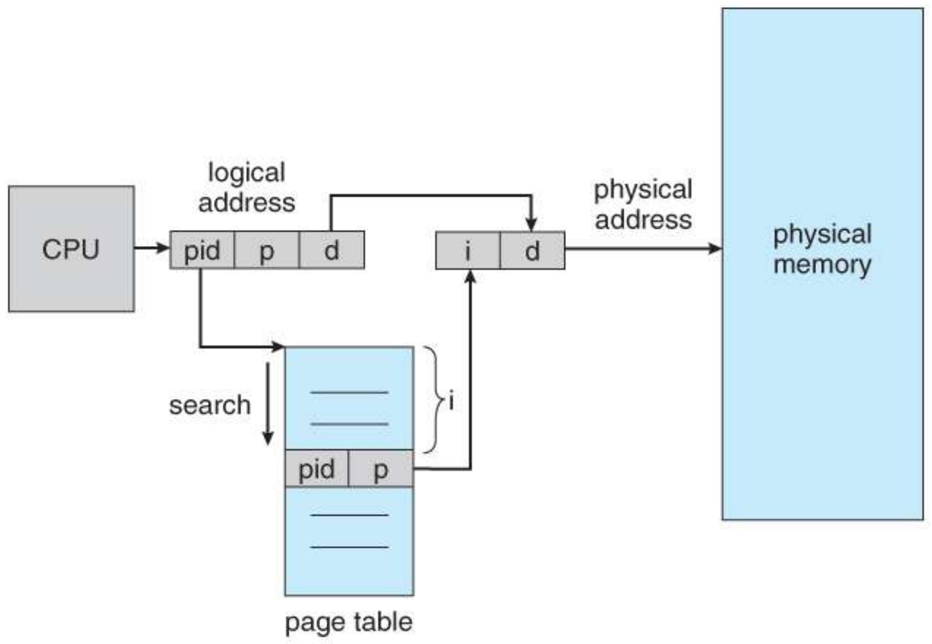

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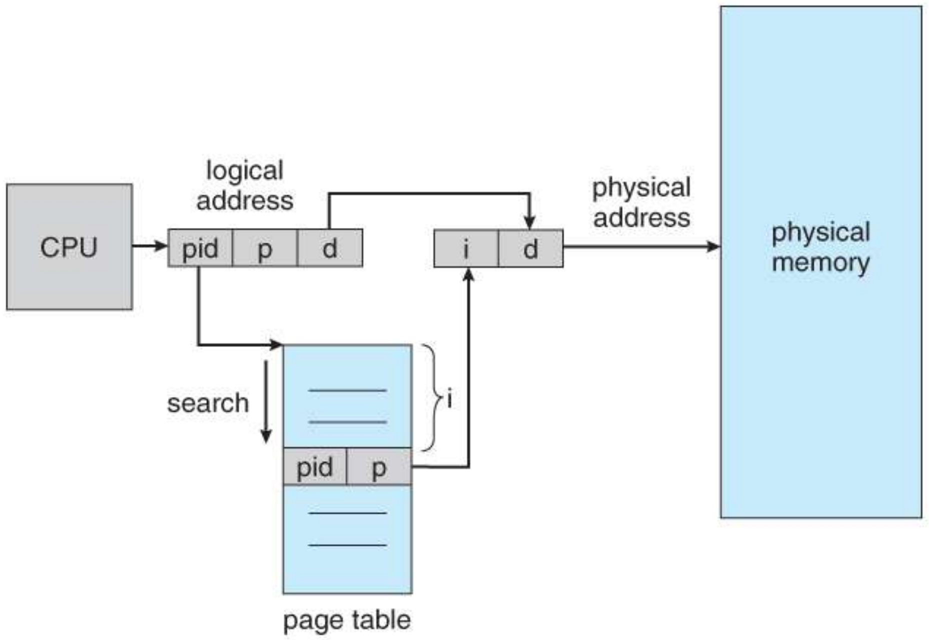

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Inverted page tables do not easily allow mapping multiple logical pages to a common physical frame (page sharing)

Each frame is mapped to exactly one process

## Summary

- **Relocation** using base and limit registers
  - Simple yet inflexible

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- Relocation using base and limit registers
    - Simple yet inflexible
- Segmentation
    - Compiler's logical view of memory presented to the OS
    - Segment tables tend to be small enough to be stored in registers
    - Contiguous memory allocation is expensive and complicated (first-fit, best-fit, or worst-fit)
    - Compaction is needed to solve external fragmentation

## Summary

- Paging
  - Simplifies memory allocation by relaxing contiguous assumption
  - Each logical page can be allocated to any physical frame
  - Page tables can be extremely large

# Summary

- Segmentation + Paging
  - Only need to allocate as many page table entries an needed
  - Sharing either at the segment or at the page level
  - Might increase internal fragmentation over pure paging
  - 2 lookups per memory reference are needed