

# Sistemi Operativi I

Corso di Laurea in Informatica  
2024-2025



**SAPIENZA**  
UNIVERSITÀ DI ROMA

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# A Quick Step Back: Segmentation

- Most users (programmers) do not think of their programs as existing in one continuous linear address space

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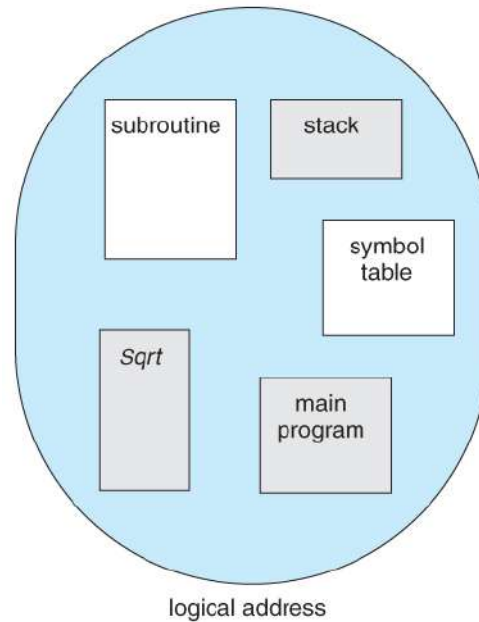
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- Memory segmentation supports this view by providing addresses with a **segment number** (mapped to a segment base address) and an **offset**

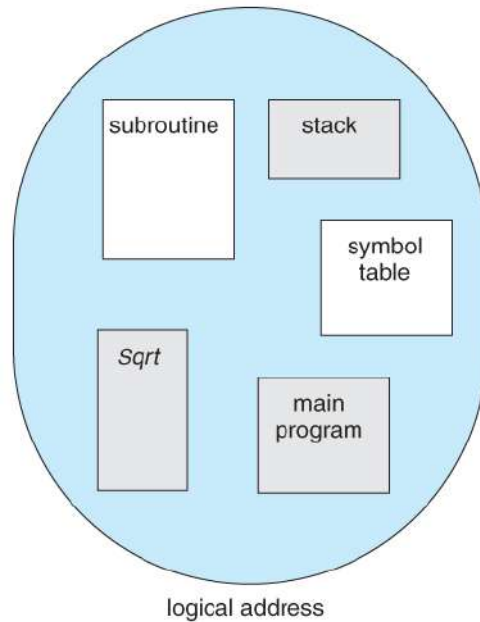
# Segmentation: Example

A C compiler generating 5 segments for the user code, library code, global (static) variables, the stack, and the heap



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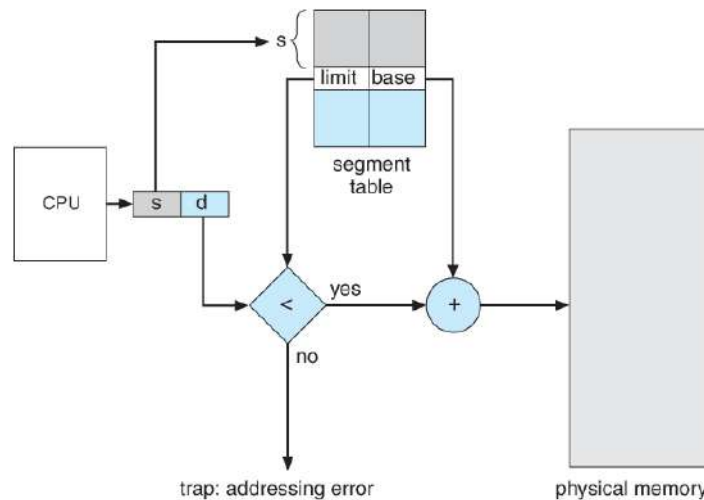
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The compiler generates addresses identifying segments and offset

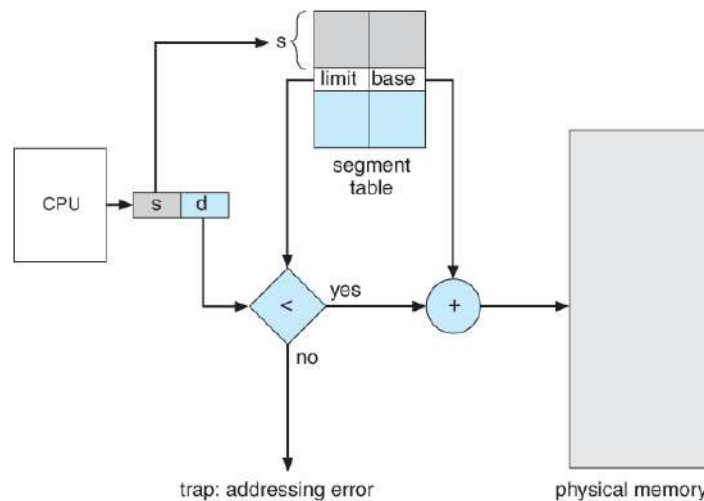
# Segmentation Hardware

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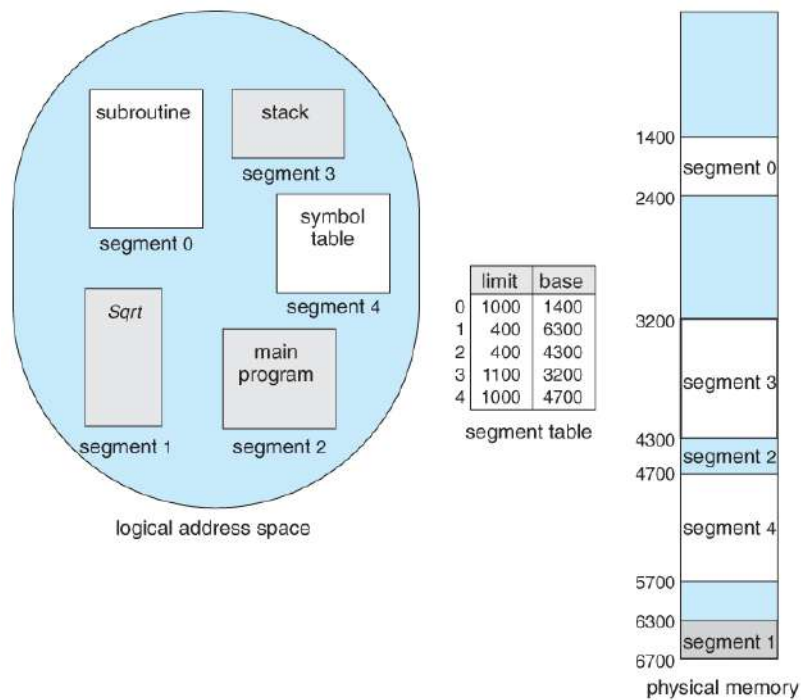


Note that we came back to the assumption that each segment is kept in **contiguous** memory and may be of different size...

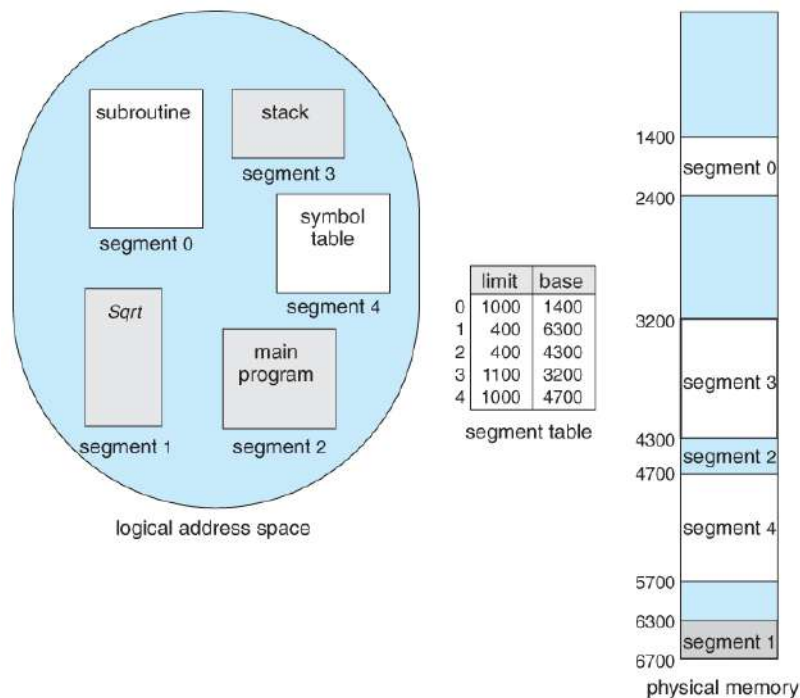


# Segment Table

Each entry contains a base address in memory, the length of the segment, plus additional protection information (e.g., sharing, read/write permissions)



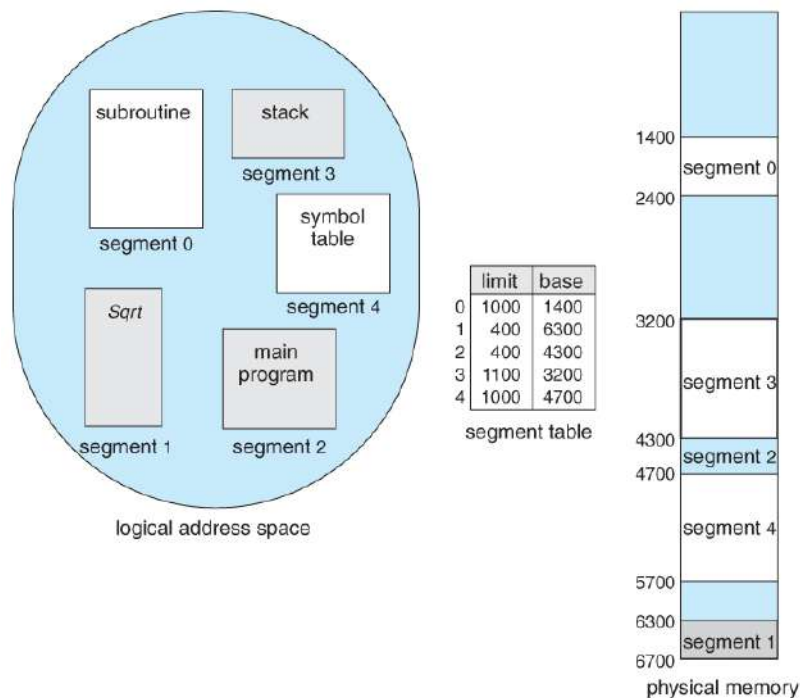
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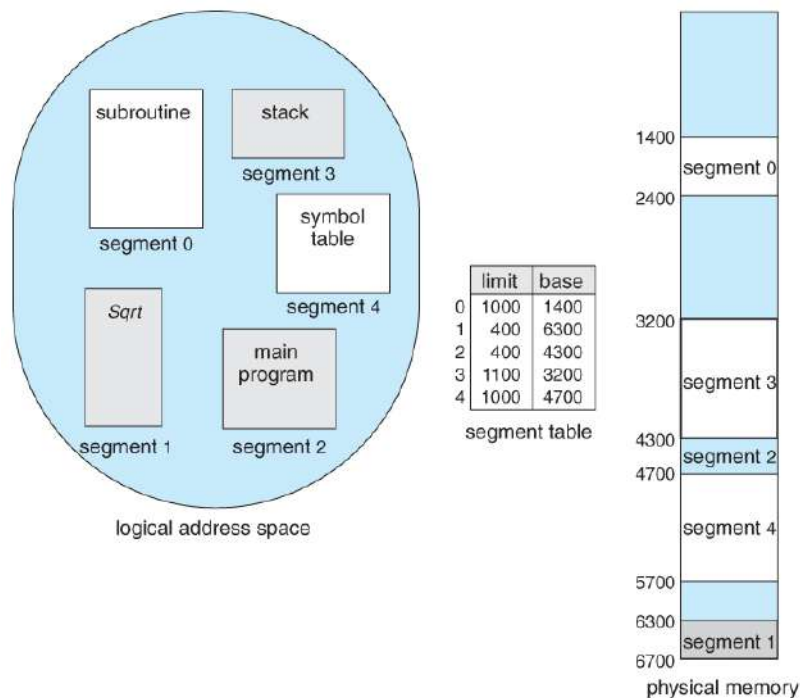


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**Segment Table**, instead, must store a very limited amount of segments per process (3÷5)

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- Additional HW (like TLB cache) might be needed if programs use many logical segments




# Combine Segmentation with Paging

Try to get the best of both world

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Segmentation  
ease of sharing

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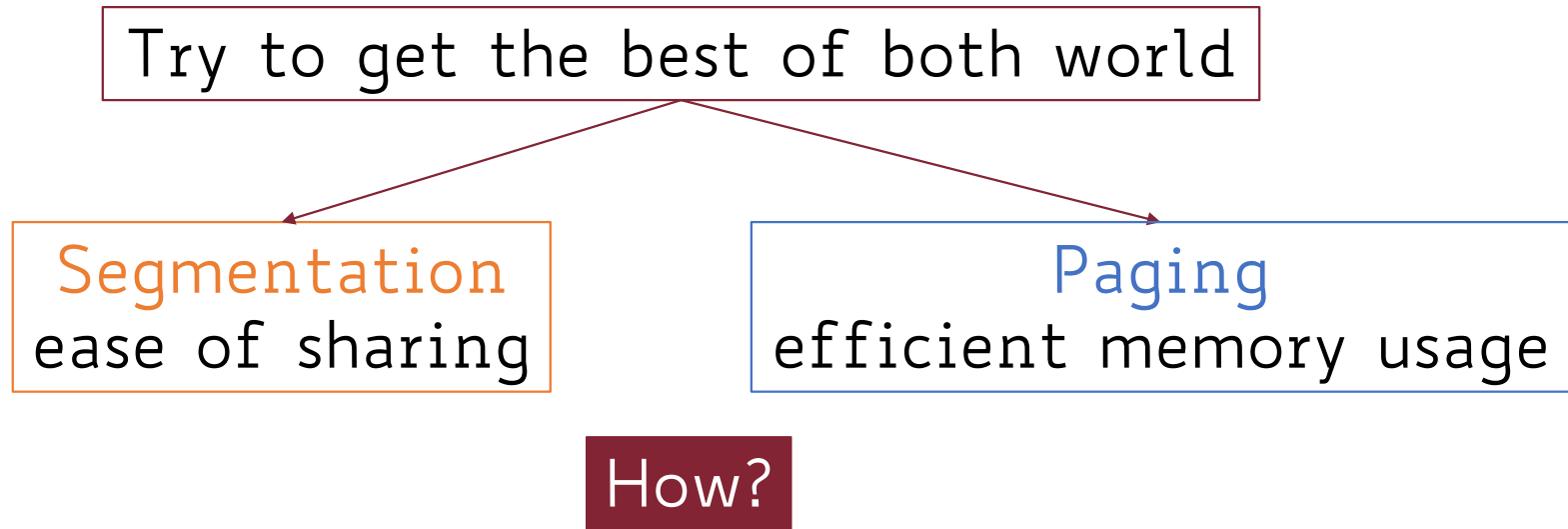
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How?

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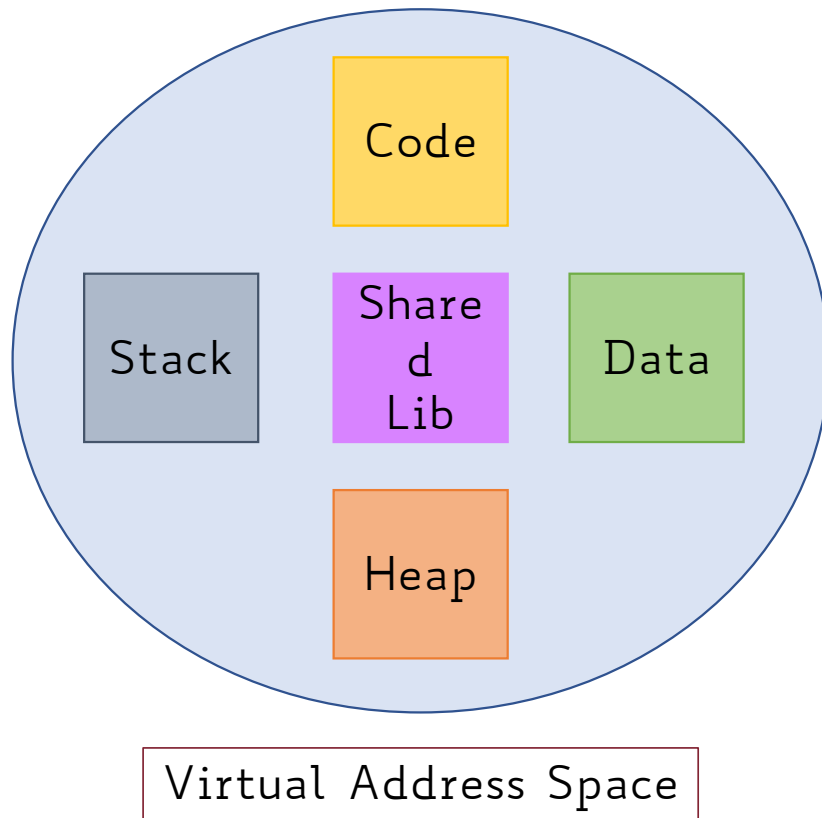
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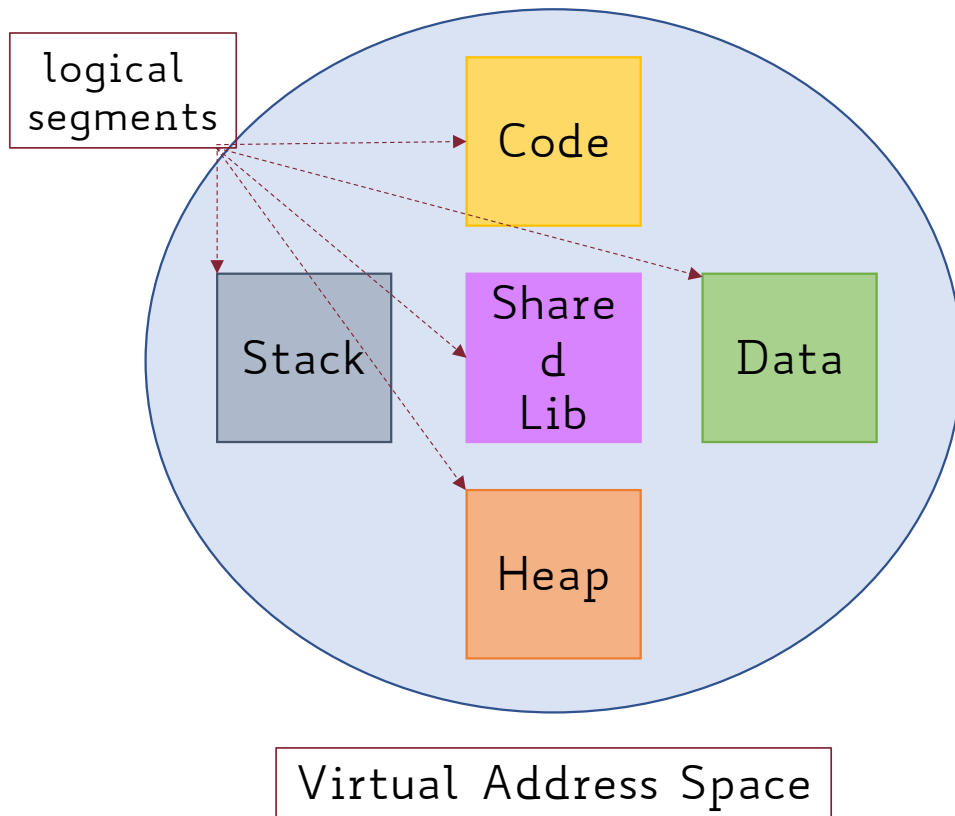


Map a logical segment onto multiple page frames

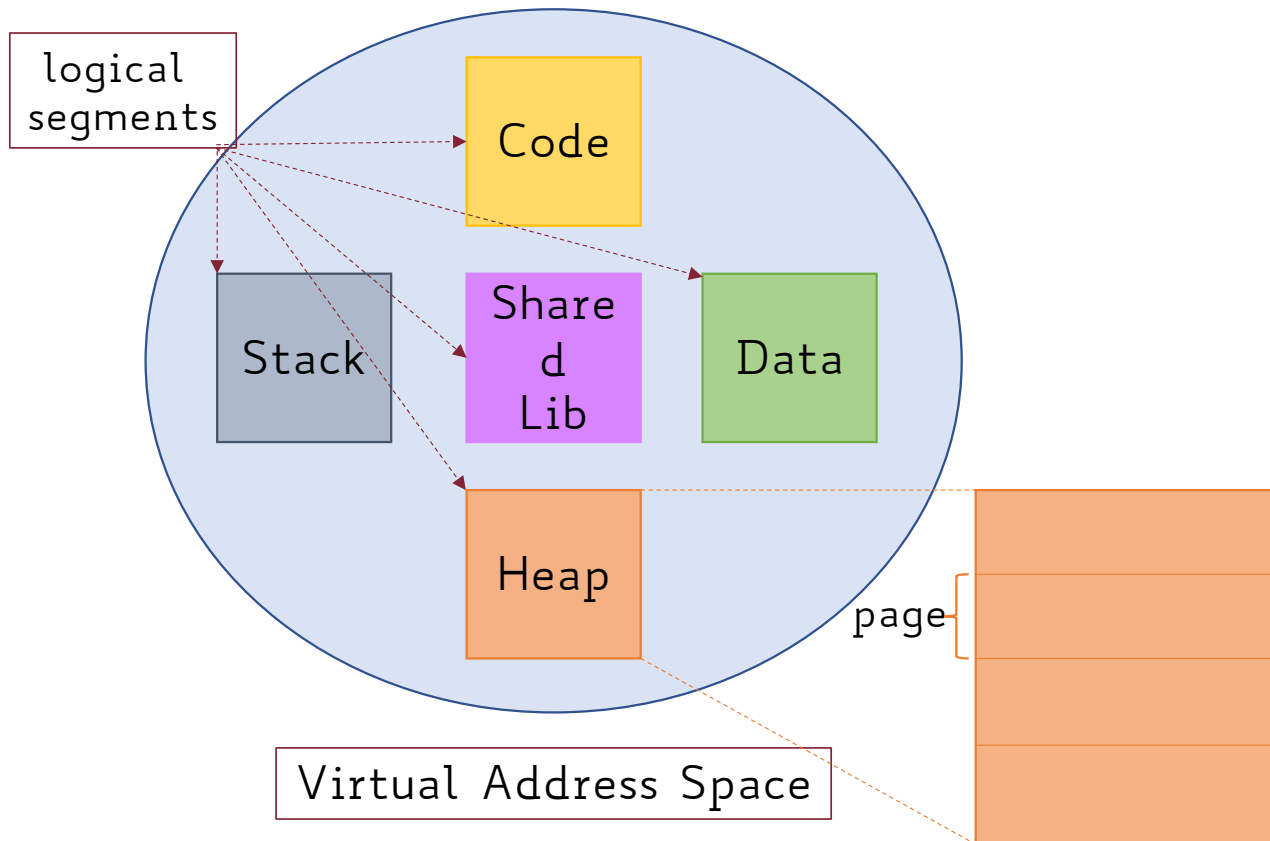
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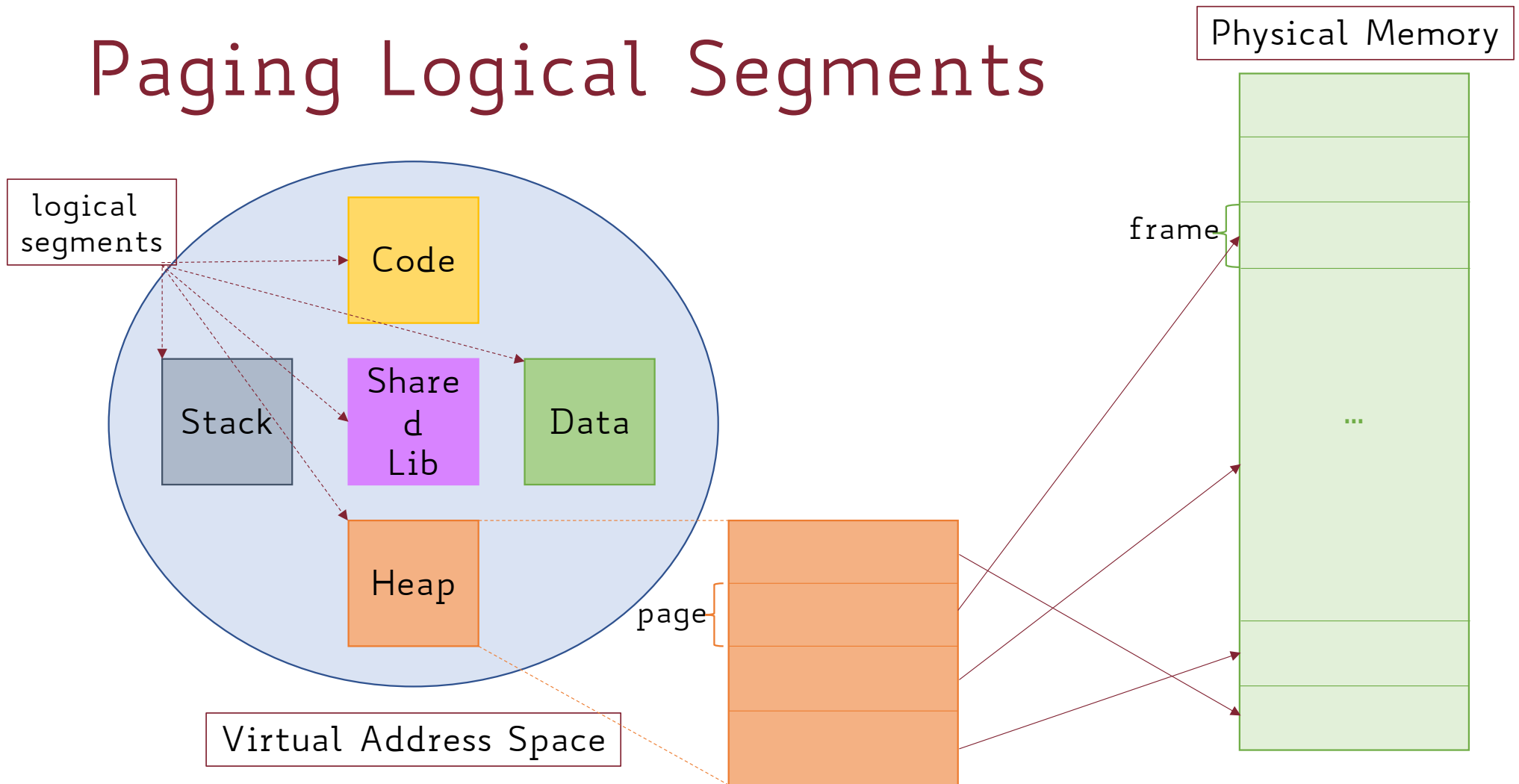
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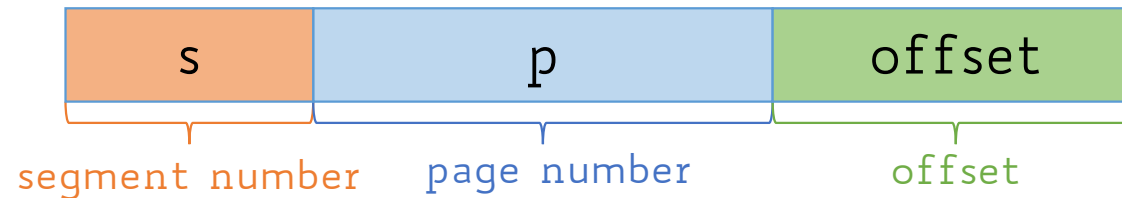


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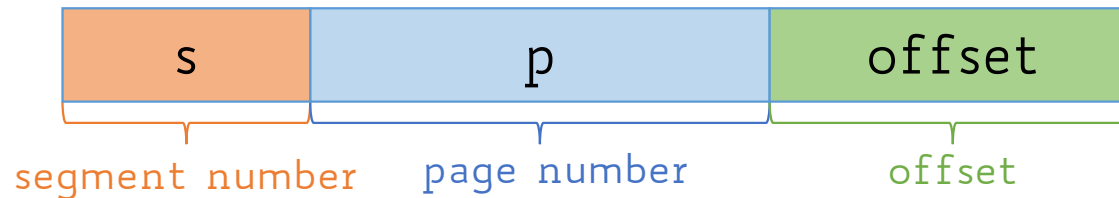
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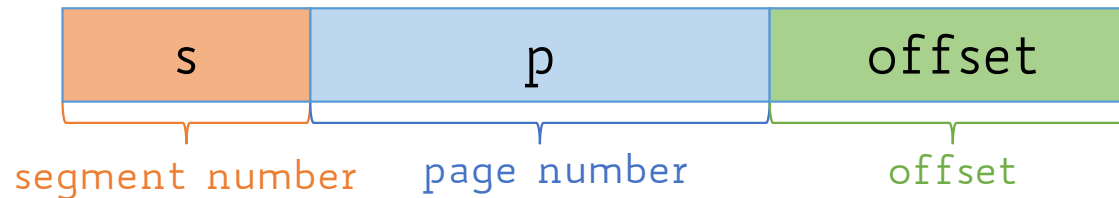
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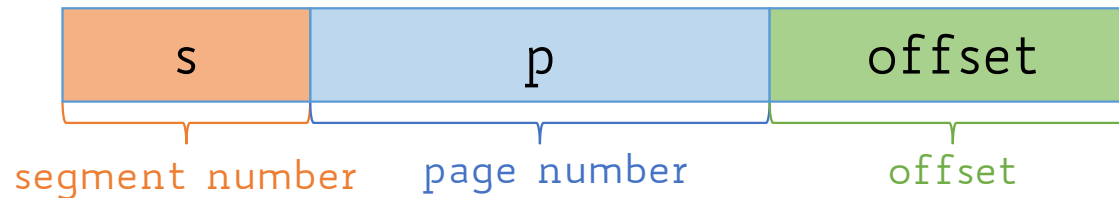


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- Check the page number + offset against the limit of the segment



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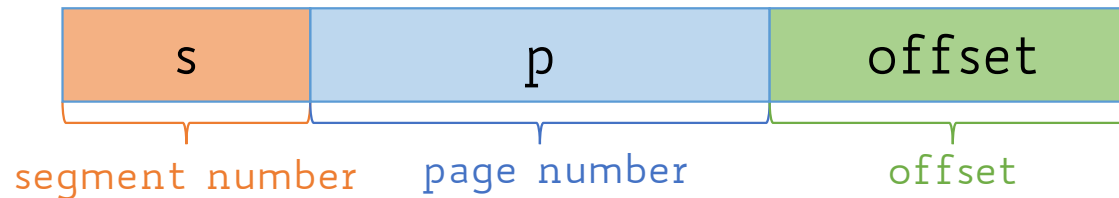
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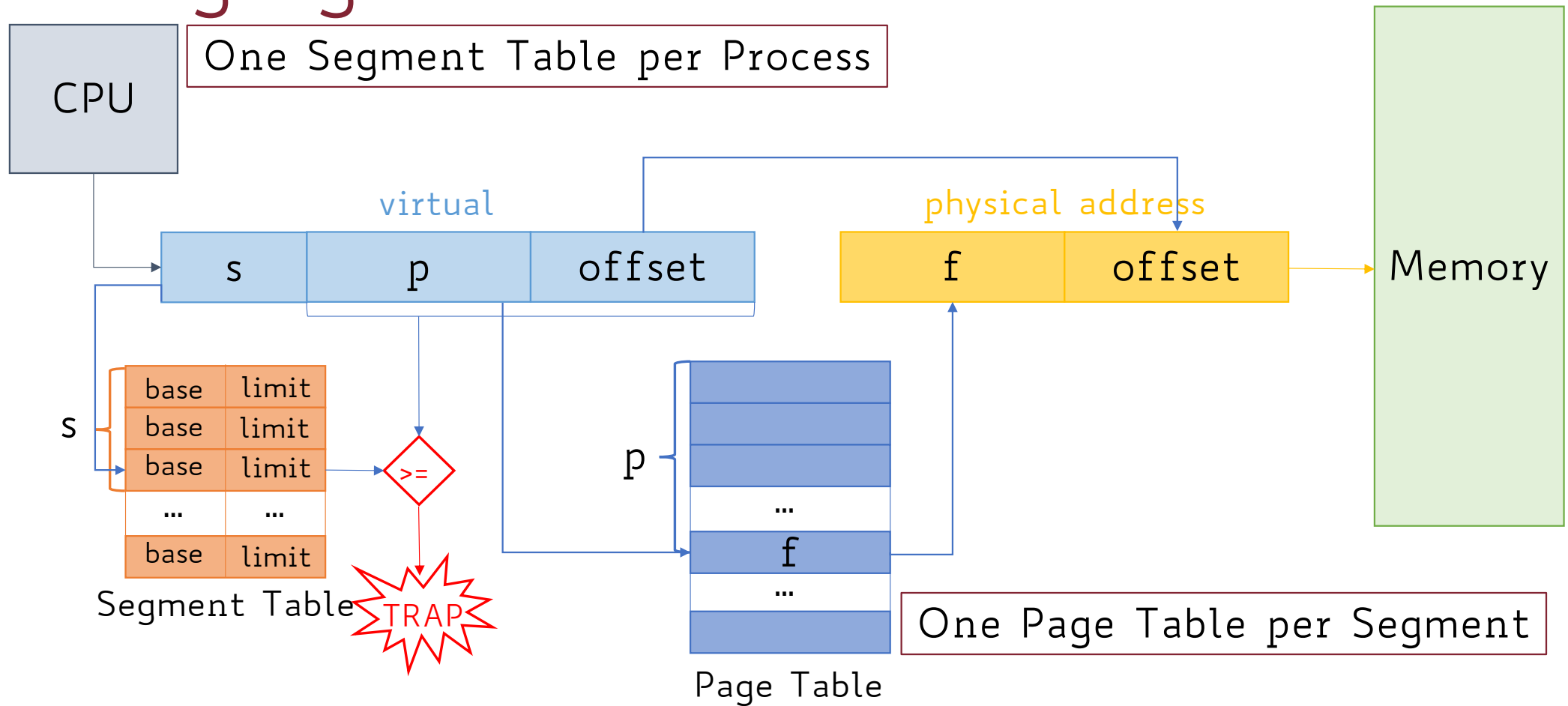
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Slower but more flexible



# Segmented Paging Hardware: Practical Example 3

Suppose a physical memory of 1024 addressable words (assuming 1 word = 1 byte)

Frame size is 64 words (i.e., 64 bytes)

Page table size (i.e., number of entries) is thus  $1024 \text{ bytes} / 64 \text{ bytes per frame} = 16$

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13 bits (virtual address) vs. 10 bits (physical address)

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- Even more flexible!

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- Slower context switches (why?)
- Slower address translation (why?)

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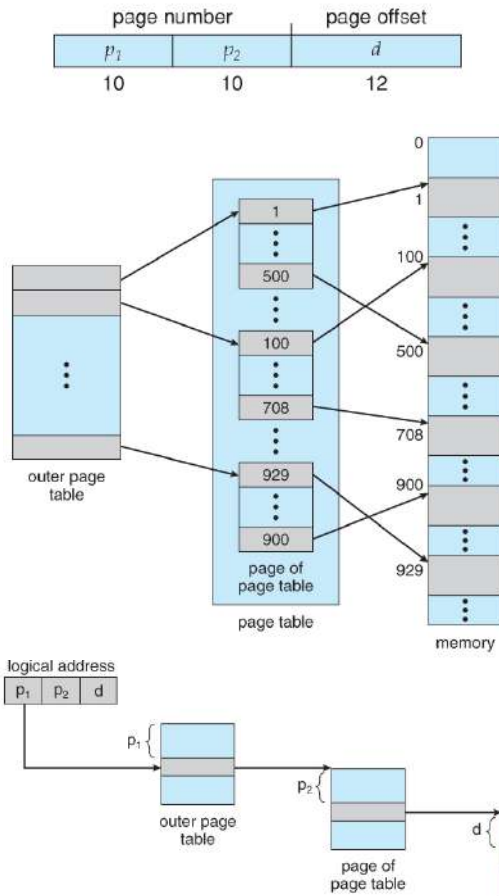
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**More advanced paging structures are needed!**

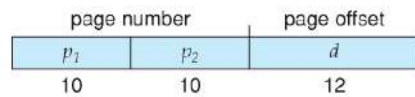
# Advanced Paging: Two-Tier Page Table

# Let's page the page table!



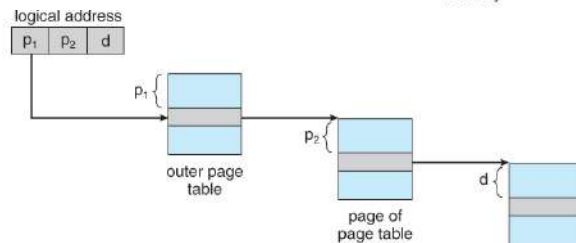
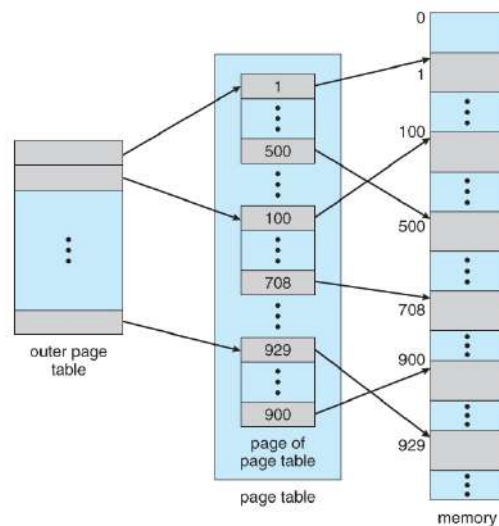


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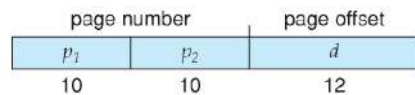


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20-bit page number broken into 2 10-bit page numbers



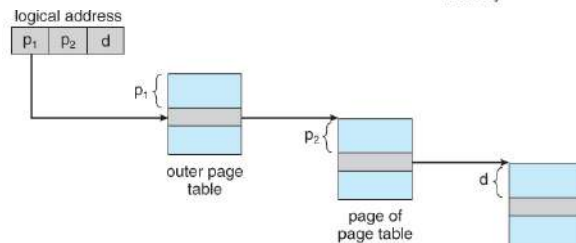
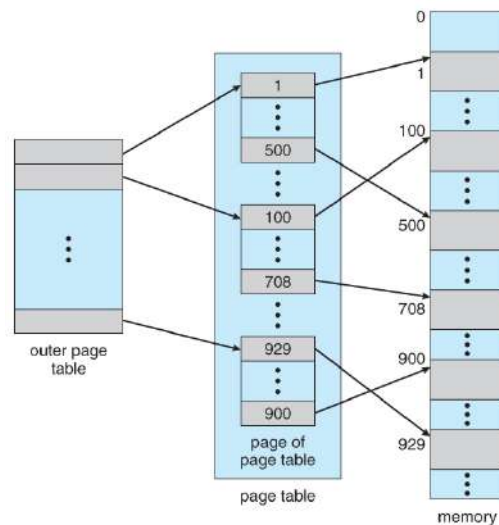
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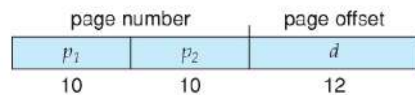
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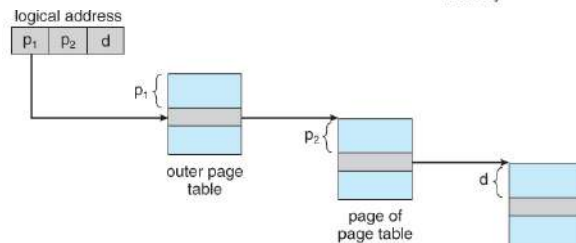
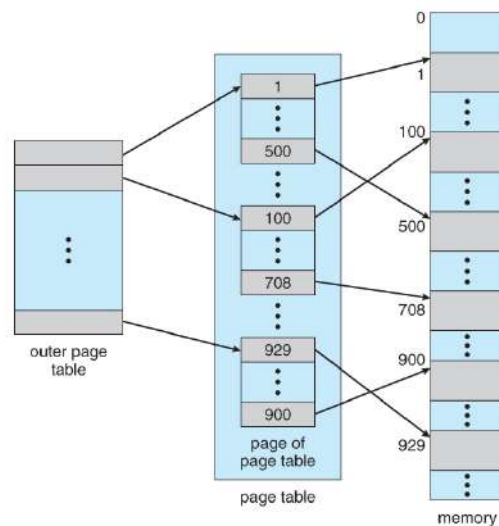
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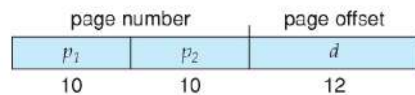


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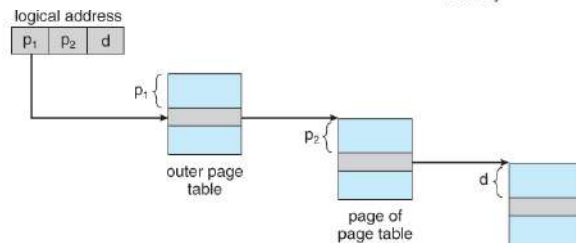
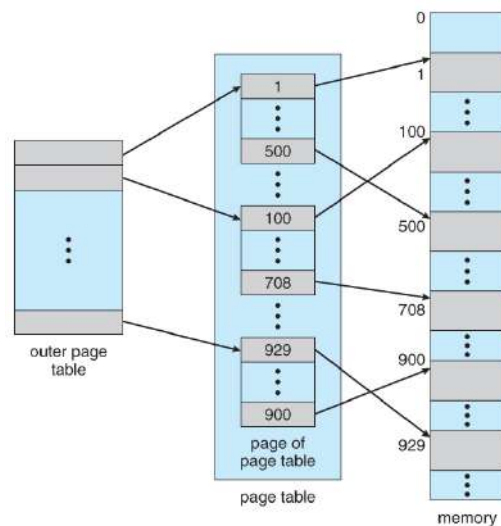
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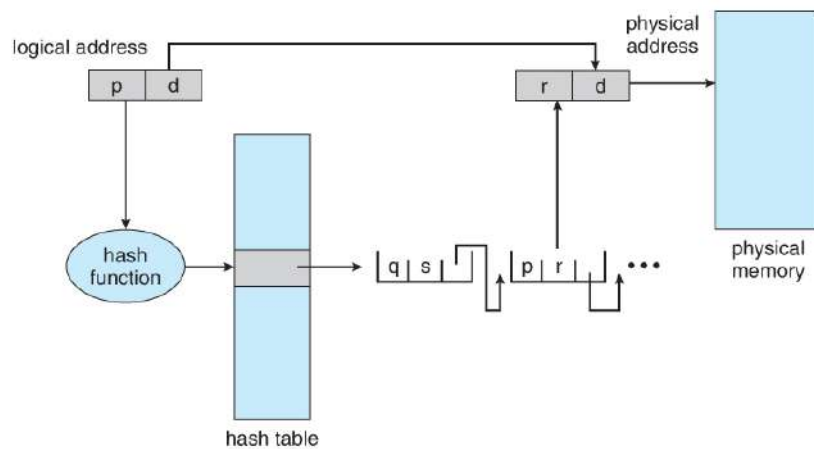
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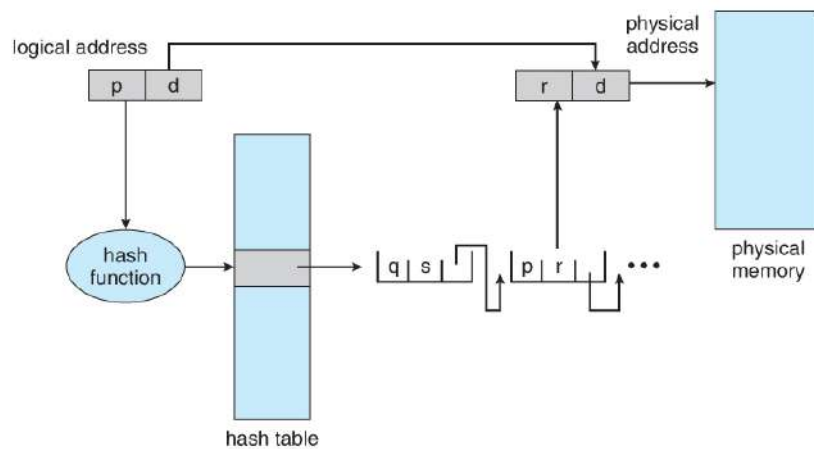
The remaining 12 bits of the 32-bit logical address are still the offset within the 4KiB frame

# Advanced Paging: Hashed Page Table



Use **hash tables** to store highly sparse page tables

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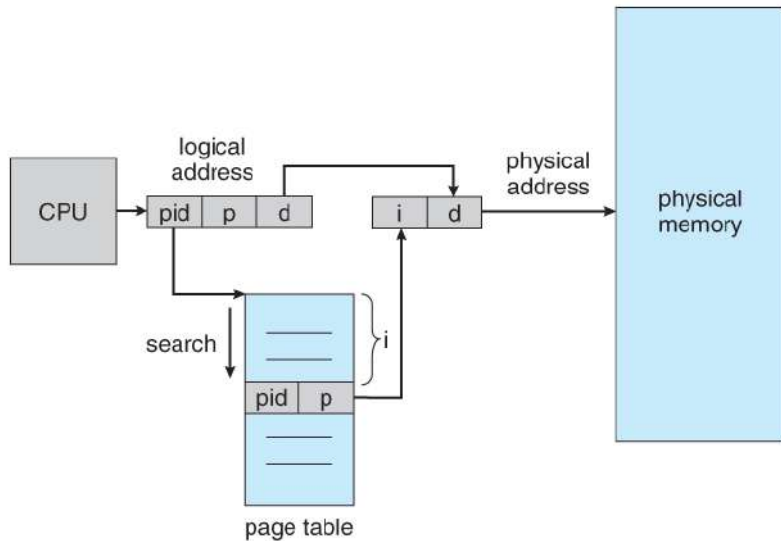
Use **hash tables** to store highly sparse page tables

Indexing via **hash function** rather than integers

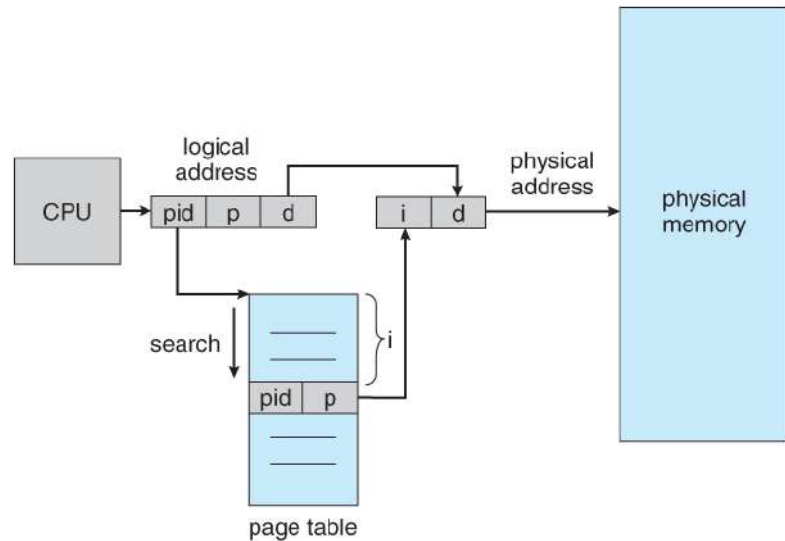
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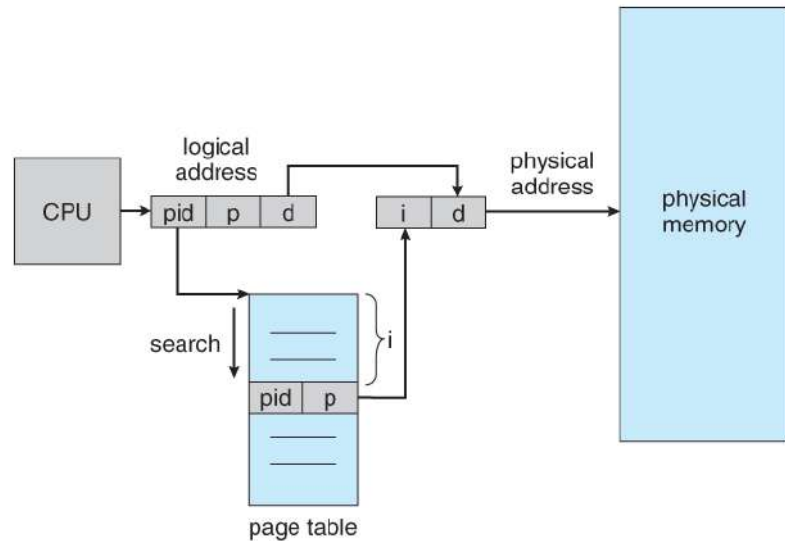
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Inverted page tables do not easily allow mapping multiple logical pages to a common physical frame (page sharing)

Each frame is mapped to exactly one process

# Summary

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- **Relocation** using base and limit registers
  - Simple yet inflexible
- **Segmentation**
  - Compiler's logical view of memory presented to the OS
  - Segment tables tend to be small enough to be stored in registers
  - Contiguous memory allocation is expensive and complicated (first-fit, best-fit, or worst-fit)
  - Compaction is needed to solve external fragmentation

# Summary

- **Paging**

- Simplifies memory allocation by relaxing contiguous assumption
- Each logical page can be allocated to any physical frame
- Page tables can be extremely large

# Summary

- **Segmentation + Paging**

- Only need to allocate as many page table entries as needed
- Sharing either at the segment or at the page level
- Might increase internal fragmentation over pure paging
- 2 lookups per memory reference are needed