# Sistemi Operativi I

Corso di Laurea in Informatica 2023-2024



#### Gabriele Tolomei

Dipartimento di Informatica Sapienza Università di Roma tolomei@di.uniroma1.it

### Paging + Segmentation

- Paging (OS' view of memory)
  - Divide memory into fixed-size pages and map them to physical frames
- Segmentation (compiler's view of memory)
  - Divide process into logical segments (e.g., code, data, stack, heap)
- Combine paging with segmentation
  - Segmented Paging

# Paging + Segmentation

- Paging (OS' view of memory)
  - Divide memory into fixed-size pages and map them to physical frames
- Segmentation (compiler's view of memory)
  - Divide process into logical segments (e.g., code, data, stack, heap)
- Combine paging with segmentation
  - Segmented Paging

So far, the entire virtual address space of a process was assumed to fit and be all in memory

• In practice, most real processes do not need all their pages loaded in memory, or at least not all at once, e.g.,:

- In practice, most real processes do not need all their pages loaded in memory, or at least not all at once, e.g.,:
  - Error handling code is not needed unless that specific error occurs, some of which are quite rare

- In practice, most real processes do not need all their pages loaded in memory, or at least not all at once, e.g.,:
  - Error handling code is not needed unless that specific error occurs, some of which are quite rare
  - Arrays are often over-sized for worst-case scenarios, and only a small fraction of the arrays is actually used in practice

- In practice, most real processes do not need all their pages loaded in memory, or at least not all at once, e.g.,:
  - Error handling code is not needed unless that specific error occurs, some of which are quite rare
  - Arrays are often over-sized for worst-case scenarios, and only a small fraction of the arrays is actually used in practice
  - Some features of certain programs are rarely used

- In practice, most real processes do not need all their pages loaded in memory, or at least not all at once, e.g.,:
  - Error handling code is not needed unless that specific error occurs, some of which are quite rare
  - Arrays are often over-sized for worst-case scenarios, and only a small fraction of the arrays is actually used in practice
  - Some features of certain programs are rarely used

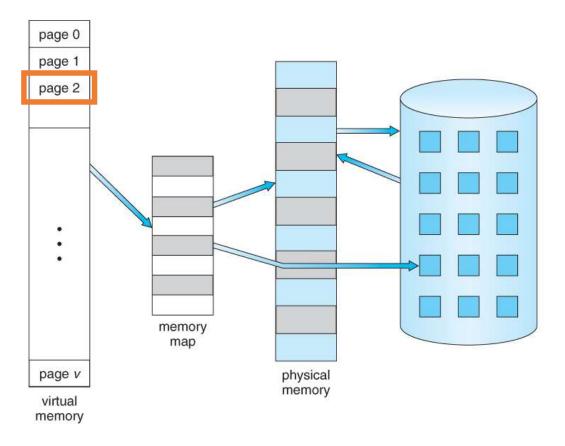
Virtual Memory uses backing storage (i.e., disk) to store unused pages and give the illusion of infinite virtual address space

• The ability to load only the portions of processes that are actually needed (and only when needed) from disk has several benefits:

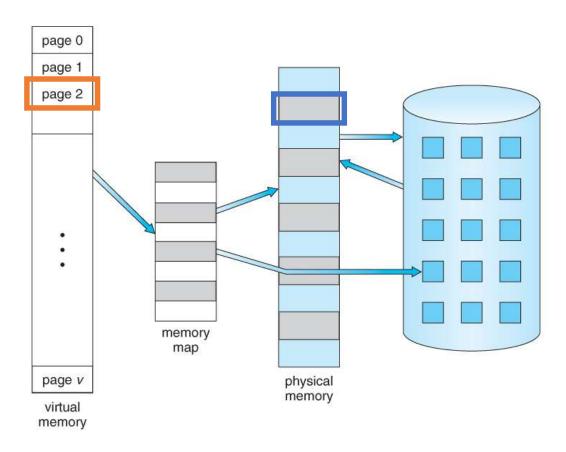
- The ability to load only the portions of processes that are actually needed (and only when needed) from disk has several benefits:
  - Programs could be written for a much larger address space than physically exists on the computer

- The ability to load only the portions of processes that are actually needed (and only when needed) from disk has several benefits:
  - Programs could be written for a much larger address space than physically exists on the computer
  - More memory is left for other programs, improving CPU utilization

- The ability to load only the portions of processes that are actually needed (and only when needed) from disk has several benefits:
  - Programs could be written for a much larger address space than physically exists on the computer
  - More memory is left for other programs, improving CPU utilization
  - Less I/O is needed for swapping processes in and out of memory, speeding things up

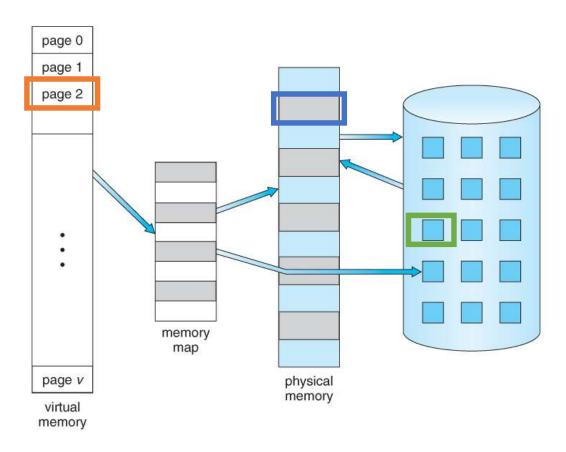


At any given time, each page can be:



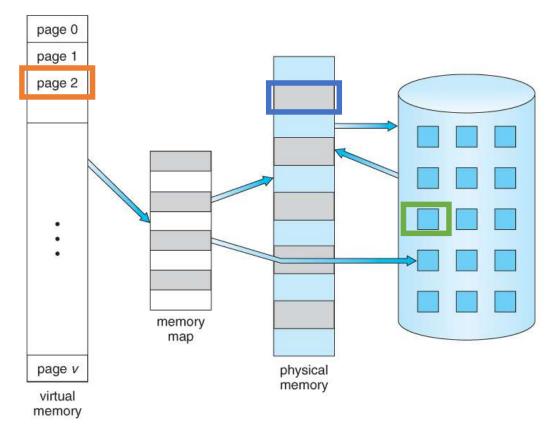
At any given time, each page can be:

in memory (physical frame)



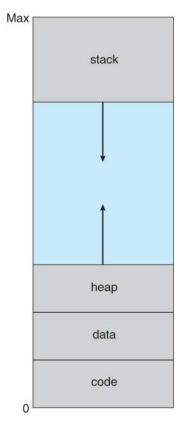
At any given time, each page can be: in memory (physical frame) on backing store (disk)

virtual memory can be much larger than physical memory



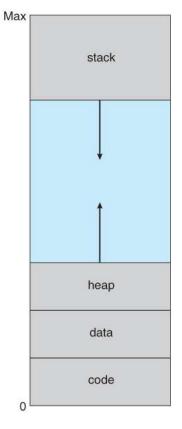
At any given time, each page can be: in memory (physical frame) on backing store (disk)

# The Sparseness of Virtual Address Space



Typically, virtual address space is highly sparse

# The Sparseness of Virtual Address Space



Typically, virtual address space is highly sparse

A lot of virtual memory addresses remain unreferenced

• Use the memory as a cache for the disk

- Use the memory as a cache for the disk
- The page table must also indicate if the page is on disk or in memory (just using a single invalid bit)

- Use the memory as a cache for the disk
- The page table must also indicate if the page is on disk or in memory (just using a single invalid bit)
- Once the page is loaded from disk to memory, the OS updates the corresponding entry of the page table along with the valid bit

• Remember: access to disk is extremely slower than access to memory

- Remember: access to disk is extremely slower than access to memory
- Therefore, memory accesses must reference pages that are in memory with high probability

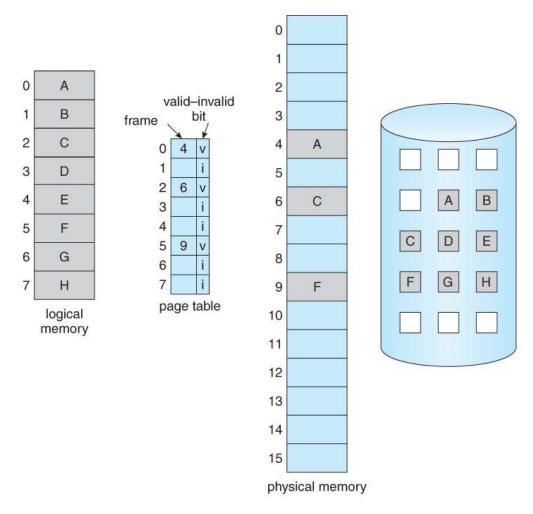
• The 90÷10 rule claims that on a particular time frame, most of the memory references made by a process is around a small "area"

- The 90÷10 rule claims that on a particular time frame, most of the memory references made by a process is around a small "area"
- We call this area as the working set of the process

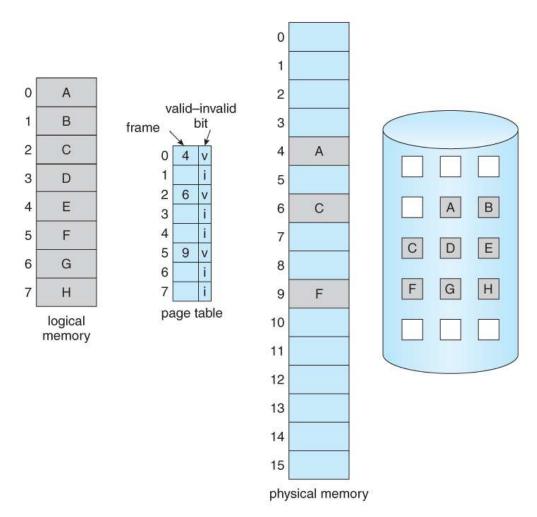
- The 90÷10 rule claims that on a particular time frame, most of the memory references made by a process is around a small "area"
- We call this area as the working set of the process
- Since the working set is fairly small compared to the whole virtual address space, it will likely fit in memory

• Of course, during the lifetime of a process its working set may change (i.e., a process may eventually refer *all* of its virtual address space)

- Of course, during the lifetime of a process its working set may change (i.e., a process may eventually refer *all* of its virtual address space)
- But in a reasonably small time frame, the working set stays "the same"

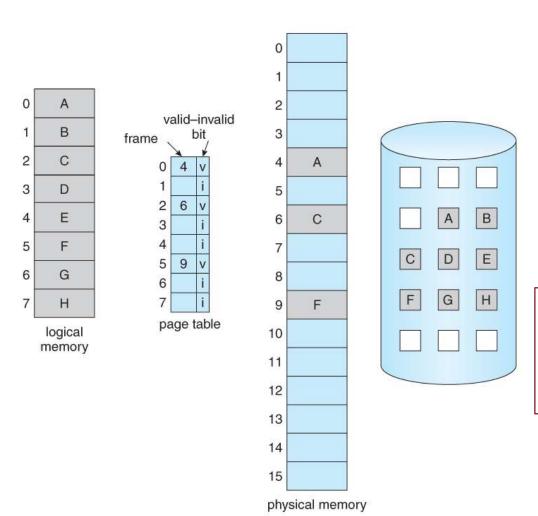


At each logical memory reference, a page table lookup is performed as usual



At each logical memory reference, a page table lookup is performed as usual

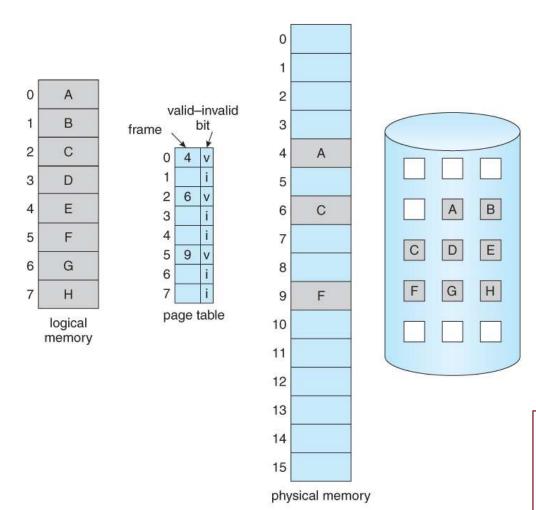
In the page table, the validinvalid bit is checked for the corresponding entry



At each logical memory reference, a page table lookup is performed as usual

In the page table, the validinvalid bit is checked for the corresponding entry

If the bit is set to 1 it means the page entry is valid (i.e., the requested page is in memory)

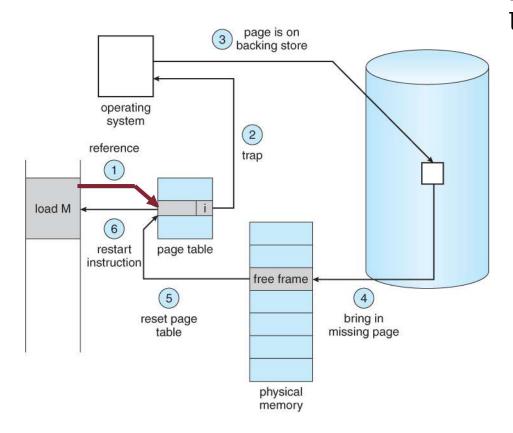


At each logical memory reference, a page table lookup is performed as usual

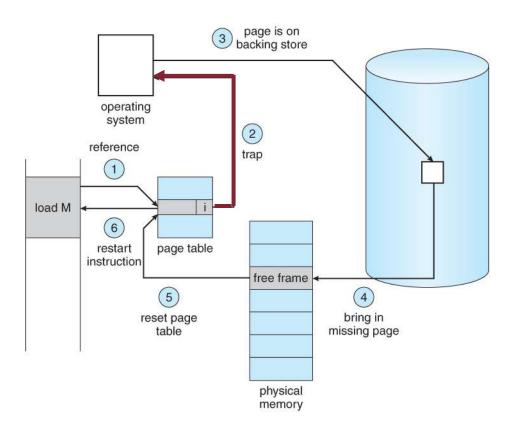
In the page table, the validinvalid bit is checked for the corresponding entry

If the bit is set to 1 it means the page entry is valid (i.e., the requested page is in memory)

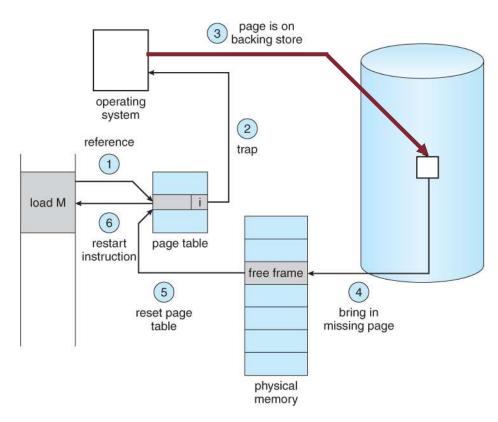
Otherwise, a page fault trap occurs, and the page has to be loaded (i.e., fetched) from disk



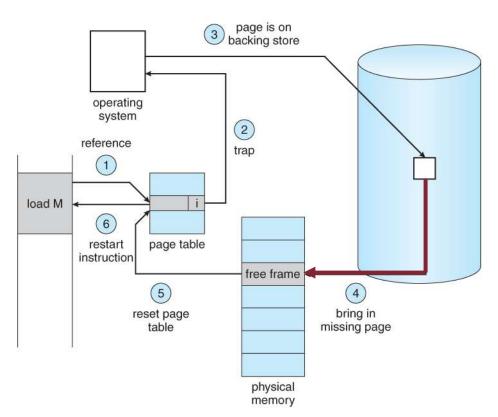
1. The memory address is first checked, to see if it is legitimate



- 1. The memory address is first checked, to see if it is legitimate
- 2. If the address is legitimate the page must be fetched from disk

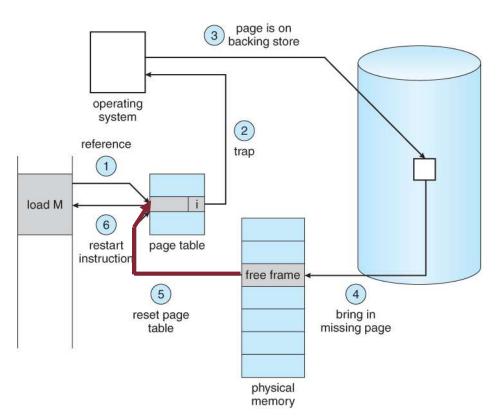


- 1. The memory address is first checked, to see if it is legitimate
- 2. If the address is legitimate the page must be fetched from disk
- 3. A free frame is located, possibly from a free-frame list (the OS might need to pick a frame to unload if all memory is full)



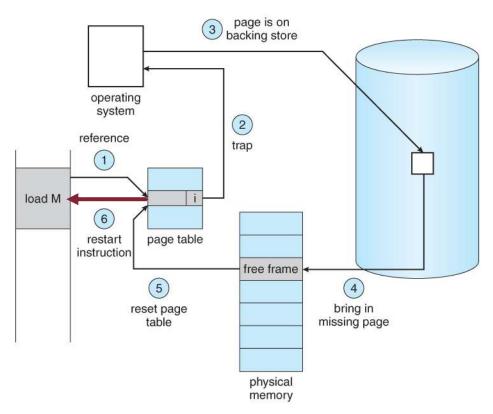
- 1. The memory address is first checked, to see if it is legitimate
- 2. If the address is legitimate the page must be fetched from disk
- 3. A free frame is located, possibly from a free-frame list (the OS might need to pick a frame to unload if all memory is full)
- 4. A disk operation is scheduled to bring in the necessary page from disk (this will block the process on an I/O wait, allowing some other process to run)

## Page Fault Handling



- 1. The memory address is first checked, to see if it is legitimate
- 2. If the address is legitimate the page must be fetched from disk
- 3. A free frame is located, possibly from a free-frame list (the OS might need to pick a frame to unload if all memory is full)
- 4. A disk operation is scheduled to bring in the necessary page from disk (this will block the process on an I/O wait, allowing some other process to run)
- 5. When the I/O operation is complete, the process's page table is updated with the new frame number, and the bit is set to valid

## Page Fault Handling



- 1. The memory address is first checked, to see if it is legitimate
- 2. If the address is legitimate the page must be fetched from disk
- 3. A free frame is located, possibly from a free-frame list (the OS might need to pick a frame to unload if all memory is full)
- 4. A disk operation is scheduled to bring in the necessary page from disk (this will block the process on an I/O wait, allowing some other process to run)
- 5. When the I/O operation is complete, the process's page table is updated with the new frame number, and the bit is set to valid
- 6. The current process gets interrupted and the instruction that caused the page fault must be restarted from the beginning

 The TLB also uses the valid bit to indicate the fact that the page is in main memory

- The TLB also uses the valid bit to indicate the fact that the page is in main memory
- If we get a TLB hit but the frame is not actually in main memory, we have to go fetch the page from disk anyway!

- The TLB also uses the valid bit to indicate the fact that the page is in main memory
- If we get a TLB hit but the frame is not actually in main memory, we have to go fetch the page from disk anyway!
- TLB hit means the requested page entry is in the cache and the referenced frame is also in memory

• If the requested page is not in the cache (TLB miss) but it is in memory:

- If the requested page is not in the cache (TLB miss) but it is in memory:
  - The OS picks a TLB entry to replace and fills it with the new entry

- If the requested page is not in the cache (TLB miss) but it is in memory:
  - The OS picks a TLB entry to replace and fills it with the new entry

- If the requested page is not in the cache (TLB miss) and it is not even in memory (i.e., it is sitting on disk):
  - The OS picks a TLB entry to replace and fills it with the new entry as follows
    - invalidates the TLB entry
    - performs page fault trap operations
    - updates the TLB entry
    - restarts the faulting instruction

## Page Fault Handling: Faulty Address

 How does the OS figure out which page generated the fault?

## Page Fault Handling: Faulty Address

- How does the OS figure out which page generated the fault?
- Architecture-dependent:
  - x86: hardware saves the virtual address that caused the fault (CR2 register)
  - On some platforms, OS gets only address of faulting instruction, must simulate the instruction and try every address to find the one that generated the fault

 Transparently restarting process execution after a page fault is tricky, since the fault may have occurred in the middle of an instruction

- Transparently restarting process execution after a page fault is tricky, since the fault may have occurred in the middle of an instruction
- To restart (from scratch) a faulty instruction the OS needs hardware support for saving:
  - The faulting instruction
  - The CPU state

• idempotent vs. non-idempotent instructions

- idempotent vs. non-idempotent instructions

- idempotent vs. non-idempotent instructions
- non-idempotent → much more difficult to restart
  - MOV [%R1], +(%R2)  $\rightarrow$  increment the value of R2 and store it to memory address in R1
  - What if memory address [%R1] causes the page fault?
  - Cannot naively redo the instruction from scratch, otherwise
     R2 gets incremented twice

- Even harder when using instructions that are not easily undoable
  - E.g., instructions that are used to move a block of memory at once
  - The block may span multiple pages: some of them can be in memory while some others not
  - Pages that are in memory can be changed meanwhile a page fault occurs

- Even harder when using instructions that are not easily undoable
  - E.g., instructions that are used to move a block of memory at once
  - The block may span multiple pages: some of them can be in memory while some others not
  - Pages that are in memory can be changed meanwhile a page fault occurs

How to unwind those complicated side-effects?

- Even harder when using instructions that are not easily undoable
  - E.g., instructions that are used to move a block of memory at once
  - The block may span multiple pages: some of them can be in memory while some others not
  - Pages that are in memory can be changed meanwhile a page fault occurs

Ensure all the addresses within the block to be moved are in memory before executing the instruction

- Theoretically, a page fault may occur at each process instruction
  - A process may reference addresses belonging to different page at each step

- Theoretically, a page fault may occur at each process instruction
  - A process may reference addresses belonging to different page at each step
- Luckily, processes usually exhibit so-called locality of reference

- Theoretically, a page fault may occur at each process instruction
  - A process may reference addresses belonging to different page at each step
- Luckily, processes usually exhibit so-called locality of reference
  - temporal → if a process accesses an item in memory, it will tend to reference the same item again soon

- Theoretically, a page fault may occur at each process instruction
  - A process may reference addresses belonging to different page at each step
- Luckily, processes usually exhibit so-called locality of reference
  - temporal → if a process accesses an item in memory, it will tend to reference the same item again soon
- spatial → if a process accesses an item in memory, it will 12/12/23 tend to reference a close item again soon

 $t_{MA}$  = physical memory access time  $t_{FAULT}$  = time to handle a page fault  $p \in [0, 1]$  = probability of page fault  $t_{ACCESS}$  = effective time for each memory reference

$$t_{ACCESS} = (1 - p) * t_{MA} + p * t_{FAULT}$$

Let's assume:  $t_{MA} = 100$  nsec and  $t_{FAULT} = 20$  msec = 20,000,000 nsec

$$t_{ACCESS} = (1 - p) * 100 + p * 20,000,000$$

```
t_{MA} = physical memory access time t_{FAULT} = time to handle a page fault p \in [0, 1] = probability of page fault t_{ACCESS} = effective time for each memory reference
```

$$t_{ACCESS} = (1 - p) * t_{MA} + p * t_{FAULT}$$

Let's assume:  $t_{MA} = 100$  nsec and  $t_{FAULT} = 20$  msec = 20,000,000 nsec

$$t_{ACCESS} = (1 - p) * 100 + p * 20,000,000$$

This heavily depends on p!

$$t_{ACCESS} = (1 - p) * 100 + p * 20,000,000$$

What if only 1 every 1,000 memory references causes a page fault (i.e., p = 0.001)

$$t_{ACCESS} = (1 - p) * 100 + p * 20,000,000$$

What if only 1 every 1,000 memory references causes a page fault (i.e., p = 0.001)

The access time increases from just 100 nsec up to ~20.1 microsec

200 times slowdown factor

$$t_{ACCESS} = (1 - p) * 100 + p * 20,000,000$$

What if we want the time access to be at most 10% slower than basic memory access?

$$t_{ACCESS} = (1 - p) * 100 + p * 20,000,000$$

What if we want the time access to be at most 10% slower than basic memory access?

We have to solve for p the following equation:

$$1.1 * 100 = (1 - p) * 100 + p * 20,000,000$$

$$t_{ACCESS} = (1 - p) * 100 + p * 20,000,000$$

What if we want the time access to be at most 10% slower than basic memory access?

We have to solve for p the following equation:

$$1.1 * 100 = (1 - p) * 100 + p * 20,000,000$$

$$1.1 * 100 = 100 - 100p + 20,000,000p = 19,999,900p = 110 - 100 =$$

To achieve that goal, we can tolerate at most 1 page fault every about 2 million accesses!

$$p = \frac{10}{19,999,900} = \frac{1}{1,999,990} \approx 0,0000005 = 5 * 10^{-7}$$

More generally, given  $t_{MA}$ ,  $t_{FAULT}$ , and a threshold  $\epsilon > 0$  if we want to find p s.t.:

$$t_{ACCESS} = (1 + \epsilon) * t_{MA}$$

We substitute t<sub>ACCESS</sub> and solve for p the resulting equation:

$$(1-p) * t_{MA} + p * t_{FAULT} = (1+\epsilon) * t_{MA} = t_{MA} - p * t_{MA} + p * t_{FAULT} = t_{MA} + \epsilon * t_{MA}$$
  
 $p(t_{FAULT} - t_{MA}) = \epsilon * t_{MA} = t_{MA}$ 

$$p = \frac{\epsilon * t_{MA}}{t_{FAULT} - t_{MA}}$$

### Virtual Memory: Considerations

 So far, we have described how the OS (with the support of HW) manages page faults

#### Virtual Memory: Considerations

- So far, we have described how the OS (with the support of HW) manages page faults
- Still, the OS has to answer 2 fundamental questions:
  - When to load process' pages into main memory (page fetching)
  - Which page to remove from memory if this gets filled (page replacement)

## Page Fetching Goals

- The overall goal is still to make physical memory look larger than it is
- Exploiting the locality reference of programs
- Keep in memory only those pages that is being used
- Keep on disk those pages that are unused
- Ideally, producing a memory system with the performance of main memory and the cost/capacity of disk!

## Page Fetching Strategies

3 page fetching strategies

## Page Fetching Strategies

3 page fetching strategies

#### Startup

This is a special case where all the pages of the process are loaded at once

virtual address space cannot be larger than physical memory

# Page Fetching Strategies

3 page fetching strategies

#### Startup

This is a special case where all the pages of the process are loaded at once

virtual address space cannot be larger than physical memory

#### Overlays

Let the programmer says when pages are loaded/removed

virtual address space can be larger than physical memory but hard and error-prone

## Page Fetching Strategies

3 page fetching strategies

#### Startup

This is a special case where all the pages of the process are loaded at once

virtual address space cannot be larger than physical memory

#### Overlays

Let the programmer says when pages are loaded/removed

virtual address space can be larger than physical memory but hard and error-prone

#### Demand

Process tells the OS when it needs a page

The OS manages page requests

# Page Fetching Strategies

3 page fetching strategies

#### Startup

This is a special case where all the pages of the process are loaded at once

virtual address space cannot be larger than physical memory

#### Overlays

Let the programmer says when pages are loaded/removed

virtual address space can be larger than physical memory but hard and error-prone

#### Demand

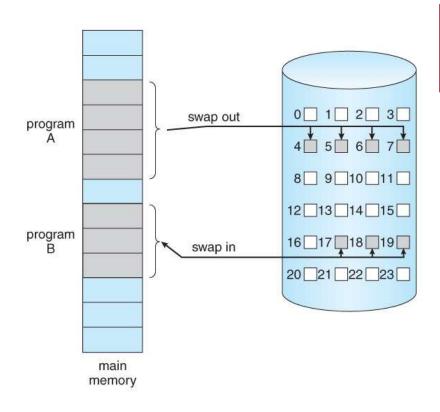
Process tells the OS when it needs a page

The OS manages page requests

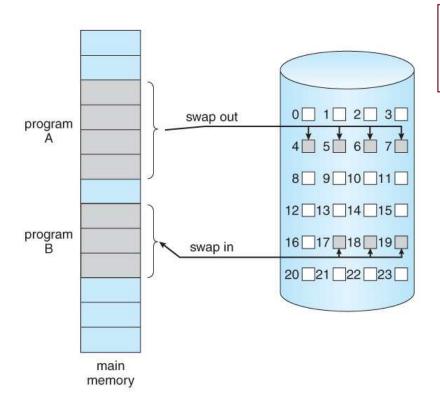
Most modern OSs use demand fetching

## (Pure) Demand Paging

- When a process starts up, **none** of its pages are loaded
- Rather, a page is swapped in only when the process references it (upon a page fault)
- This is termed a lazy swapper or pager
- Opposite of loading all the pages at process startup!



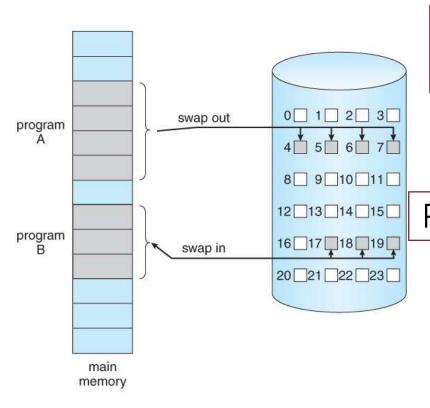
The pager guesses when pages will be needed and load them ahead of time



The pager guesses when pages will be needed and load them ahead of time

Trying to avoid page faults

12/12/23 78

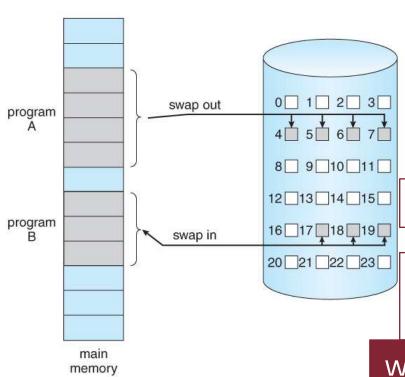


The pager guesses when pages will be needed and load them ahead of time

Trying to avoid page faults

Requires predicting the future  $\rightarrow$  very hard!

12/12/23 79



The pager guesses when pages will be needed and load them ahead of time

Trying to avoid page faults

Requires predicting the future  $\rightarrow$  very hard!

Possible approach: upon page fault, load many pages instead of only the faulty one

works if program accesses memory sequentially

• A portion of the disk reserved for storing pages that are evicted from memory

- A portion of the disk reserved for storing pages that are evicted from memory
- May be not part of the actual disk file system

- A portion of the disk reserved for storing pages that are evicted from memory
- May be not part of the actual disk file system
- On Linux there exists a dedicated swap partition (on disk)
  - no actual files are stored in that partition

- A portion of the disk reserved for storing pages that are evicted from memory
- May be not part of the actual disk file system
- On Linux there exists a dedicated swap partition (on disk)
  - no actual files are stored in that partition
- On Mac, instead, swap space is part of the file system (swapfiles)

## Swap Out

• When a page needs to be swapped out, it will be generally copied to disk

## Swap Out

- When a page needs to be swapped out, it will be generally copied to disk
- The pages for a process are divided into 2 groups:
  - Code (read-only)
  - Data (initialized/uninitialized)

## Swap Out

- When a page needs to be swapped out, it will be generally copied to disk
- The pages for a process are divided into 2 groups:
  - Code (read-only)
  - Data (initialized/uninitialized)
- Depending on which kind of page is removed, different optimizations may apply upon page swapout

#### Swap Out Optimizations

- Code page (read-only):
  - Code content does not change!
  - Just remove and load it back from executable file stored on disk
  - Make use of the filesystem

#### Swap Out Optimizations

- Code page (read-only):
  - Code content does not change!
  - Just remove and load it back from executable file stored on disk
  - Make use of the filesystem
- Data page:
  - Data content does actually change!
  - Save it to a separate paging file, so that no changes are lost when it will be loaded in the future
  - Need to use the dedicated swap space

• On a page fault, we need to load a page from disk into memory

- On a page fault, we need to load a page from disk into memory
- If physical memory has still free frames, the page can be safely loaded into one of those

- On a page fault, we need to load a page from disk into memory
- If physical memory has still free frames, the page can be safely loaded into one of those
- If physical memory is full, a frame must be swapped out to make room for the swap-in page

- On a page fault, we need to load a page from disk into memory
- If physical memory has still free frames, the page can be safely loaded into one of those
- If physical memory is full, a frame must be swapped out to make room for the swap-in page
- Several algorithms to select the page to evict from memory

• Random: pick any page at random (works surprisingly well!)

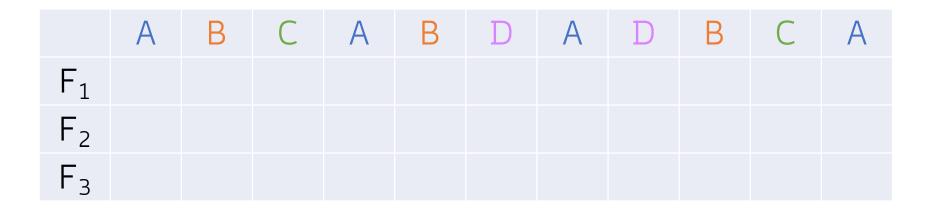
- Random: pick any page at random (works surprisingly well!)
- FIFO (First-In-First-Out): throw out the page that has been in memory for longest time (i.e., the oldest)
  - Easy to implement but may remove frequently accessed pages

- Random: pick any page at random (works surprisingly well!)
- FIFO (First-In-First-Out): throw out the page that has been in memory for longest time (i.e., the oldest)
  - Easy to implement but may remove frequently accessed pages
- MIN (OPT): remove the page that will not be accessed for the longest time (provably optimal [Belady 1966])
  - Needs to predict the future → very hard!

- Random: pick any page at random (works surprisingly well!)
- FIFO (First-In-First-Out): throw out the page that has been in memory for longest time (i.e., the oldest)
  - Easy to implement but may remove frequently accessed pages
- MIN (OPT): remove the page that will not be accessed for the longest time (provably optimal [Belady 1966])
  - Needs to predict the future → very hard!
- LRU (Least Recently Used): approximation of MIN, remove the page that has not been used in the longest time
  - Assumes the past is a good predictor of the future (not always true!)

3 physical frames:  $F_1$ ,  $F_2$ ,  $F_3$  4 virtual pages: A, B, C, D

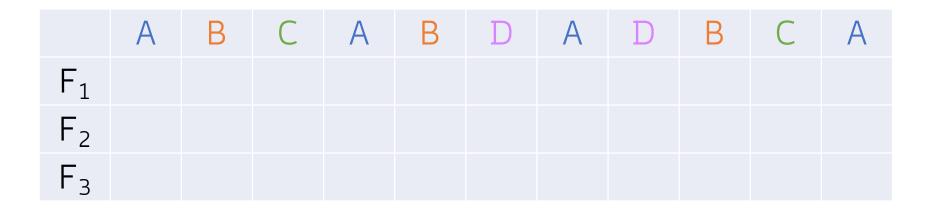
Reference sequence of pages: A, B, C, A, B, D, A, D, B, C, A



How many page faults (denoted by \*)?

3 physical frames:  $F_1$ ,  $F_2$ ,  $F_3$  4 virtual pages: A, B, C, D

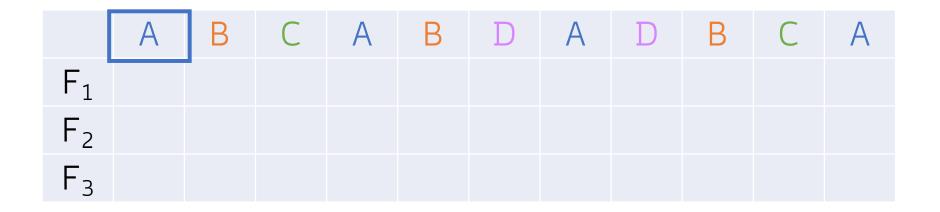
Reference sequence of pages: A, B, C, A, B, D, A, D, B, C, A



Initially, no frame is loaded in memory at all (pure demand paging)

3 physical frames:  $F_1$ ,  $F_2$ ,  $F_3$  4 virtual pages: A, B, C, D

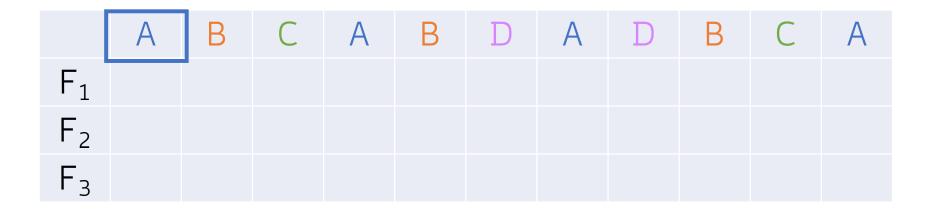
Reference sequence of pages: A, B, C, A, B, D, A, D, B, C, A



Virtual address within page A is referenced

3 physical frames:  $F_1$ ,  $F_2$ ,  $F_3 \mid 4$  virtual pages: A, B, C, D

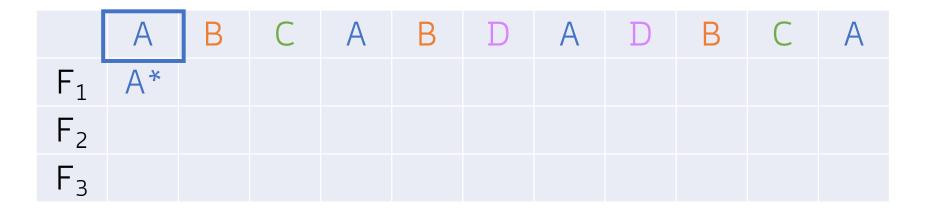
Reference sequence of pages: A, B, C, A, B, D, A, D, B, C, A



Virtual address within page A is referenced page fault

3 physical frames:  $F_1$ ,  $F_2$ ,  $F_3$  4 virtual pages: A, B, C, D

Reference sequence of pages: A, B, C, A, B, D, A, D, B, C, A



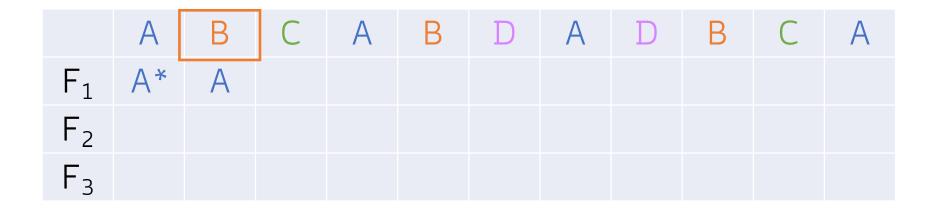
Virtual address within page A is referenced

page fault

A loaded

3 physical frames:  $F_1$ ,  $F_2$ ,  $F_3$  4 virtual pages: A, B, C, D

Reference sequence of pages: A, B, C, A, B, D, A, D, B, C, A

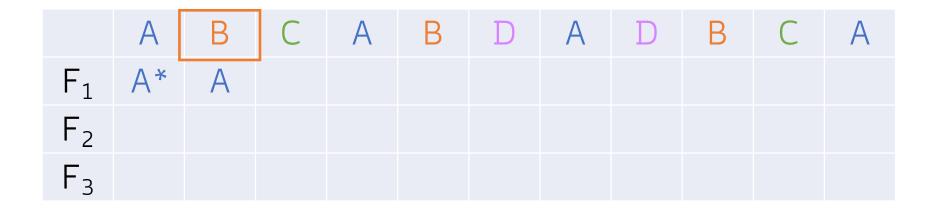


Virtual address within page B is referenced

FIFO = A

3 physical frames: F<sub>1</sub>, F<sub>2</sub>, F<sub>3</sub> 4 virtual pages: A, B, C, D

Reference sequence of pages: A, B, C, A, B, D, A, D, B, C, A



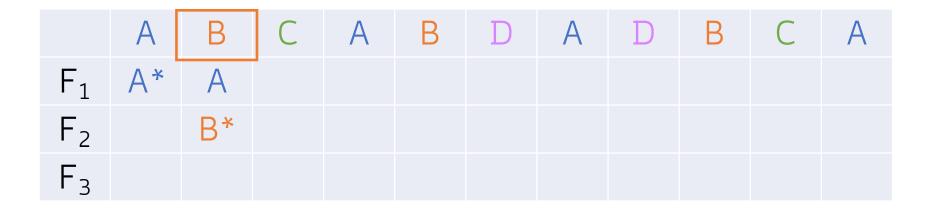
Virtual address within page B is referenced

page fault

FIFO = A

3 physical frames:  $F_1$ ,  $F_2$ ,  $F_3$  4 virtual pages: A, B, C, D

Reference sequence of pages: A, B, C, A, B, D, A, D, B, C, A



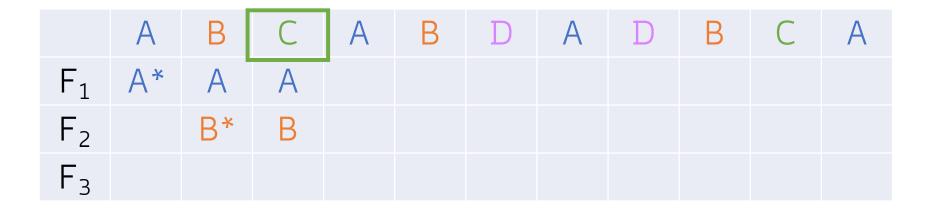
Virtual address within page B is referenced

page fault B loaded

FIFO = A → B

3 physical frames:  $F_1$ ,  $F_2$ ,  $F_3$  4 virtual pages: A, B, C, D

Reference sequence of pages: A, B, C, A, B, D, A, D, B, C, A

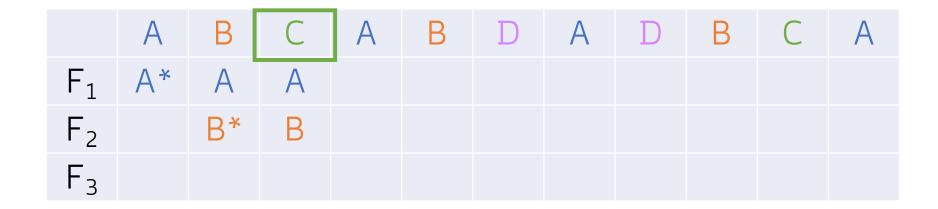


Virtual address within page C is referenced

 $FIFO = A \rightarrow B$ 

3 physical frames:  $F_1$ ,  $F_2$ ,  $F_3$  4 virtual pages: A, B, C, D

Reference sequence of pages: A, B, C, A, B, D, A, D, B, C, A



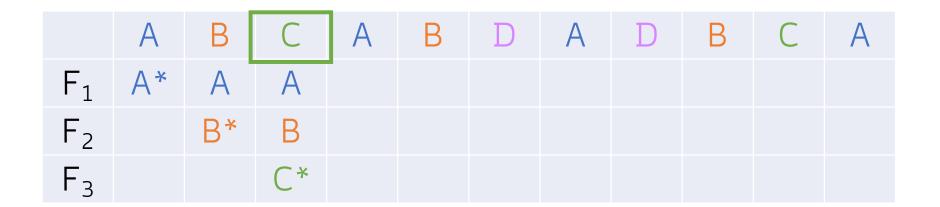
Virtual address within page C is referenced

page fault

 $FIFO = A \rightarrow B$ 

3 physical frames:  $F_1$ ,  $F_2$ ,  $F_3$  4 virtual pages: A, B, C, D

Reference sequence of pages: A, B, C, A, B, D, A, D, B, C, A

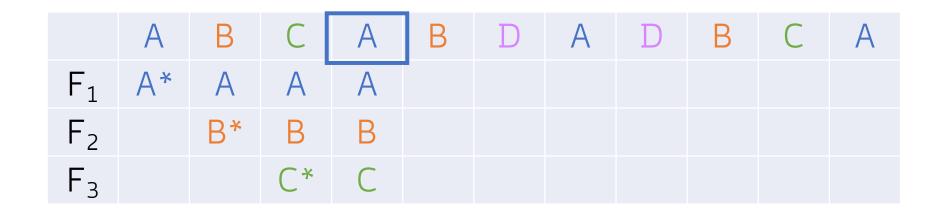


Virtual address within page C is referenced page fault

page fault C loaded

3 physical frames:  $F_1$ ,  $F_2$ ,  $F_3 \mid 4$  virtual pages: A, B, C, D

Reference sequence of pages: A, B, C, A, B, D, A, D, B, C, A



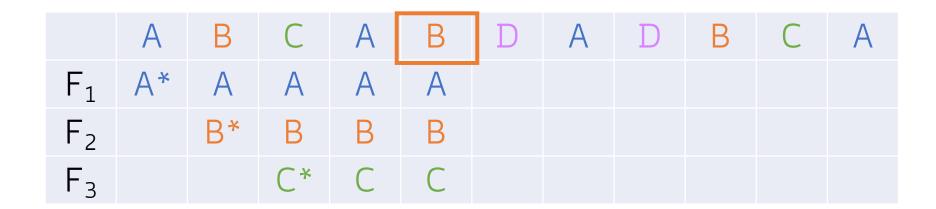
Virtual address within page A is referenced

$$\mathsf{FIFO} = \mathsf{A} \to \mathsf{B} \to \mathsf{C}$$

A is already loaded

3 physical frames:  $F_1$ ,  $F_2$ ,  $F_3 \mid 4$  virtual pages: A, B, C, D

Reference sequence of pages: A, B, C, A, B, D, A, D, B, C, A



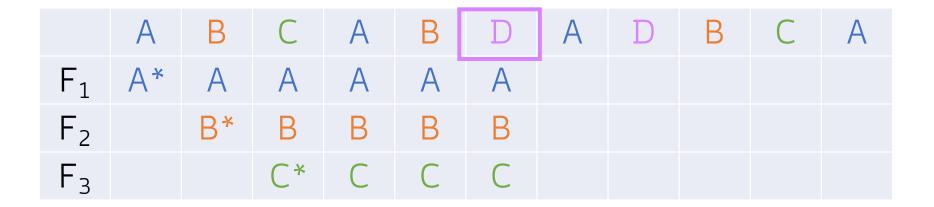
Virtual address within page B is referenced

$$FIFO = A \rightarrow B \rightarrow C$$

B is already loaded

3 physical frames:  $F_1$ ,  $F_2$ ,  $F_3$  4 virtual pages: A, B, C, D

Reference sequence of pages: A, B, C, A, B, D, A, D, B, C, A

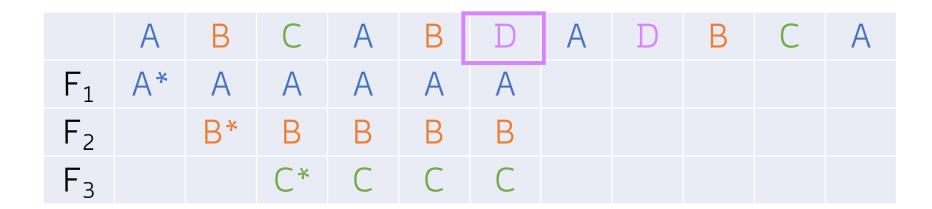


Virtual address within page D is referenced

 $\mathsf{FIFO} = \mathsf{A} \to \mathsf{B} \to \mathsf{C}$ 

3 physical frames:  $F_1$ ,  $F_2$ ,  $F_3 \mid 4$  virtual pages: A, B, C, D

Reference sequence of pages: A, B, C, A, B, D, A, D, B, C, A

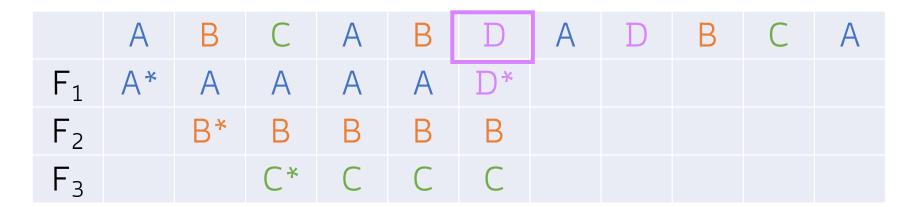


Virtual address within page D is referenced page fault

 $FIFO = A \rightarrow B \rightarrow C$ 

3 physical frames: F<sub>1</sub>, F<sub>2</sub>, F<sub>3</sub> 4 virtual pages: A, B, C, D

Reference sequence of pages: A, B, C, A, B, D, A, D, B, C, A



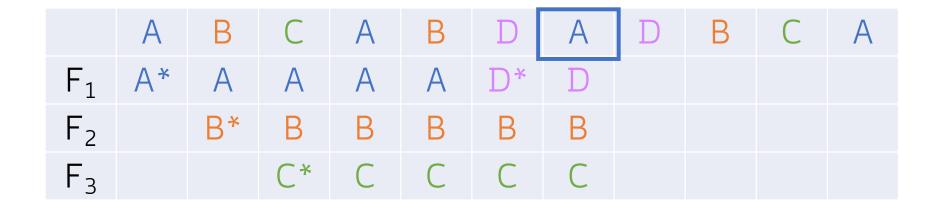
Virtual address within page D is referenced page fault

page fault

A replaced D loaded

3 physical frames: F<sub>1</sub>, F<sub>2</sub>, F<sub>3</sub> 4 virtual pages: A, B, C, D

Reference sequence of pages: A, B, C, A, B, D, A, D, B, C, A

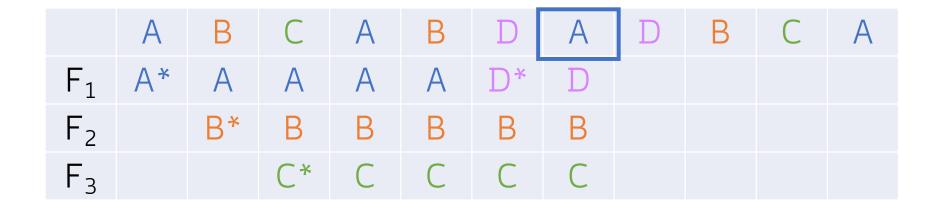


Virtual address within page A is referenced

$$\mathsf{FIFO} = \mathsf{B} \to \mathsf{C} \to \mathsf{D}$$

3 physical frames:  $F_1$ ,  $F_2$ ,  $F_3 \mid 4$  virtual pages: A, B, C, D

Reference sequence of pages: A, B, C, A, B, D, A, D, B, C, A

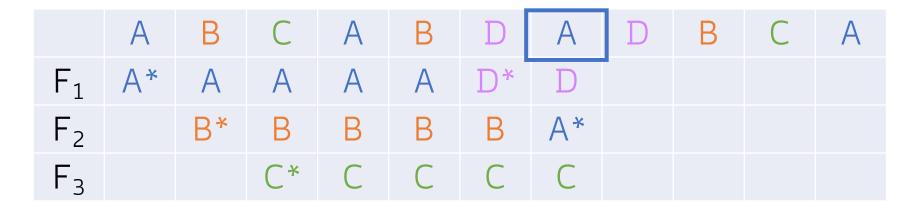


Virtual address within page A is referenced page fault

 $FIFO = B \rightarrow C \rightarrow D$ 

3 physical frames:  $F_1$ ,  $F_2$ ,  $F_3 \mid 4$  virtual pages: A, B, C, D

Reference sequence of pages: A, B, C, A, B, D, A, D, B, C, A

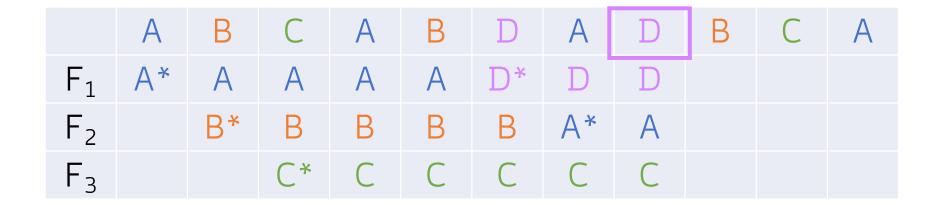


Virtual address within page A is referenced page fault

B replaced A loaded

3 physical frames:  $F_1$ ,  $F_2$ ,  $F_3 \mid 4$  virtual pages: A, B, C, D

Reference sequence of pages: A, B, C, A, B, D, A, D, B, C, A



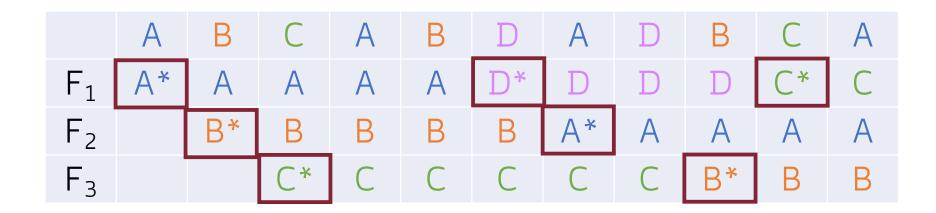
Virtual address within page D is referenced

$$\mathsf{FIFO} = \mathsf{C} \to \mathsf{D} \to \mathsf{A}$$

is already loaded

```
3 physical frames: F_1, F_2, F_3 4 virtual pages: A, B, C, D
```

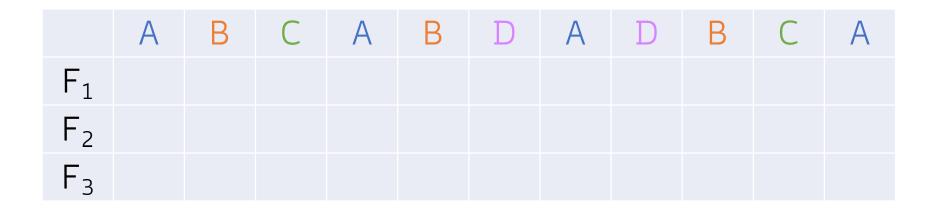
Reference sequence of pages: A, B, C, A, B, D, A, D, B, C, A



Eventually, we get a total of 7 page faults

3 physical frames:  $F_1$ ,  $F_2$ ,  $F_3$  4 virtual pages: A, B, C, D

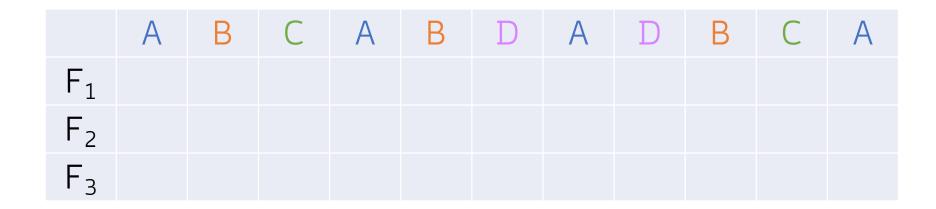
Reference sequence of pages: A, B, C, A, B, D, A, D, B, C, A



How many page faults (denoted by \*)?

3 physical frames:  $F_1$ ,  $F_2$ ,  $F_3$  4 virtual pages: A, B, C, D

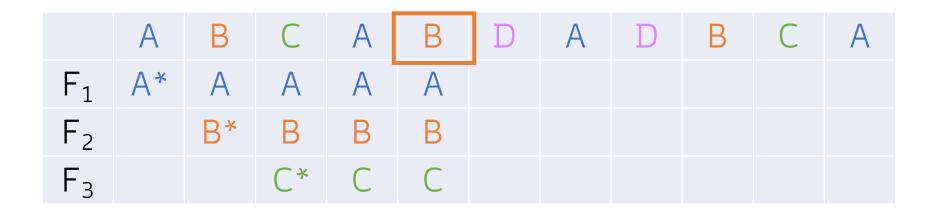
Reference sequence of pages: A, B, C, A, B, D, A, D, B, C, A



Initially, no frame is loaded in memory at all (pure demand paging)

```
3 physical frames: F_1, F_2, F_3 4 virtual pages: A, B, C, D
```

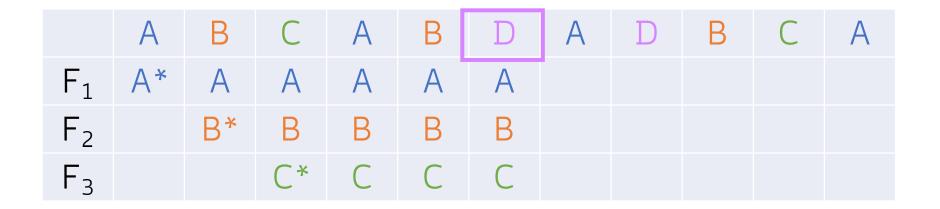
Reference sequence of pages: A, B, C, A, B, D, A, D, B, C, A



Up to this point, the same as FIFO

```
3 physical frames: F_1, F_2, F_3 4 virtual pages: A, B, C, D
```

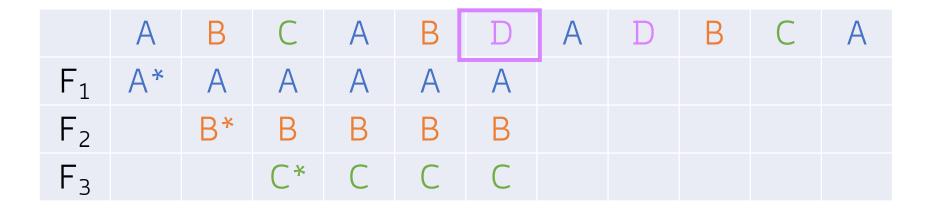
Reference sequence of pages: A, B, C, A, B, D, A, D, B, C, A



Virtual address within page D is referenced

```
3 physical frames: F_1, F_2, F_3 \mid | 4 virtual pages: A, B, C, D
```

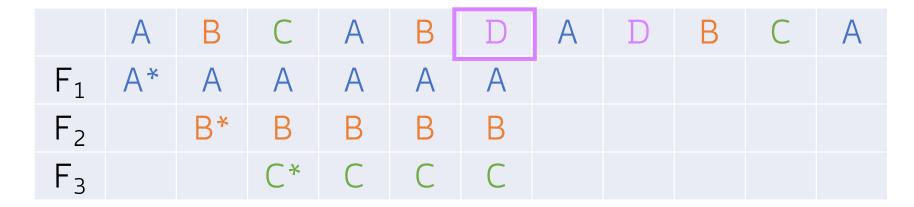
Reference sequence of pages: A, B, C, A, B, D, A, D, B, C, A



Virtual address within page D is referenced page fault

3 physical frames:  $F_1$ ,  $F_2$ ,  $F_3 \mid | 4$  virtual pages: A, B, C, D

Reference sequence of pages: A, B, C, A, B, D, A, D, B, C, A

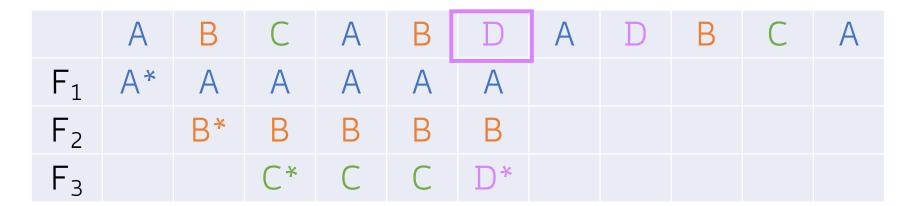


Virtual address within page D is referenced page fault

What's the page that will be requested the furthest away?

3 physical frames:  $F_1$ ,  $F_2$ ,  $F_3 \mid 4$  virtual pages: A, B, C, D

Reference sequence of pages: A, B, C, A, B, D, A, D, B, C, A



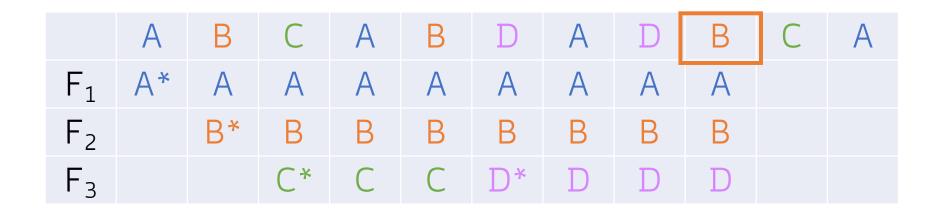
Virtual address within page D is referenced page fault

C replaced D loaded

C is the page that will be requested the furthest away

```
3 physical frames: F_1, F_2, F_3 4 virtual pages: A, B, C, D
```

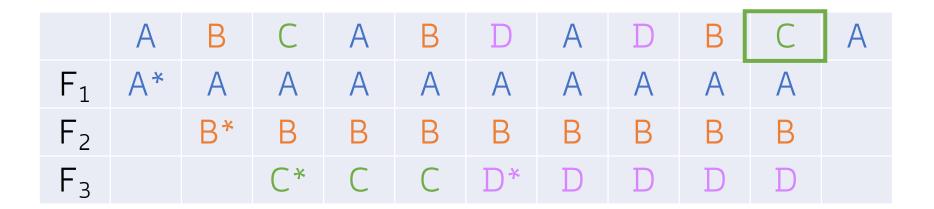
Reference sequence of pages: A, B, C, A, B, D, A, D, B, C, A



Up to this point, no more page faults

```
3 physical frames: F_1, F_2, F_3 4 virtual pages: A, B, C, D
```

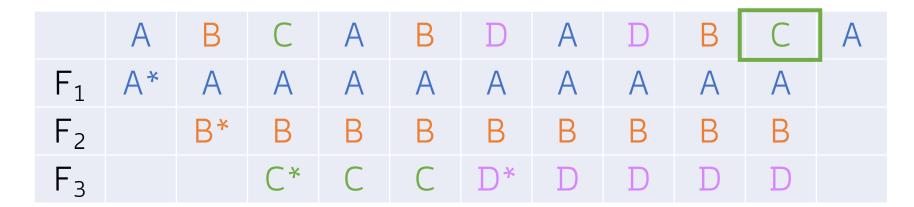
Reference sequence of pages: A, B, C, A, B, D, A, D, B, C, A



Virtual address within page C is referenced

3 physical frames:  $F_1$ ,  $F_2$ ,  $F_3 \mid 4$  virtual pages: A, B, C, D

Reference sequence of pages: A, B, C, A, B, D, A, D, B, C, A



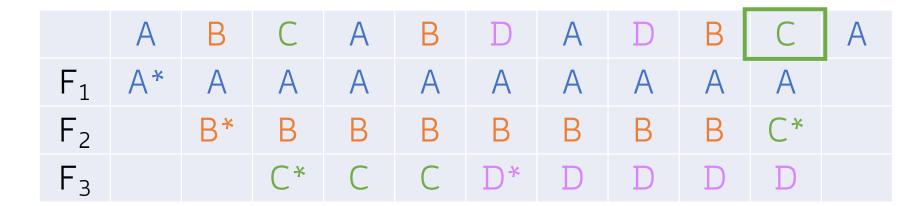
Virtual address within page C is referenced

page fault

What's the page that will be requested the furthest away?

3 physical frames:  $F_1$ ,  $F_2$ ,  $F_3$  4 virtual pages: A, B, C, D

Reference sequence of pages: A, B, C, A, B, D, A, D, B, C, A



Virtual address within page C is referenced

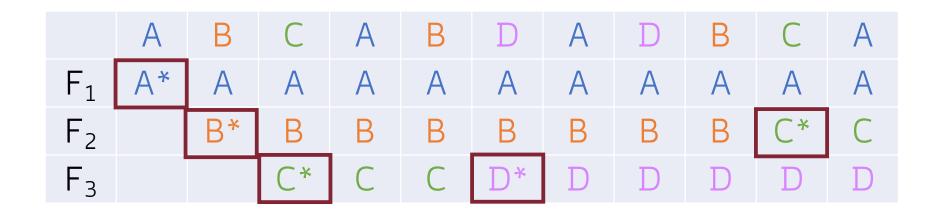
page fault

B replaced C loaded

B or D will be requested the furthest away (surely not A): pick one (e.g., B)

```
3 physical frames: F_1, F_2, F_3 4 virtual pages: A, B, C, D
```

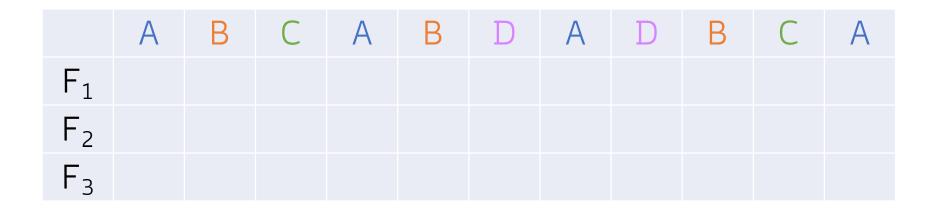
Reference sequence of pages: A, B, C, A, B, D, A, D, B, C, A



Eventually, we get a total of 5 page faults

```
3 physical frames: F_1, F_2, F_3 4 virtual pages: A, B, C, D
```

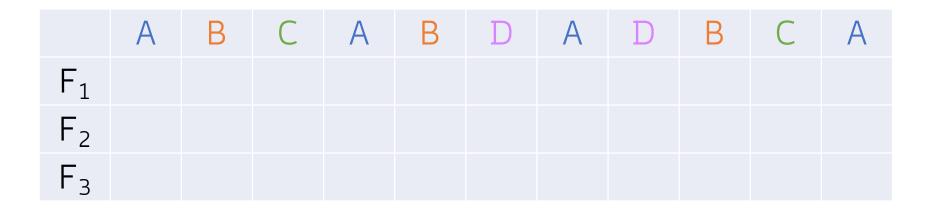
Reference sequence of pages: A, B, C, A, B, D, A, D, B, C, A



How many page faults (denoted by \*)?

```
3 physical frames: F_1, F_2, F_3 4 virtual pages: A, B, C, D
```

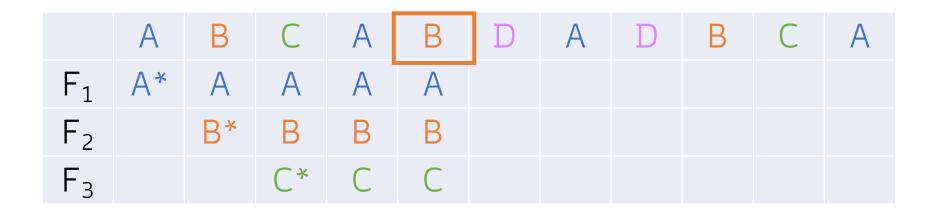
Reference sequence of pages: A, B, C, A, B, D, A, D, B, C, A



Initially, no frame is loaded in memory at all (pure demand paging)

```
3 physical frames: F_1, F_2, F_3 4 virtual pages: A, B, C, D
```

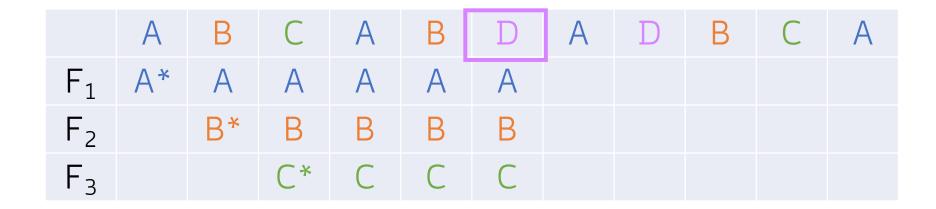
Reference sequence of pages: A, B, C, A, B, D, A, D, B, C, A



Up to this point, the same as FIFO

```
3 physical frames: F_1, F_2, F_3 \mid | 4 virtual pages: A, B, C, D
```

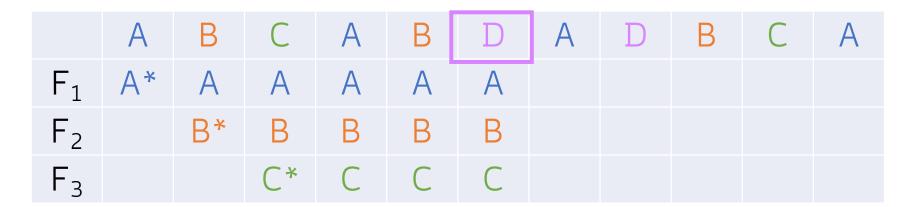
Reference sequence of pages: A, B, C, A, B, D, A, D, B, C, A



Virtual address within page D is referenced page fault

```
3 physical frames: F_1, F_2, F_3 \mid 4 virtual pages: A, B, C, D
```

Reference sequence of pages: A, B, C, A, B, D, A, D, B, C, A

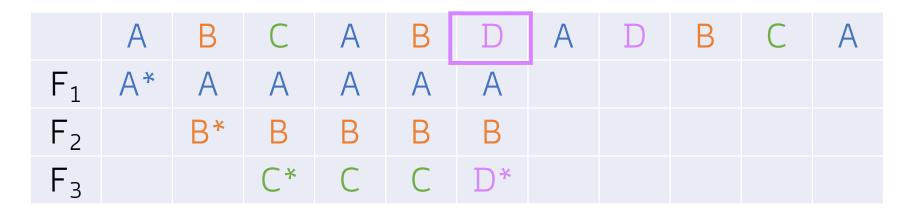


Virtual address within page D is referenced page fault

We can't look forward anymore!

```
3 physical frames: F_1, F_2, F_3 \mid 4 virtual pages: A, B, C, D
```

Reference sequence of pages: A, B, C, A, B, D, A, D, B, C, A



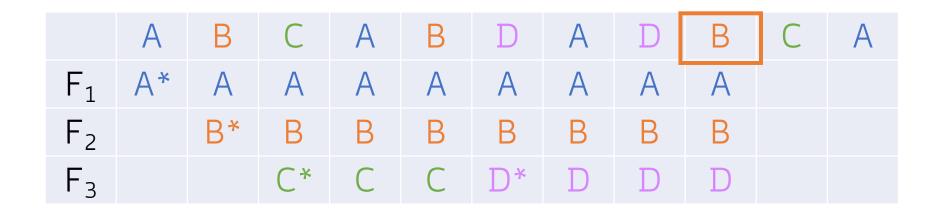
Virtual address within page D is referenced page fault

C replaced D loaded

C is the page that has not been used for the longest time in the past

```
3 physical frames: F_1, F_2, F_3 4 virtual pages: A, B, C, D
```

Reference sequence of pages: A, B, C, A, B, D, A, D, B, C, A

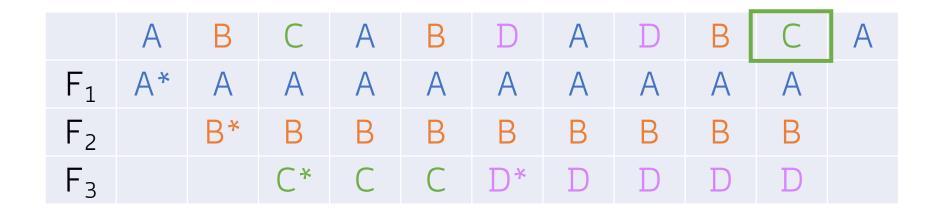


Up to this point, no more page faults

137

```
3 physical frames: F_1, F_2, F_3 4 virtual pages: A, B, C, D
```

Reference sequence of pages: A, B, C, A, B, D, A, D, B, C, A



Virtual address within page C is referenced

```
3 physical frames: F_1, F_2, F_3 4 virtual pages: A, B, C, D
```

Reference sequence of pages: A, B, C, A, B, D, A, D, B, C, A

```
      A
      B
      C
      A
      B
      D
      A
      D
      B
      C
      A

      F1
      A*
      A
      A
      A
      A
      A
      A
      A
      A
      A
      A
      A
      A
      A
      A
      A
      A
      A
      A
      A
      A
      A
      A
      A
      A
      A
      A
      A
      A
      A
      A
      A
      A
      A
      A
      A
      A
      A
      A
      A
      A
      A
      A
      A
      A
      B
      B
      B
      B
      B
      B
      B
      B
      B
      B
      B
      B
      B
      B
      B
      B
      B
      B
      B
      B
      B
      B
      B
      B
      B
      B
      B
      B
      B
      B
      B
      B
      B
      B
      B
      B
      B
      B
      B
      D
      D
      D
      D
      D
      D
      D
      D
      D
      D
      D
      D
      D
      D
      D
      D
      D
      D
      D
      D
      D
      D</td
```

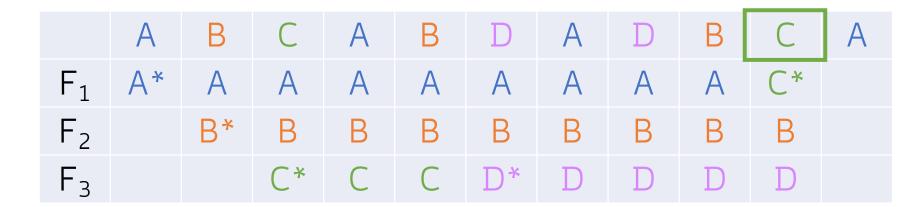
Virtual address within page C is referenced

page fault

We can't look forward anymore!

3 physical frames:  $F_1$ ,  $F_2$ ,  $F_3$  4 virtual pages: A, B, C, D

Reference sequence of pages: A, B, C, A, B, D, A, D, B, C, A



Virtual address within page C is referenced

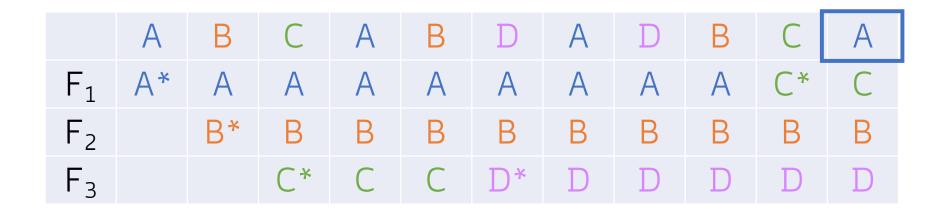
page fault

A replaced C loaded

A is the page that has not been used for the longest time in the past

```
3 physical frames: F_1, F_2, F_3 4 virtual pages: A, B, C, D
```

Reference sequence of pages: A, B, C, A, B, D, A, D, B, C, A



Virtual address within page A is referenced

```
3 physical frames: F_1, F_2, F_3 4 vir
```

4 virtual pages: A, B, C, D

Reference sequence of pages: A, B, C, A, B, D, A, D, B, C, A

```
      A
      B
      C
      A
      B
      D
      A
      D
      B
      C
      A

      F1
      A*
      A
      A
      A
      A
      A
      A
      A
      C*
      C

      F2
      B*
      B
      B
      B
      B
      B
      B
      B
      B
      B

      F3
      C*
      C
      C
      D*
      D
      D
      D
      D
```

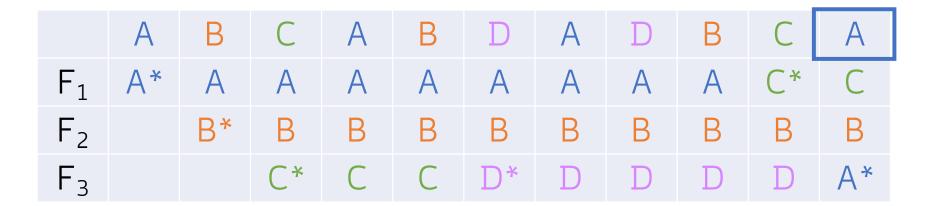
Virtual address within page A is referenced

page fault

We can't look forward anymore!

3 physical frames:  $F_1$ ,  $F_2$ ,  $F_3$  4 virtual pages: A, B, C, D

Reference sequence of pages: A, B, C, A, B, D, A, D, B, C, A



Virtual address within page A is referenced

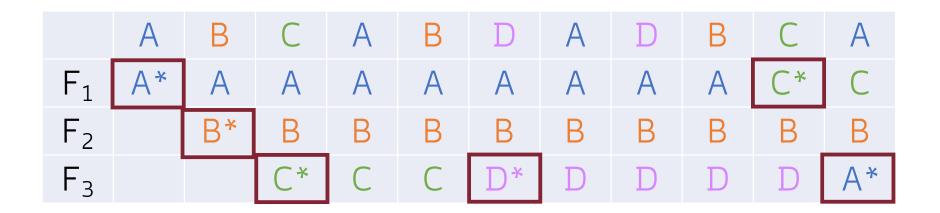
page fault

D replaced A loaded

D is the page that has not been used for the longest time in the past

```
3 physical frames: F_1, F_2, F_3 4 virtual pages: A, B, C, D
```

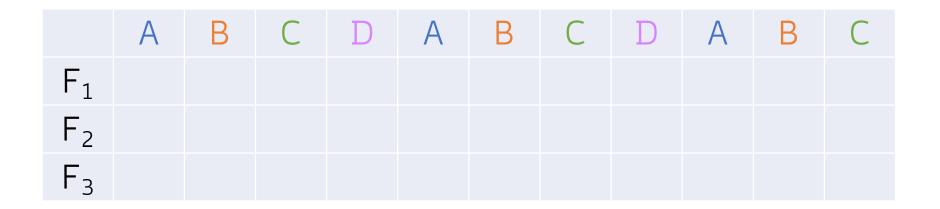
Reference sequence of pages: A, B, C, A, B, D, A, D, B, C, A



Eventually, we get a total of 6 page faults

```
3 physical frames: F_1, F_2, F_3 4 virtual pages: A, B, C, D
```

Reference sequence of pages: A, B, C, D, A, B, C, D, A, B, C



How many page faults (denoted by \*)?

```
3 physical frames: F_1, F_2, F_3 4 virtual pages: A, B, C, D
```

Reference sequence of pages: A, B, C, D, A, B, C, D, A, B, C

	A	В	C	D	Α	В	C	D	A	В	C
$F_1$	A*	A	A								
$F_2$		B*	В								
$F_3$			C*								

12/12/23 146

```
3 physical frames: F_1, F_2, F_3 4 virtual pages: A, B, C, D
```

Reference sequence of pages: A, B, C, D, A, B, C, D, A, B, C

	A	В	C	D	Α	В	C	D	A	В	C
$F_1$	<b>A</b> *	A	Α	D*							
$F_2$		B*	В	В							
$F_3$			C*	C							

```
3 physical frames: F_1, F_2, F_3 \mid | 4 virtual pages: A, B, C, D
```

Reference sequence of pages: A, B, C, D, A, B, C, D, A, B, C

```
A B C D A B
F<sub>1</sub> A* A A D* D
F<sub>2</sub> B* B B A*
F_3
```

```
3 physical frames: F_1, F_2, F_3 4 virtual pages: A, B, C, D
```

Reference sequence of pages: A, B, C, D, A, B, C, D, A, B, C

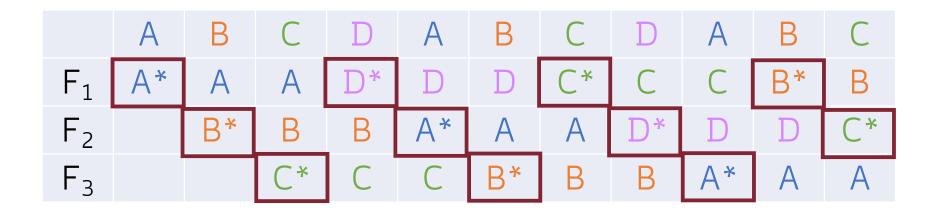
```
3 physical frames: F_1, F_2, F_3 4 virtual pages: A, B, C, D
```

Reference sequence of pages: A, B, C, D, A, B, C, D, A, B, C

```
A B C D A B C D
F<sub>1</sub> A* A A D* D D C*
F<sub>2</sub> B* B A* A A
F_3
```

```
3 physical frames: F_1, F_2, F_3 \mid 4 virtual pages: A, B, C, D
```

Reference sequence of pages: A, B, C, D, A, B, C, D, A, B, C



Eventually, we get a total of 11 page faults

# Page Replacement: What If We Add Memory?

- Does adding memory always reduce the number of page faults?
- Intuitively, it would seem so...
- The answer, in fact, depends on the page replacement algorithm
- Let's see this with an example, using FIFO page replacement

# FIFO Page Replacement: Example

```
5 virtual pages: A, B, C, D, E

3 physical frames: F<sub>1</sub>, F<sub>2</sub>, F<sub>3</sub>

4 physical frames: F<sub>1</sub>, F<sub>2</sub>, F<sub>3</sub>, F<sub>4</sub>

Scenario 1
```

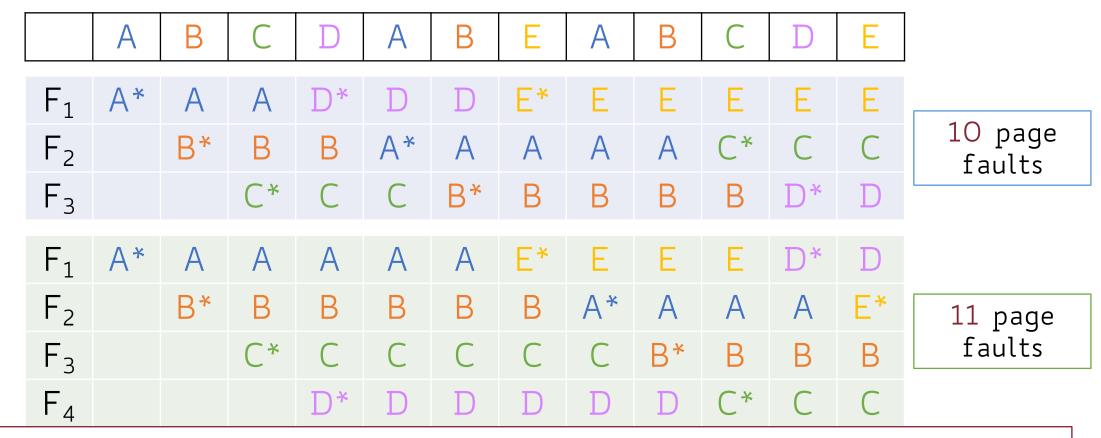
Reference sequence of pages: A, B, C, D, A, B, E, A, B, C, D, E

# FIFO Page Replacement: Example

	A	В	U	D	Α	В	Ε	A	В	U	D	Ε
$F_1$	<b>A</b> *	Α	Α	D*	D	D	E*	Ε	Ε	Ε	Ε	Ε
$F_2$		B*	В	В	A*	Α	Α	Α	Α	C*	C	C
$F_3$			C*	C	C	B*	В	В	В	В	D*	D
$F_1$	<b>A</b> *	Α	Α	Α	Α	Α	E*	Ε	Ε	Ε	D*	D
$F_2$		B*	В	В	В	В	В	A*	Α	Α	Α	E*
$F_3$			C*	C	C	C	C	C	B*	В	В	В
$F_4$				D*	D	D	D	D	D	C*	C	C

12/12/23 154

### FIFO Page Replacement: Example



Belady's Anomaly

Adding page frames may cause more page faults with some algorithms

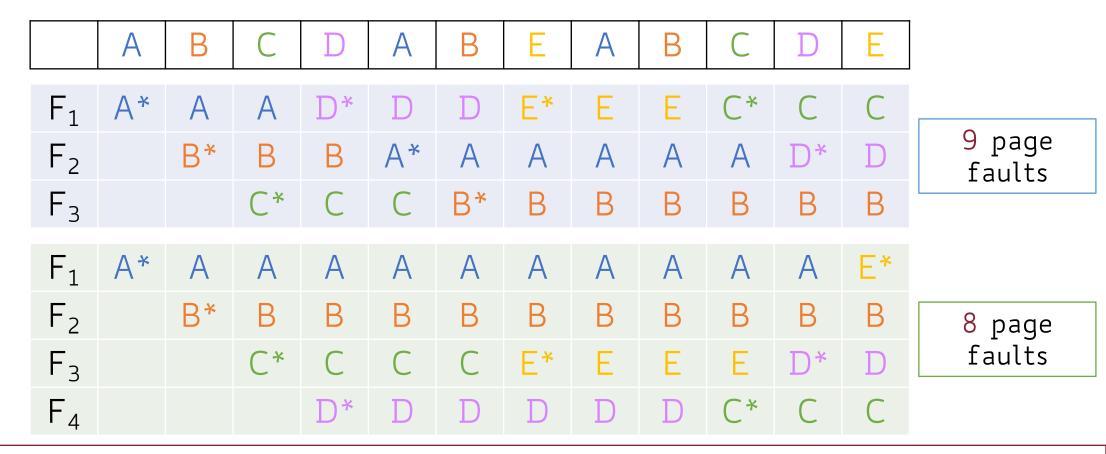
12/12/23 155

# LRU Page Replacement: Example



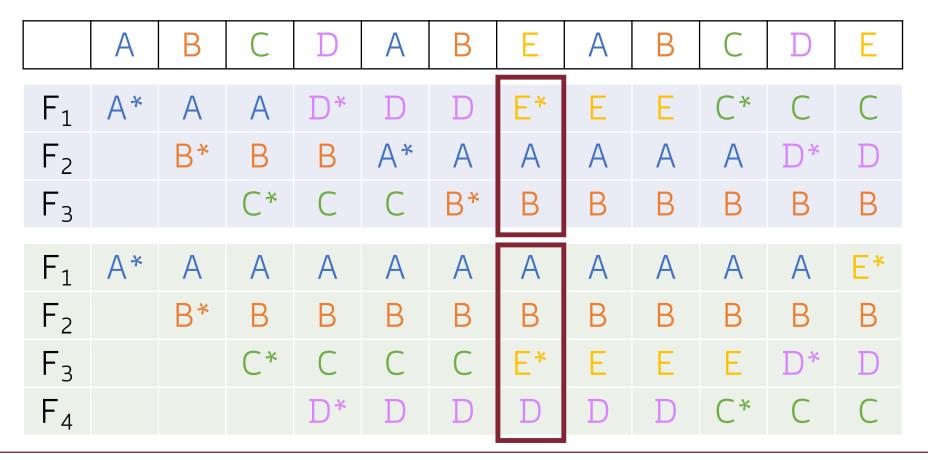
With LRU, adding page frames always decreases the number of page faults

# LRU Page Replacement: Example



With LRU, adding page frames always decreases the number of page faults

# LRU Page Replacement: Example



At each point in time 4-frame memory contains a subset of 3-frame

### Page Replacement: Summary

- FIFO is easy to implement but may lead to too many page faults
- May suffer from Belady's Anomaly

### Page Replacement: Summary

 MIN is the optimal choice but cannot be used in practice since future memory references are never known in advance

### Page Replacement: Summary

- LRU is a fair approximation of MIN assuming the past is a good predictor of the future
  - Exploits the locality reference (small working set that fits in memory)
  - Works poorly when the locality reference doesn't hold (large working set)