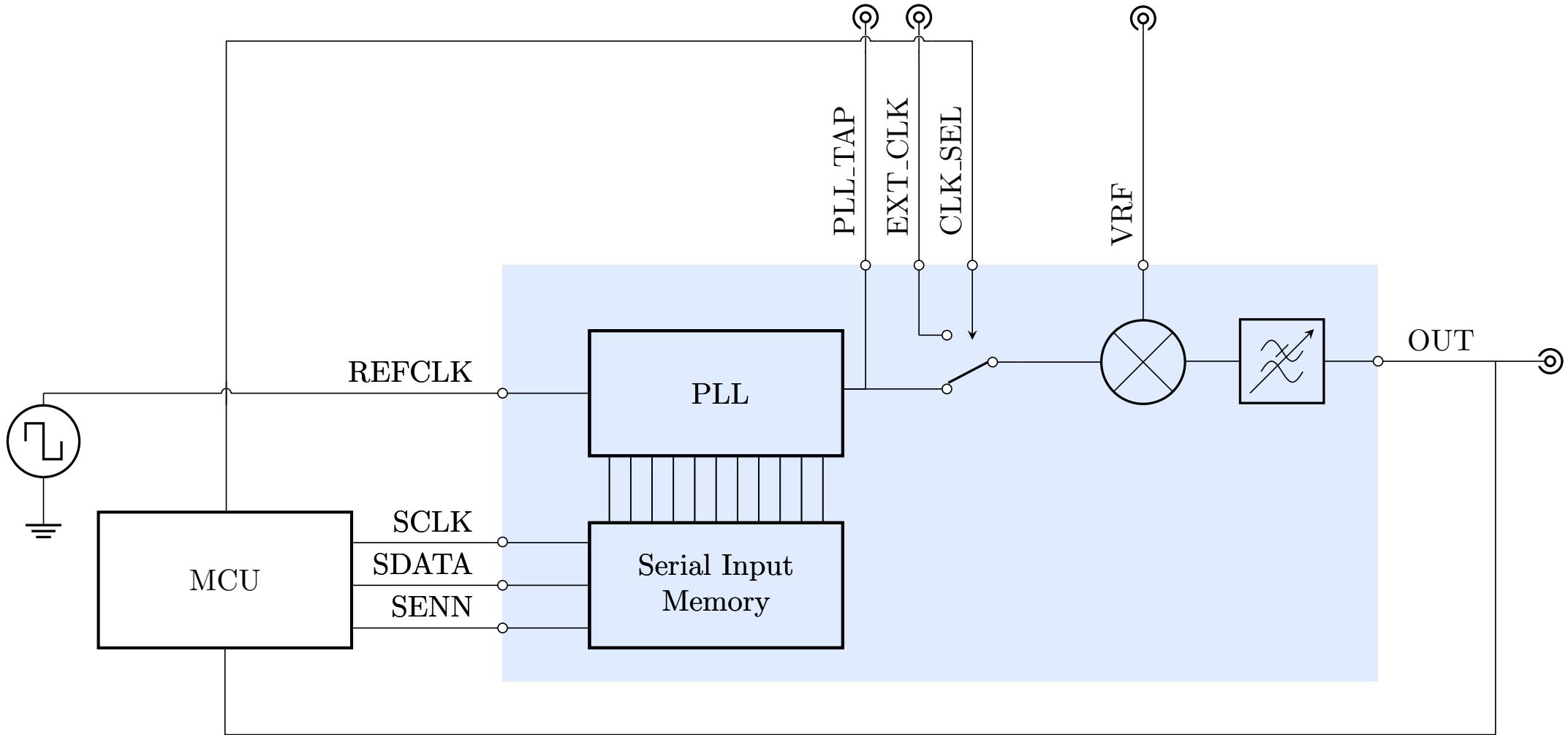


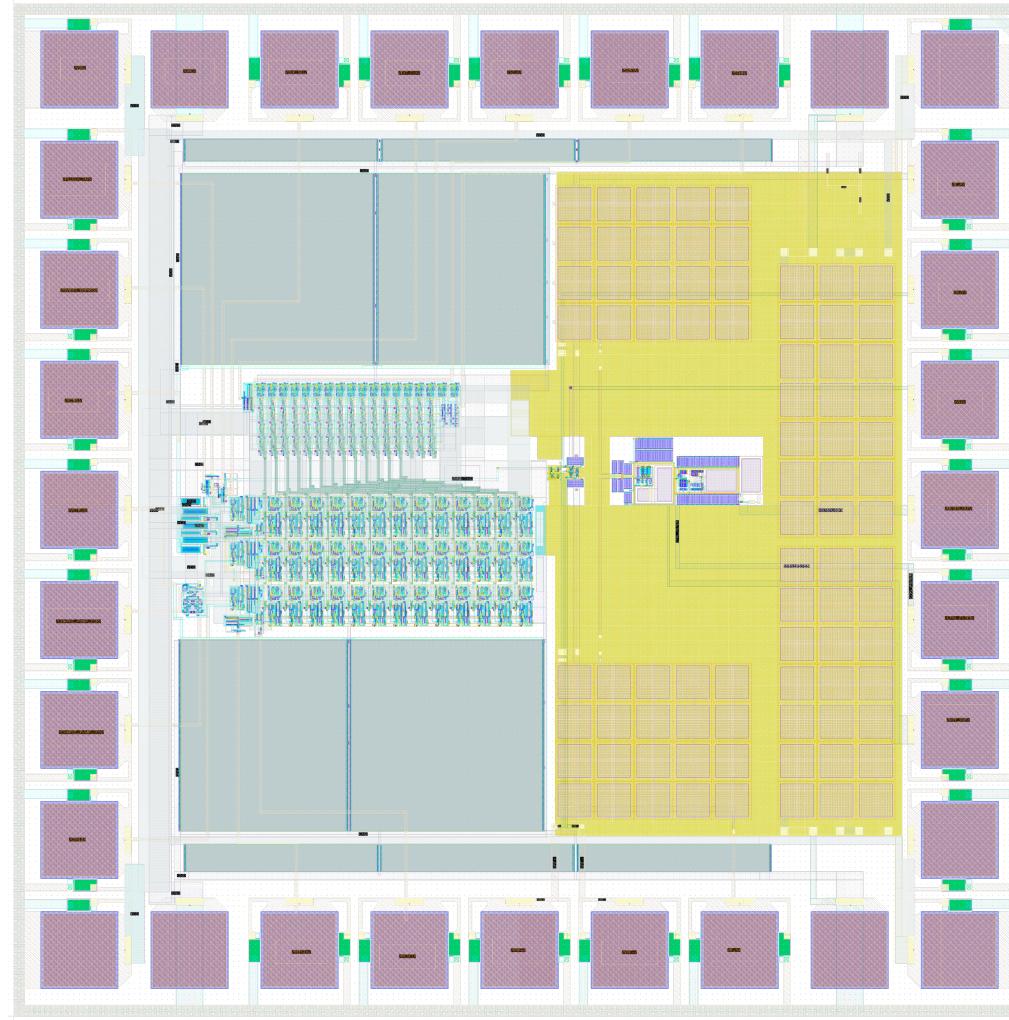
Spectrum Analyzer

Team 4: Zonghua Ouyang & Abhik Kumar

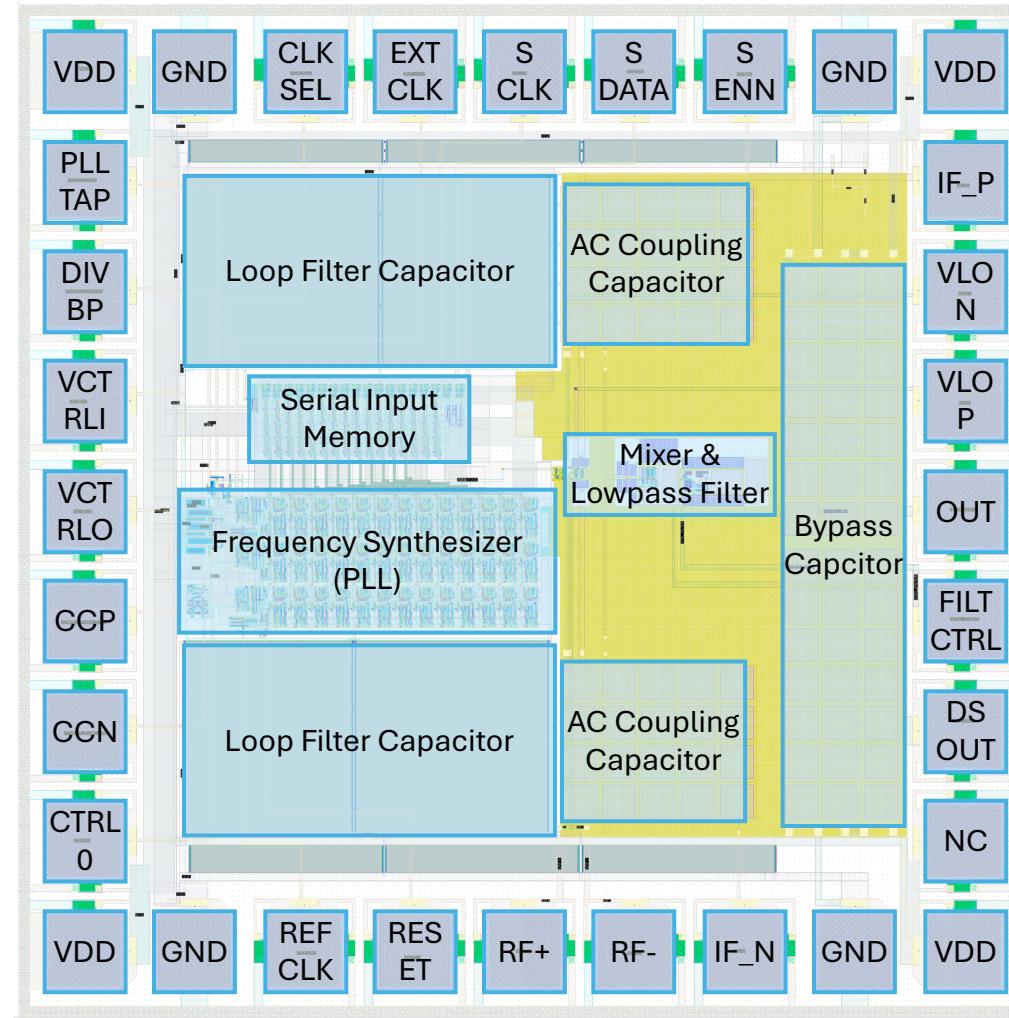
Block Diagram



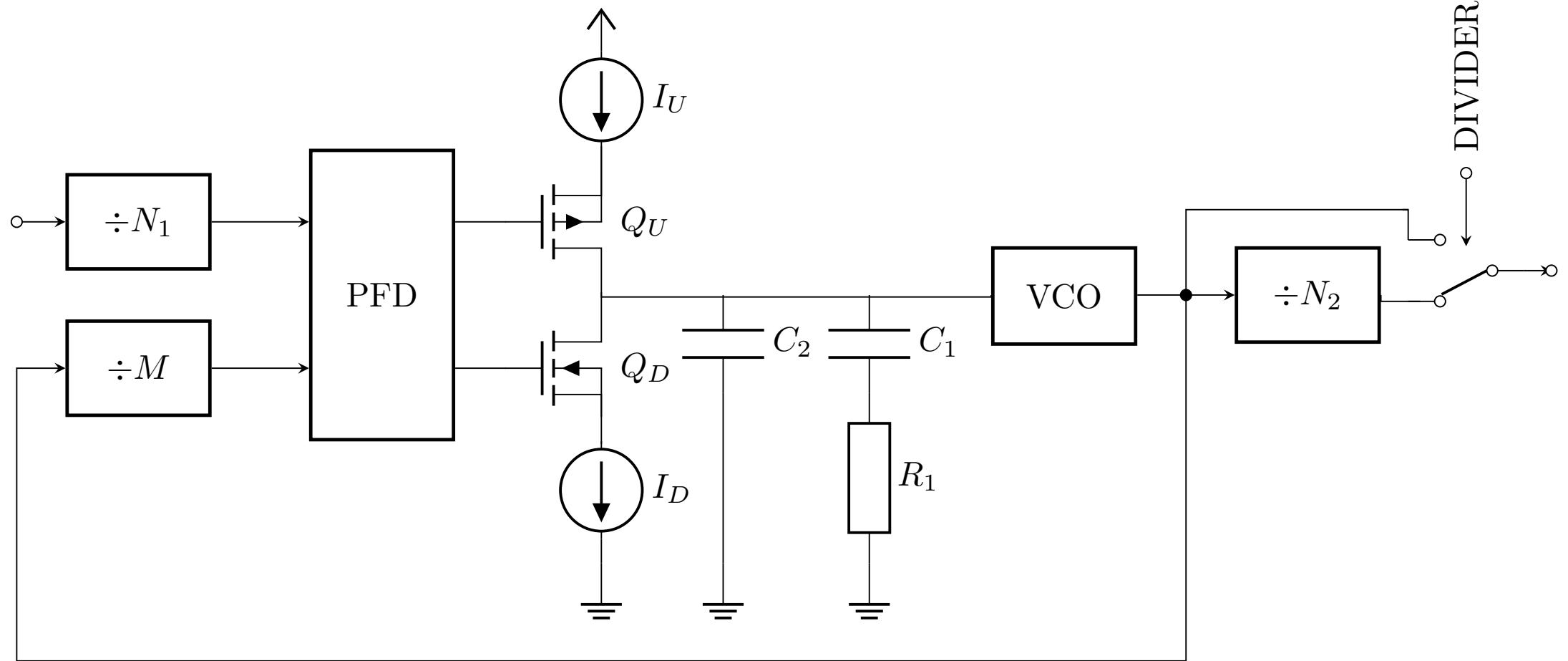
Layout



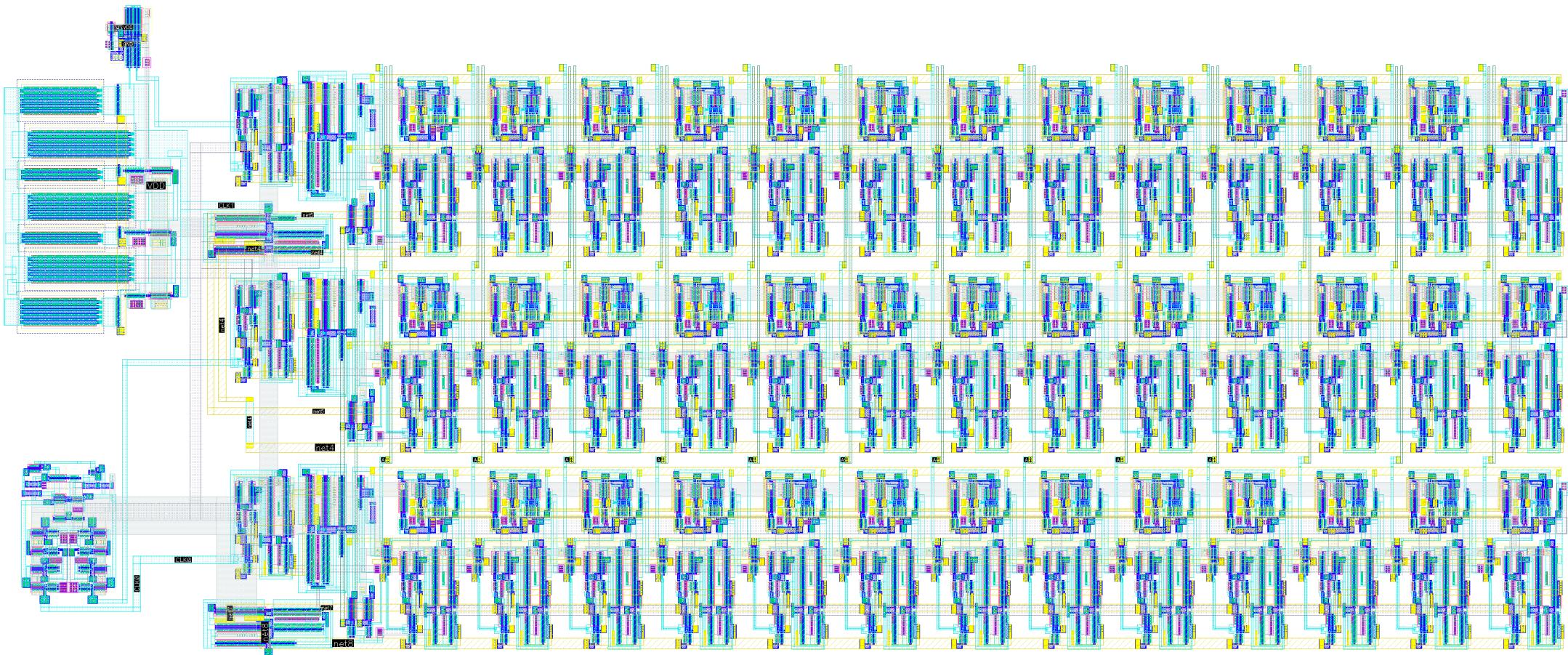
Layout



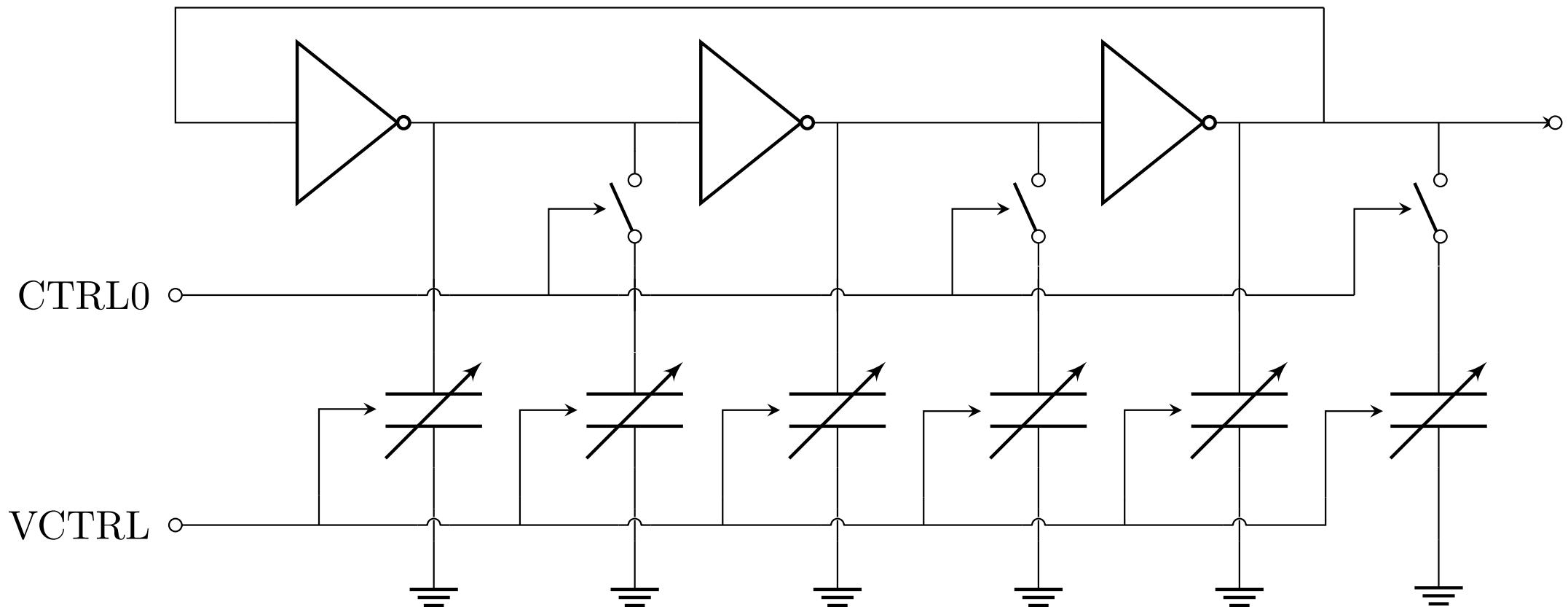
PLL: Block Diagram



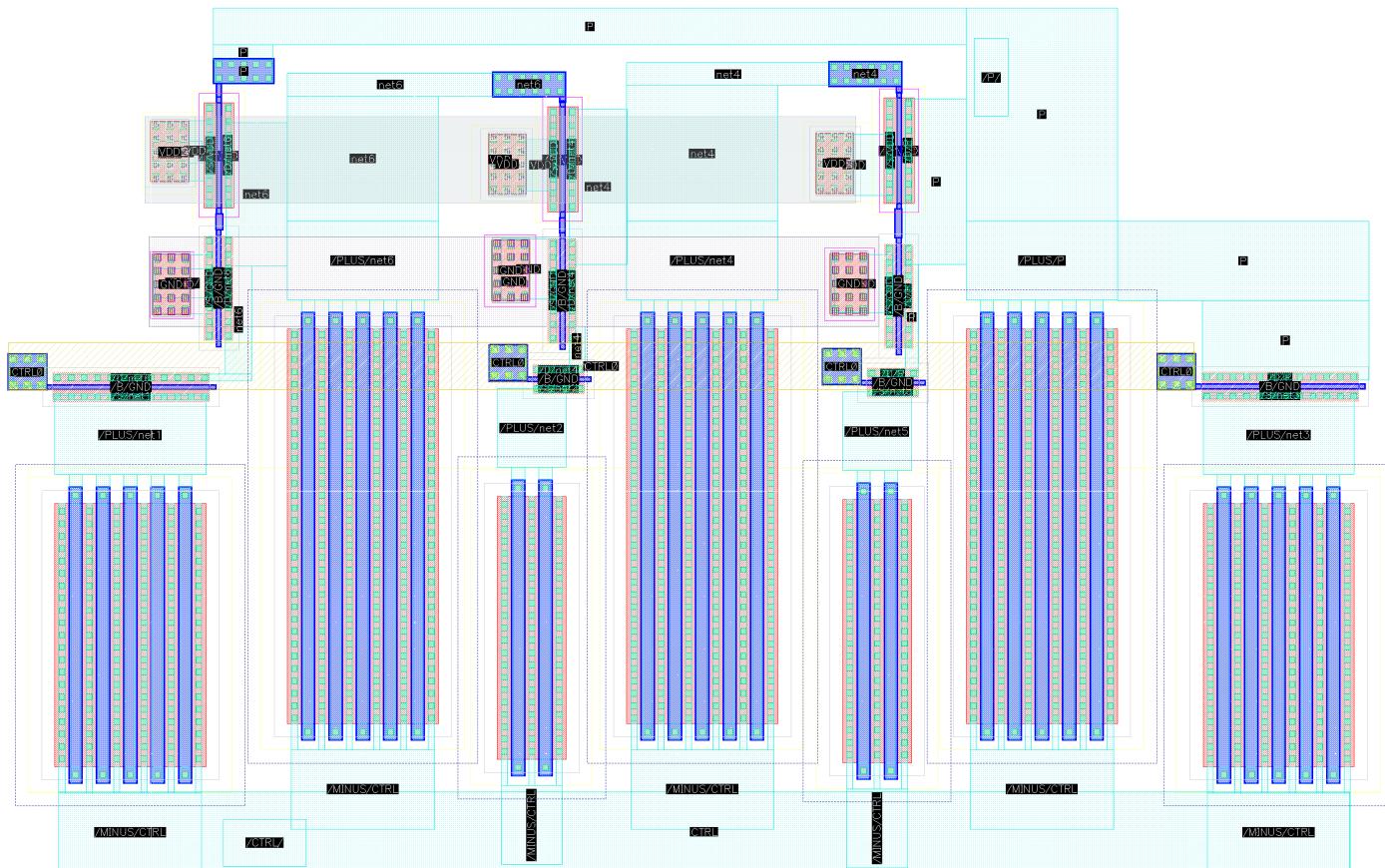
PLL: Layout



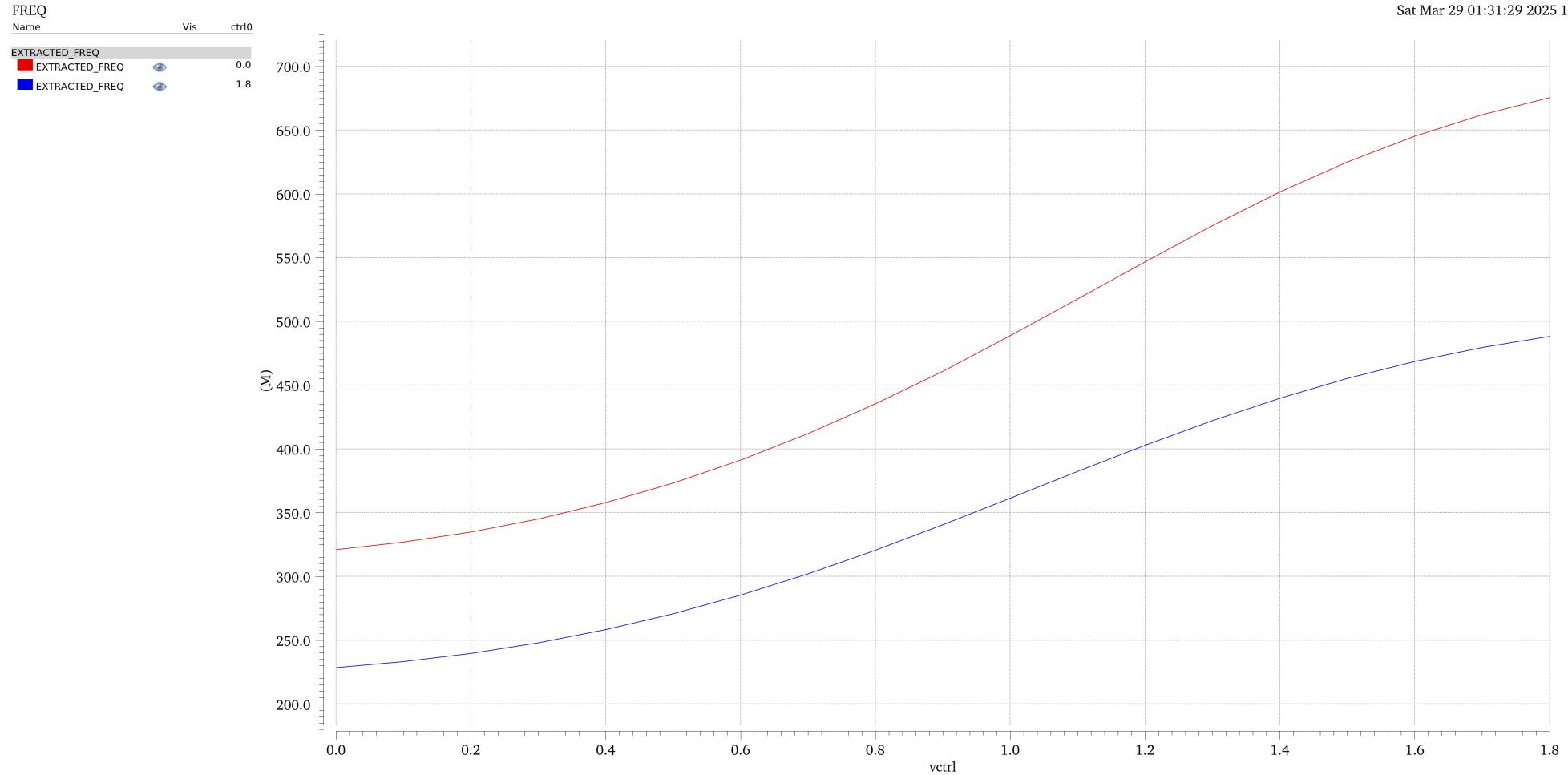
PLL: VCO: Block Diagram



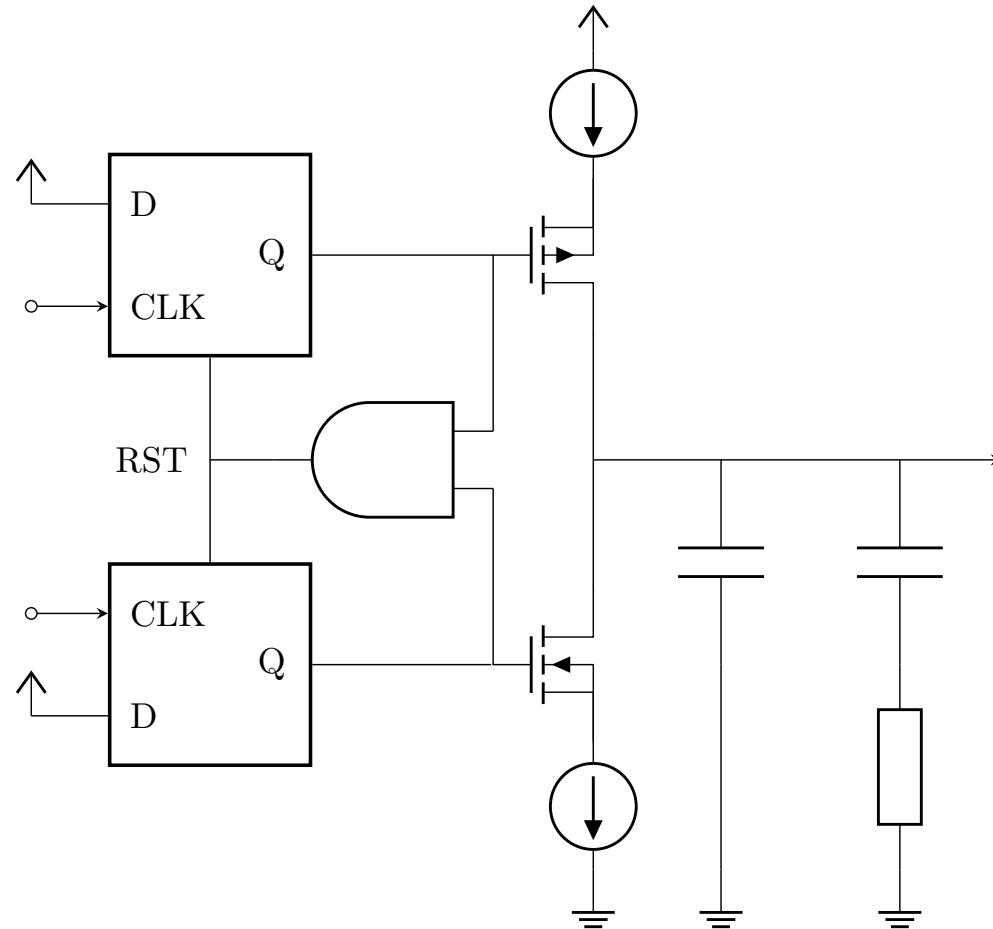
PLL: VCO: Layout



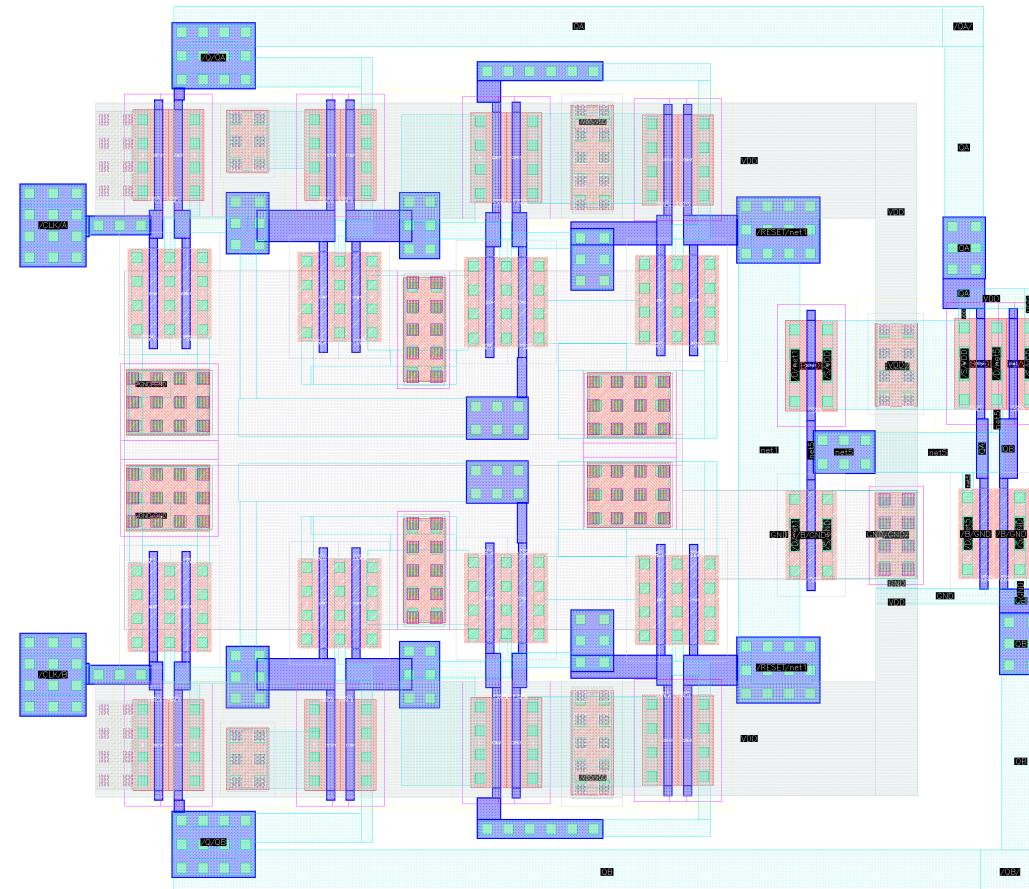
PLL: VCO: Simulation & Test Result



PLL: PFD & Charge Pump: Block Diagram

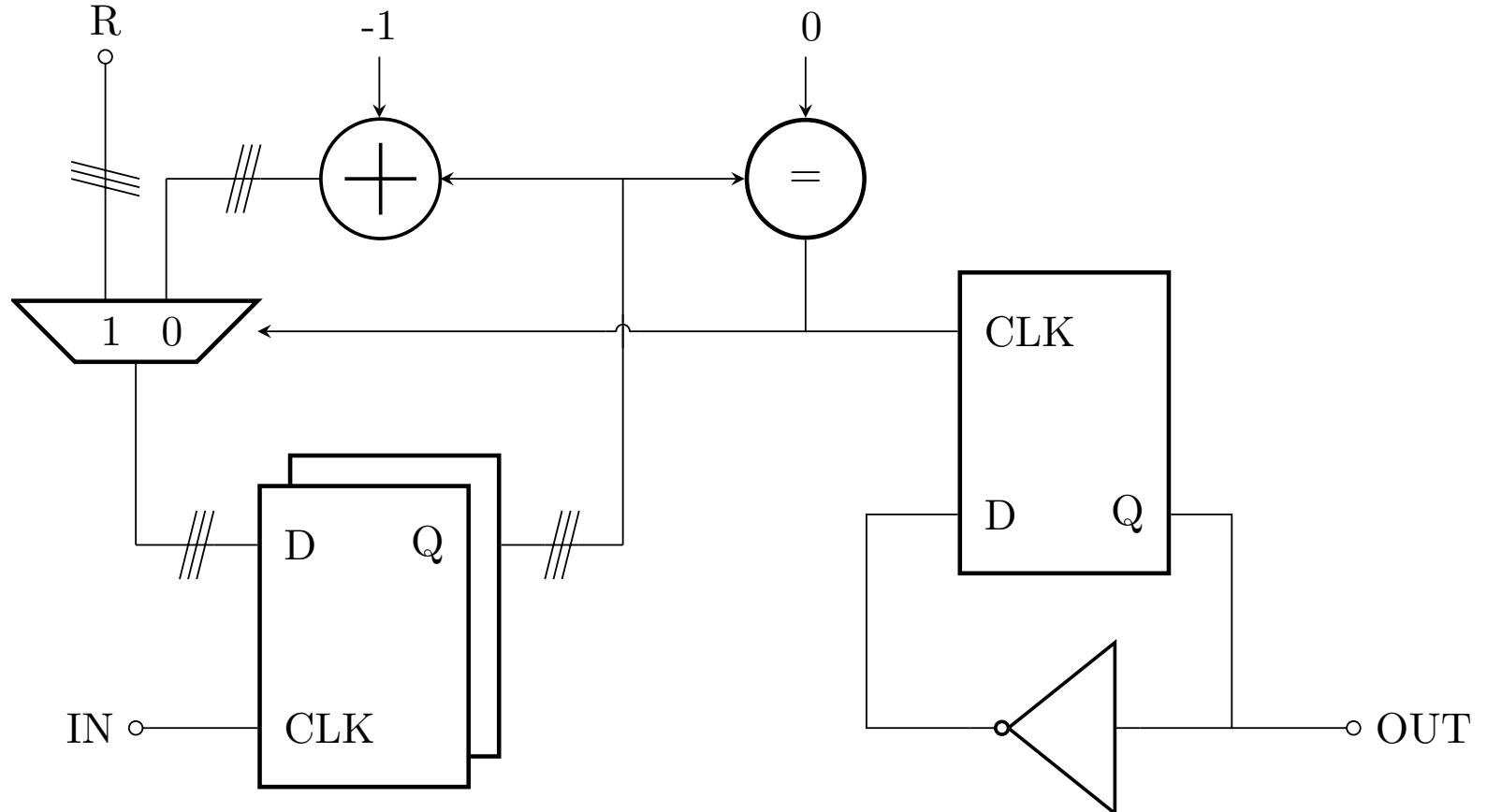


PLL: PFD & Charge Pump: Layout

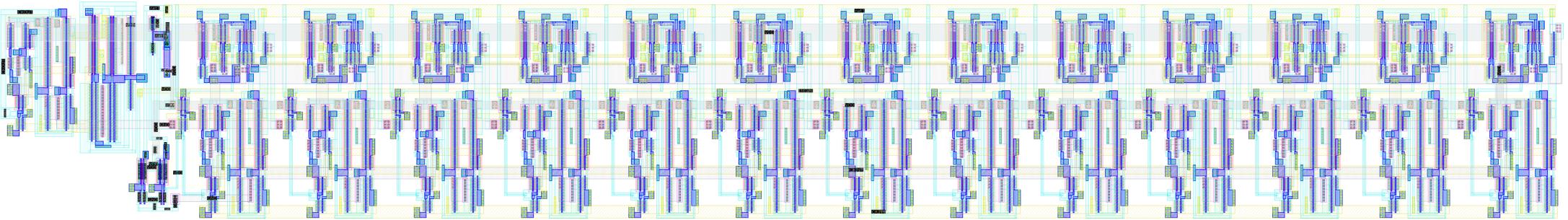


PLL: Divider: Block Diagram

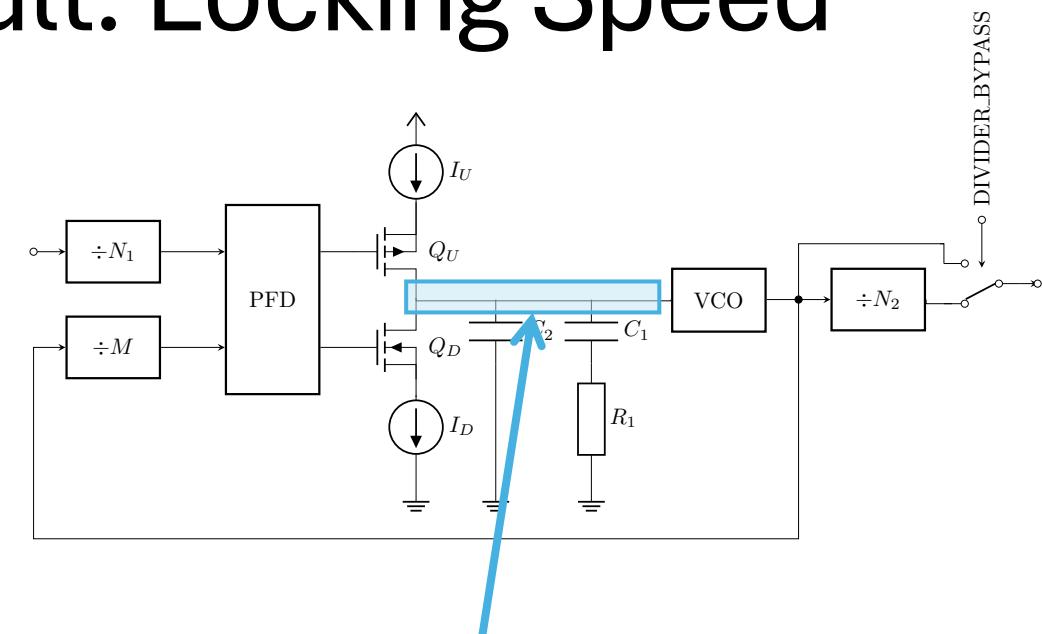
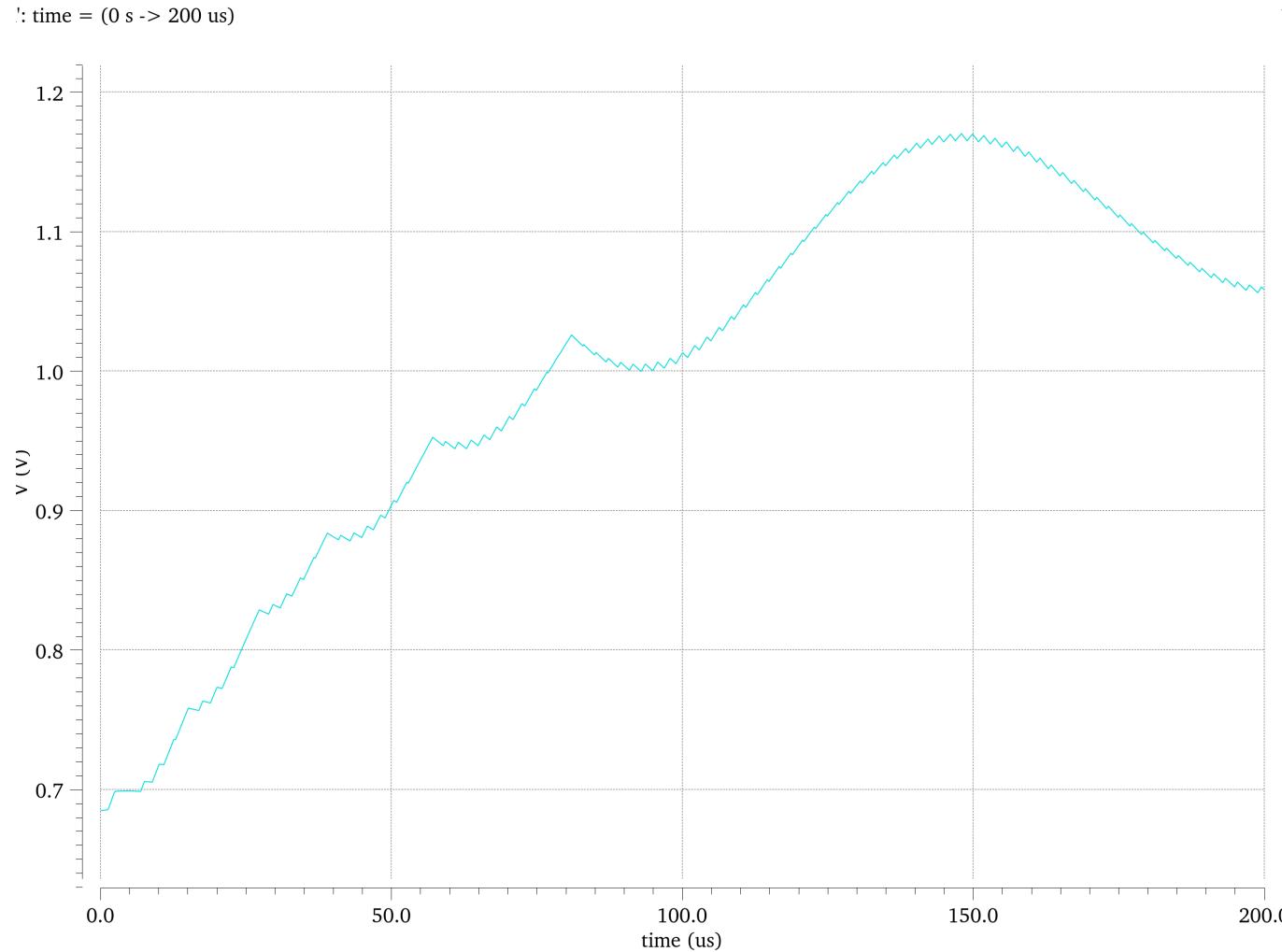
The divider is to divide the frequency by $2(R+1)$



PLL: Divider: Layout

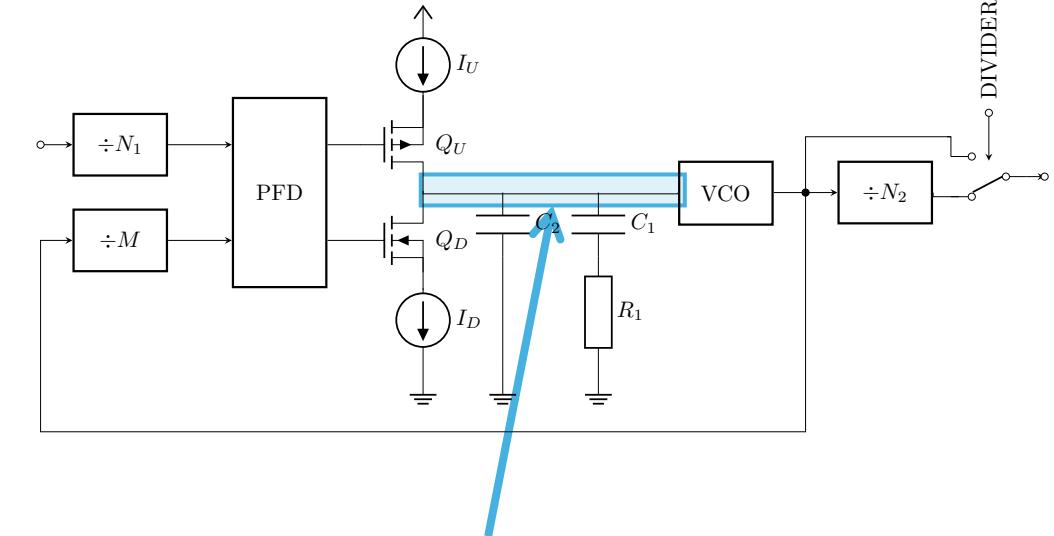
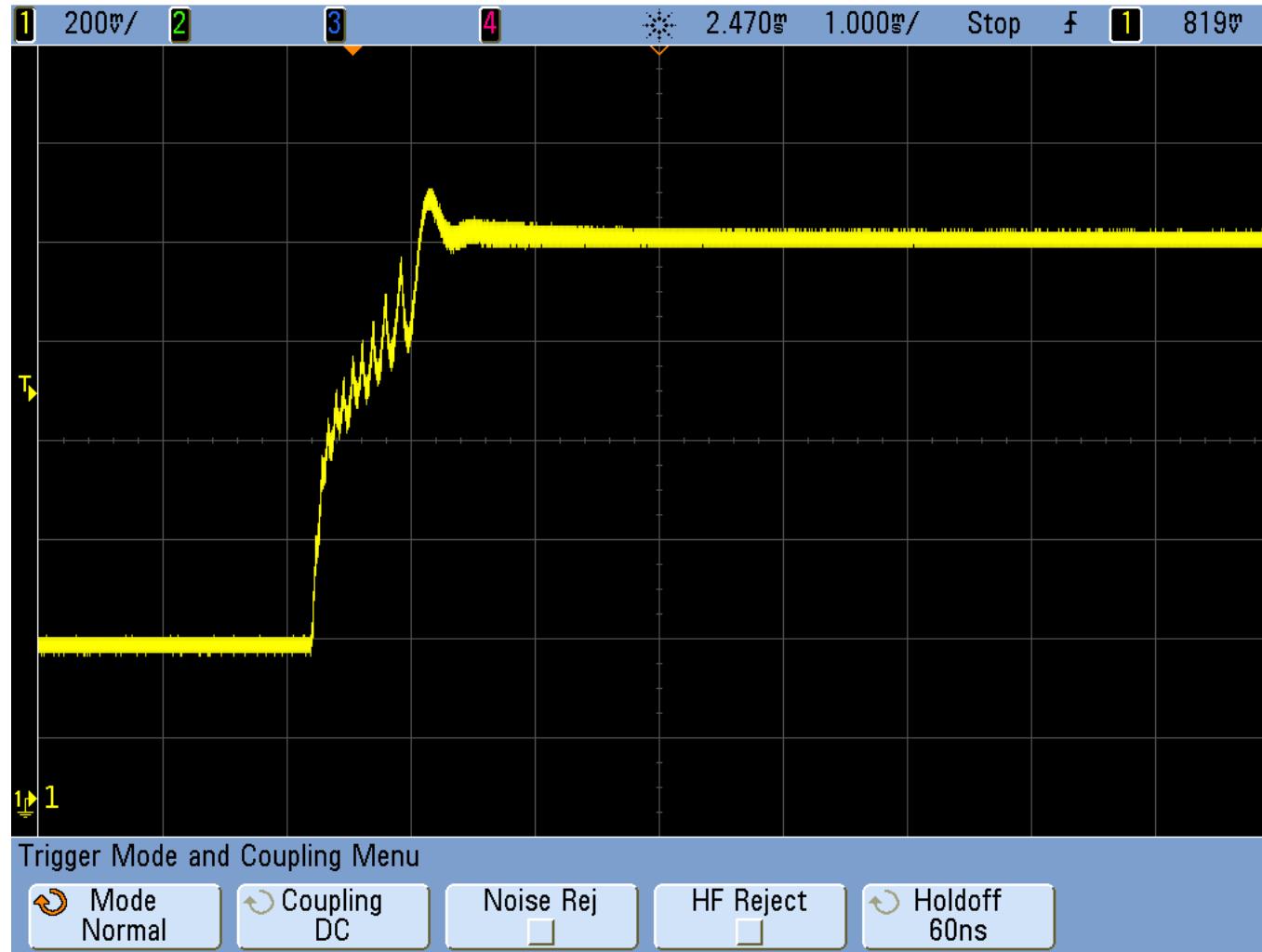


PLL: Test & Simulation Result: Locking Speed



The waveform shown is from this network

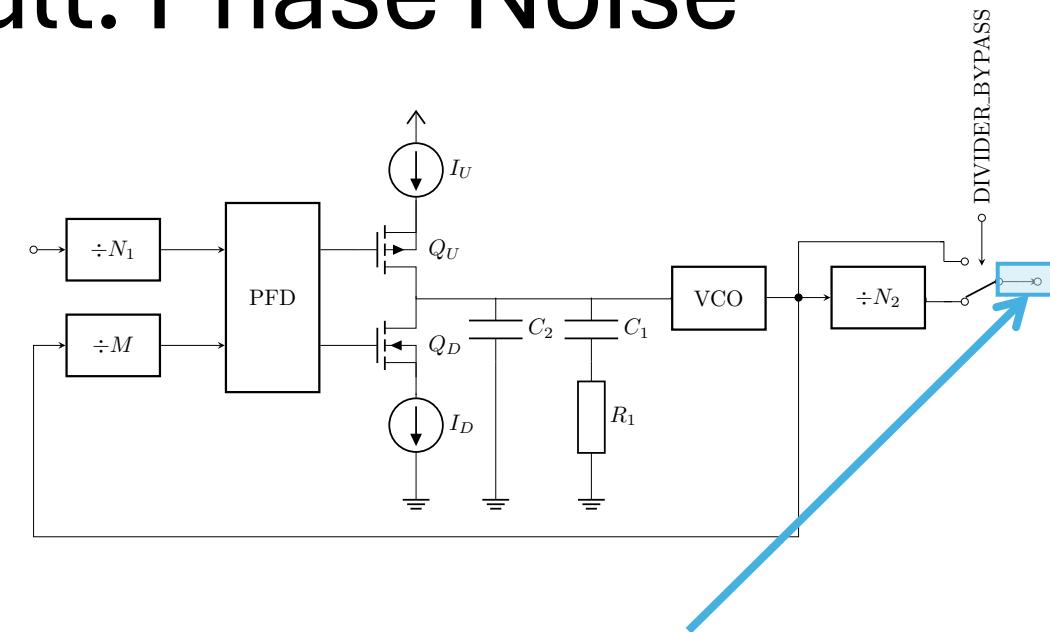
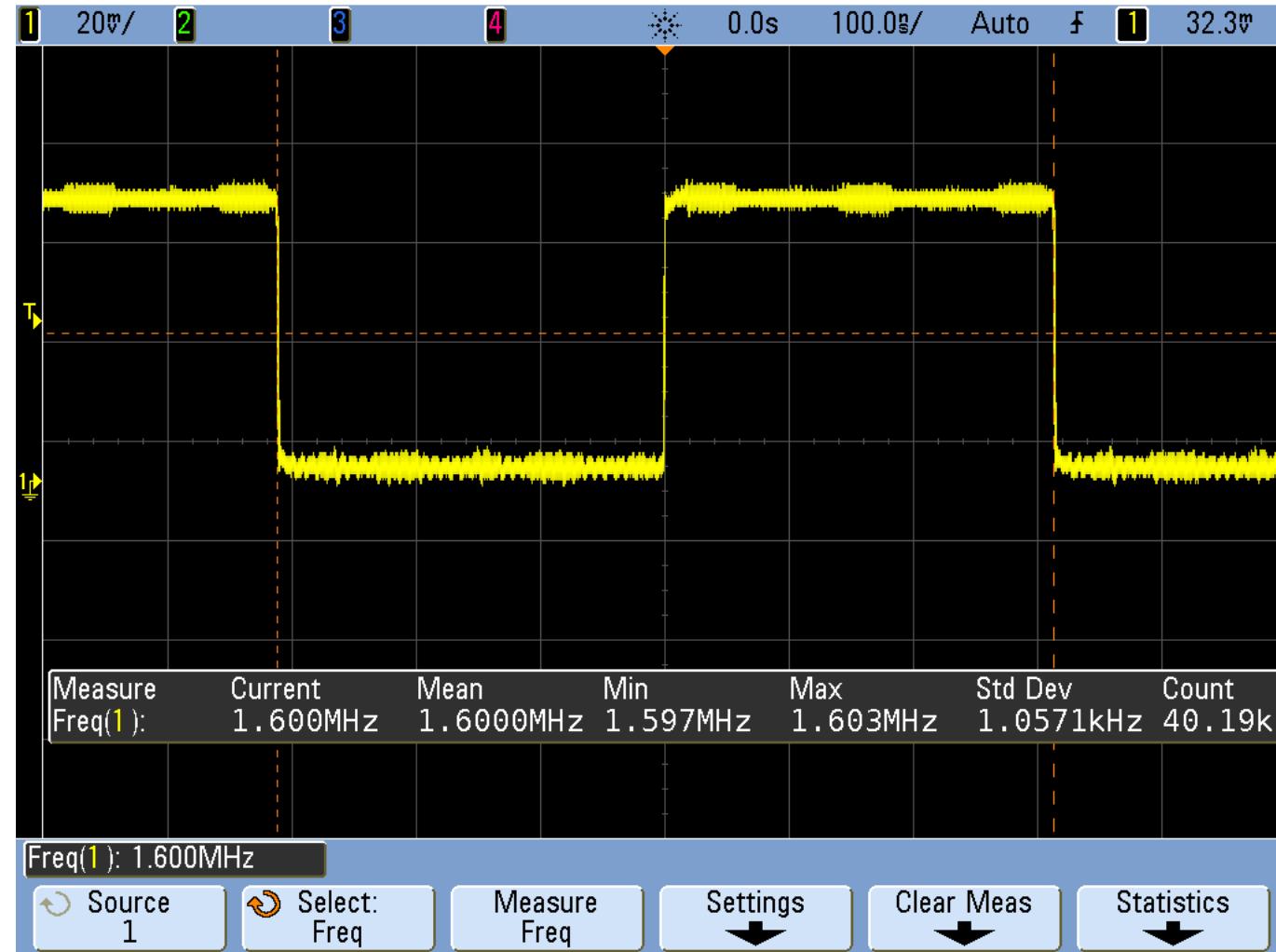
PLL: Test & Simulation Result: Locking Speed



The waveform shown is from this network

The locking time is about 1 ms.

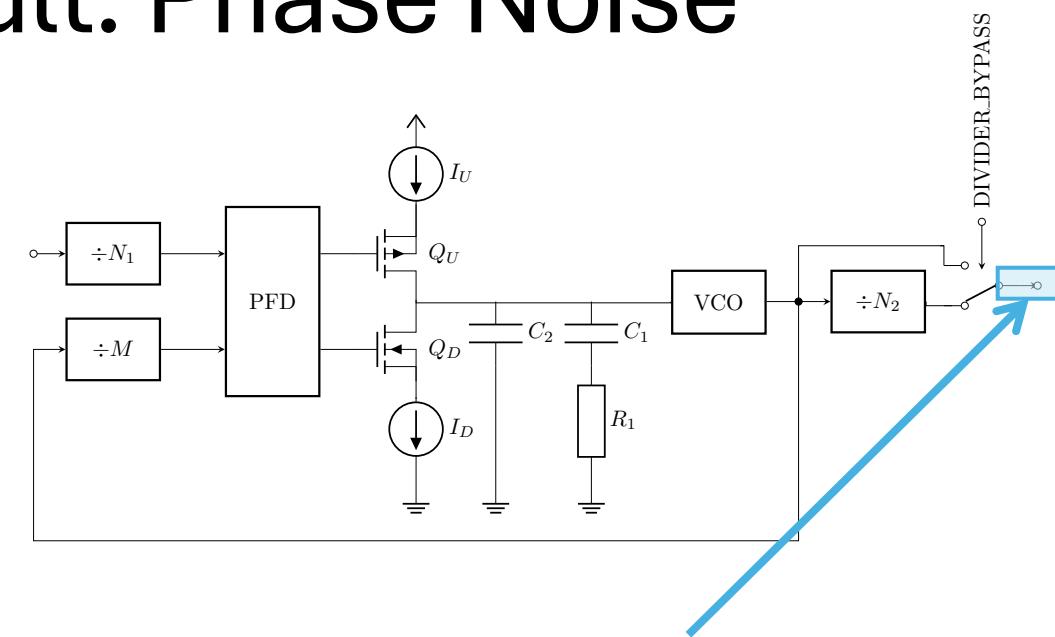
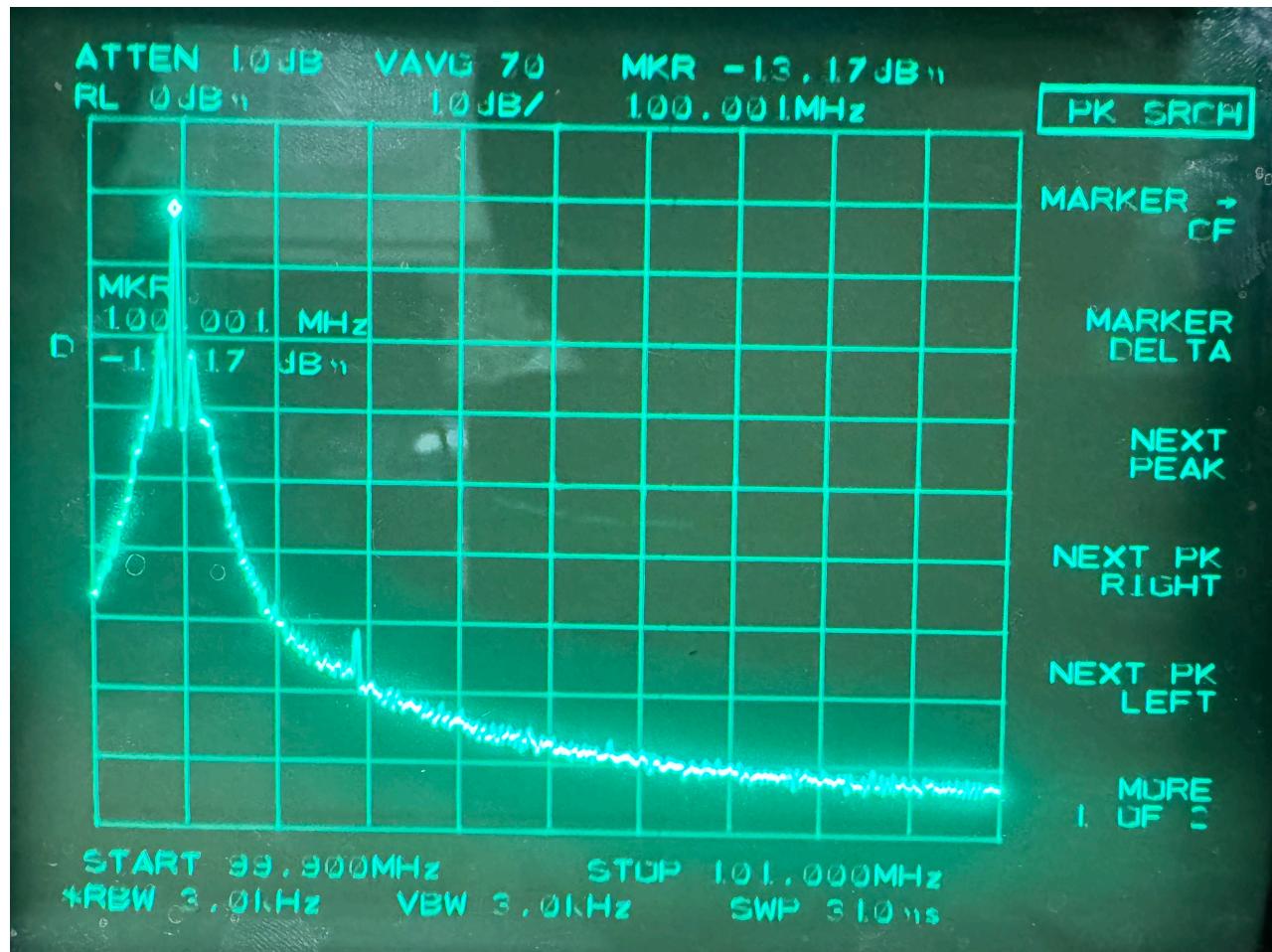
PLL: Test & Simulation Result: Phase Noise



The waveform shown is from this network

Offset (kHz)	Phase Noise (dBc)
0	0
1	-30.5
10	-31.5
100	-56.34
1000	-82.87

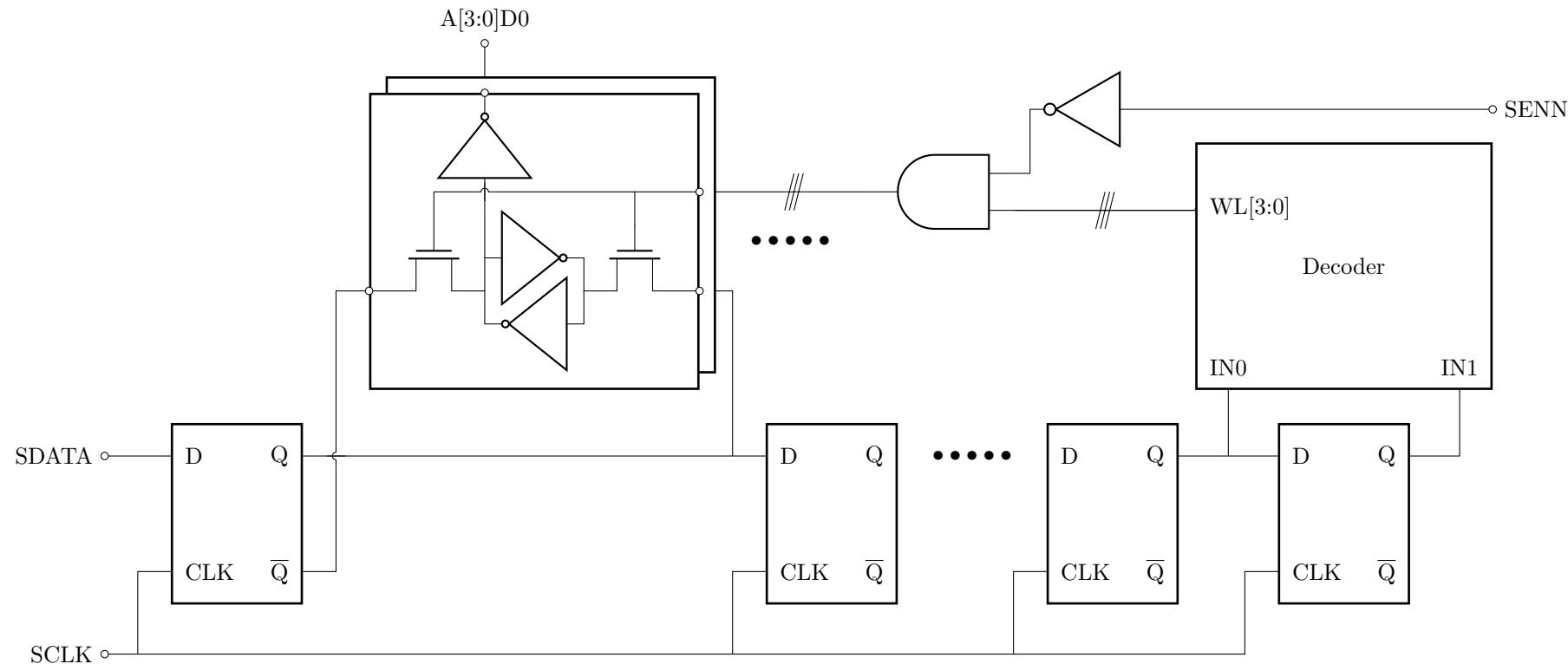
PLL: Test & Simulation Result: Phase Noise



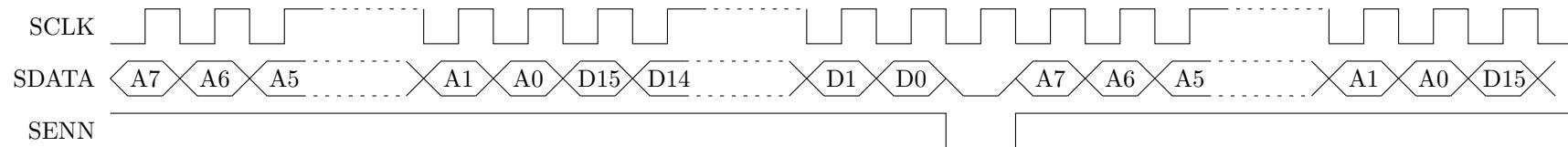
The waveform shown is from this network

Offset (kHz)	Phase Noise (dBc)
0	0
1	-30.5
10	-31.5
100	-56.34
1000	-82.87

Serial Input Memory: Block Diagram



Timing Diagram:



Serial Input Memory: Layout

