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Electronic Design Automation
CSE 215
Digital Access Control Finite State Machine
Project 3

Introduction

The purpose of this document is to illustrate the usage of Alliance tools to perform placement and routing to the digital access control finite state machine created and synthesized in project one and project two respectively.

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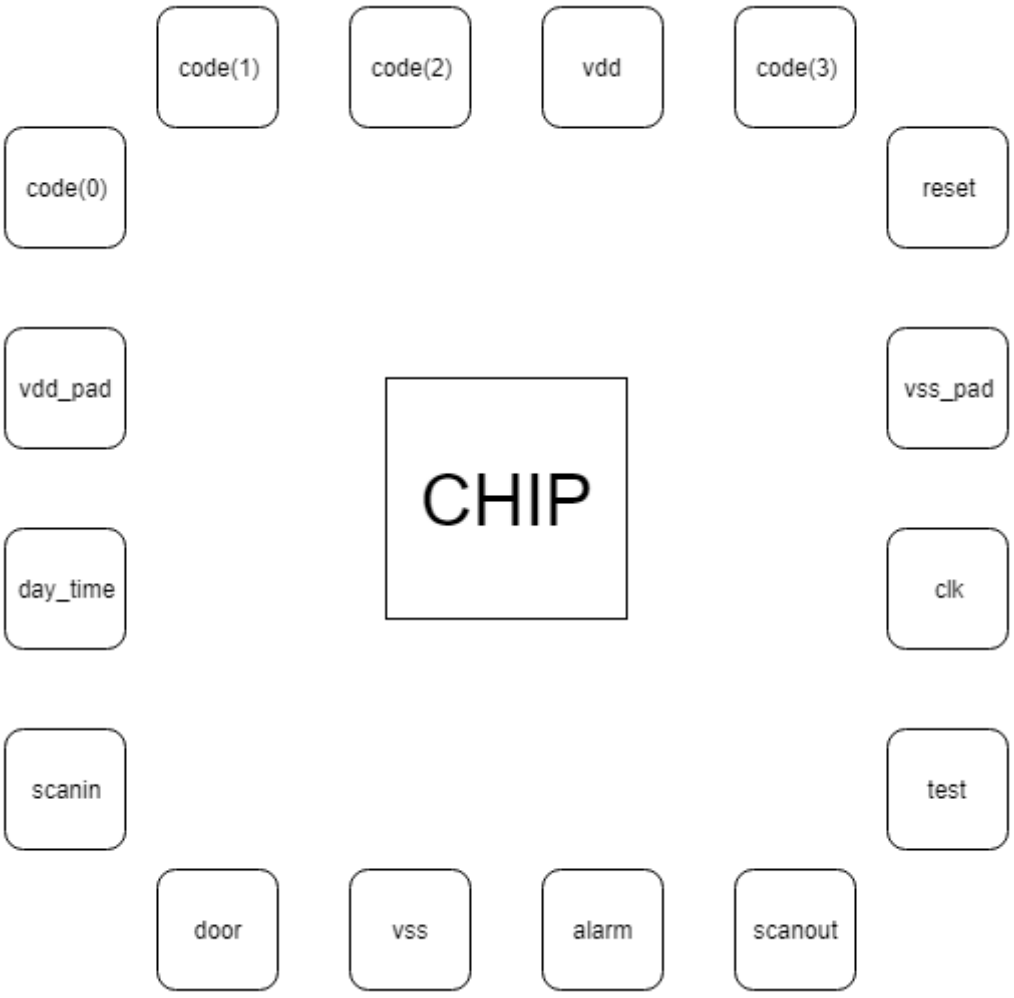
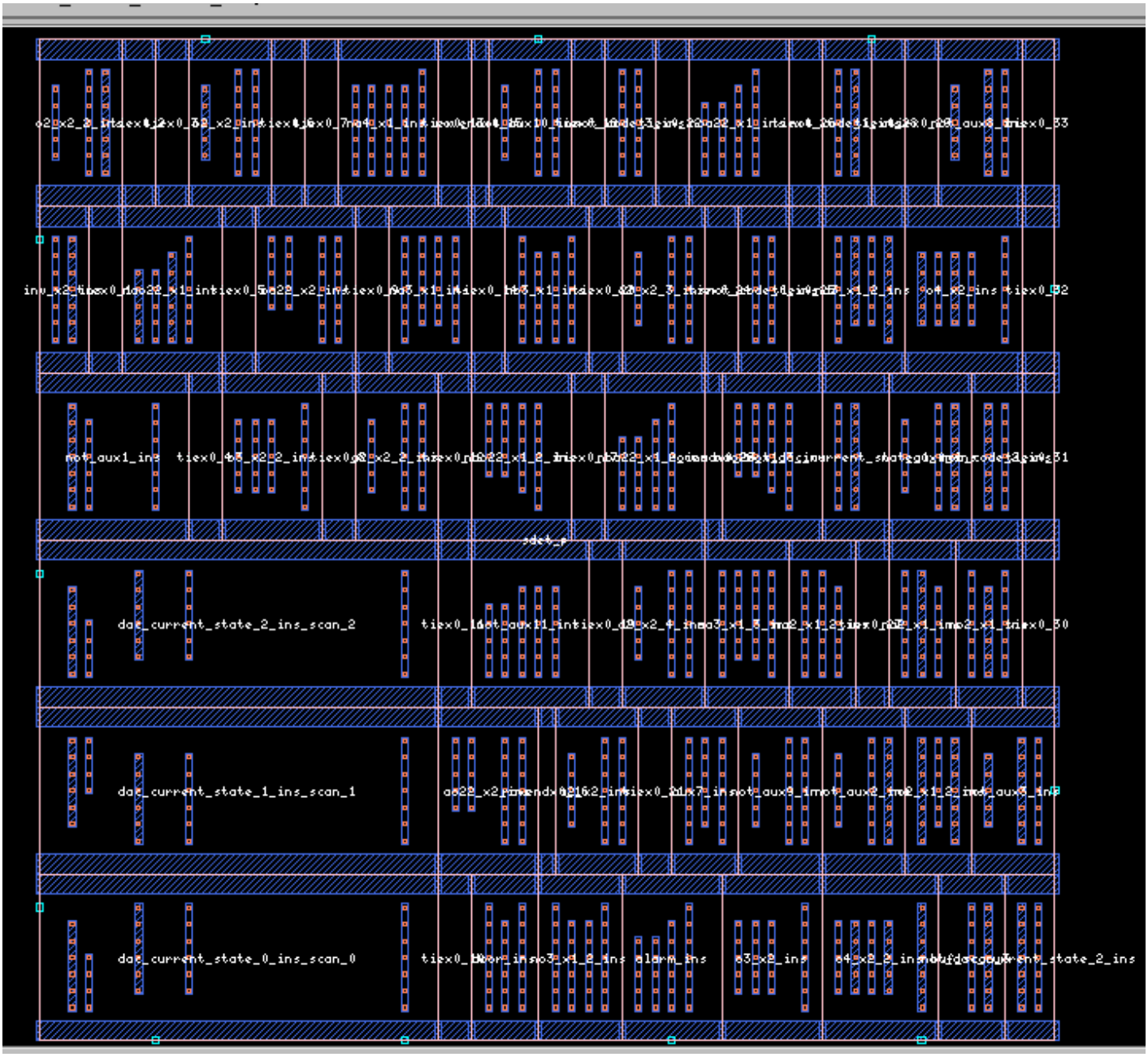
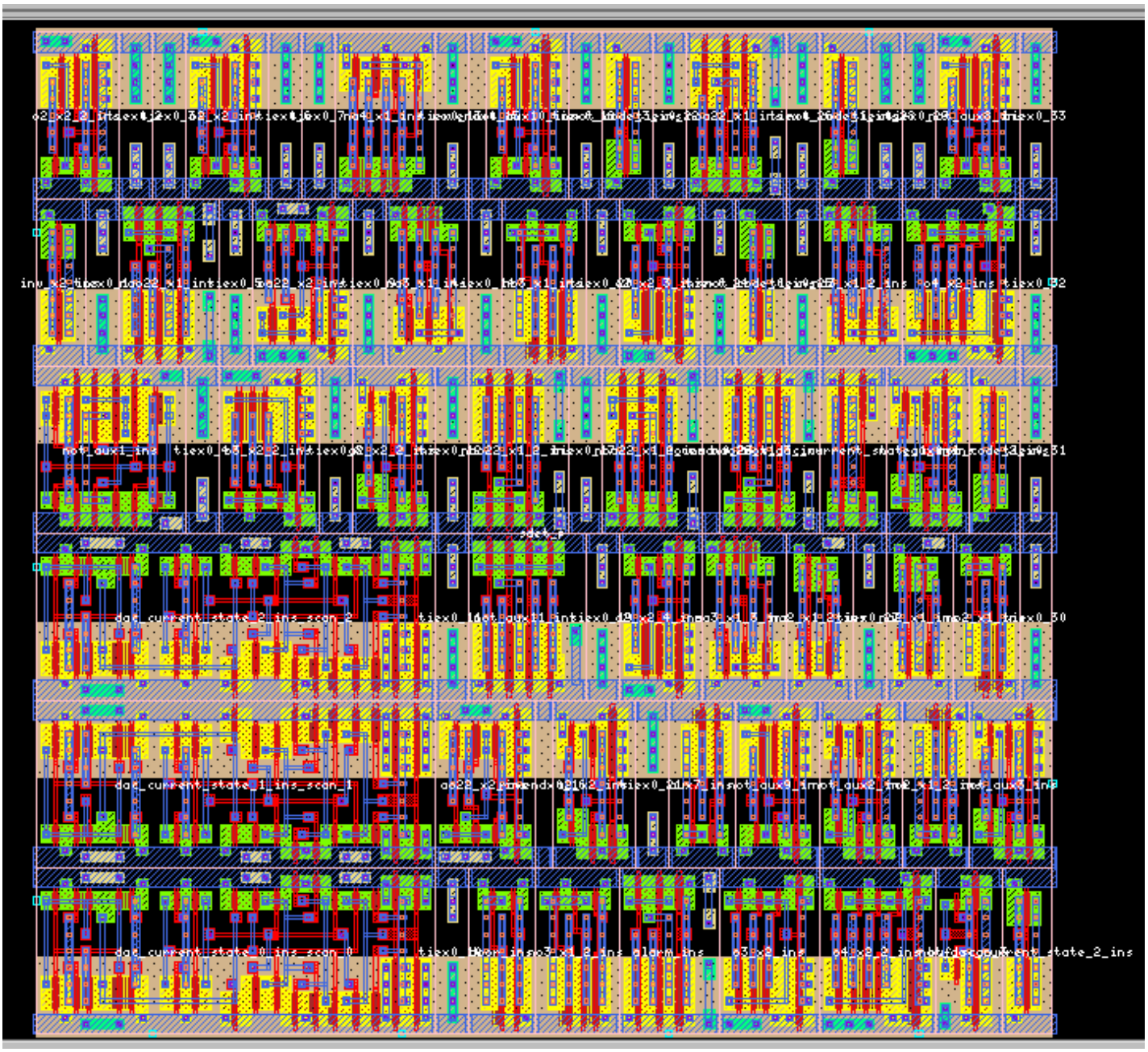
1- Pad Placement



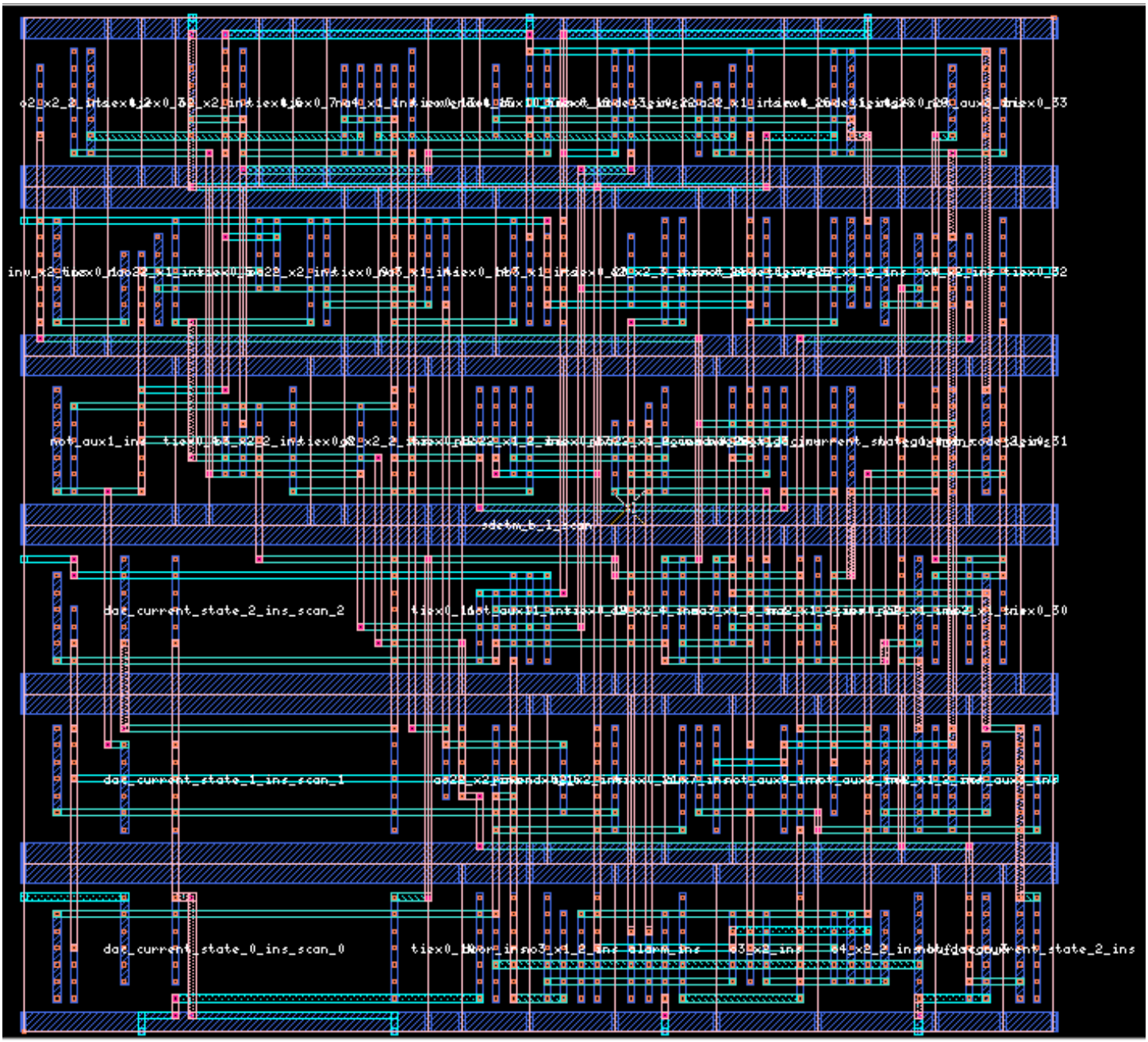
2- OCP Output Layout View using Graal



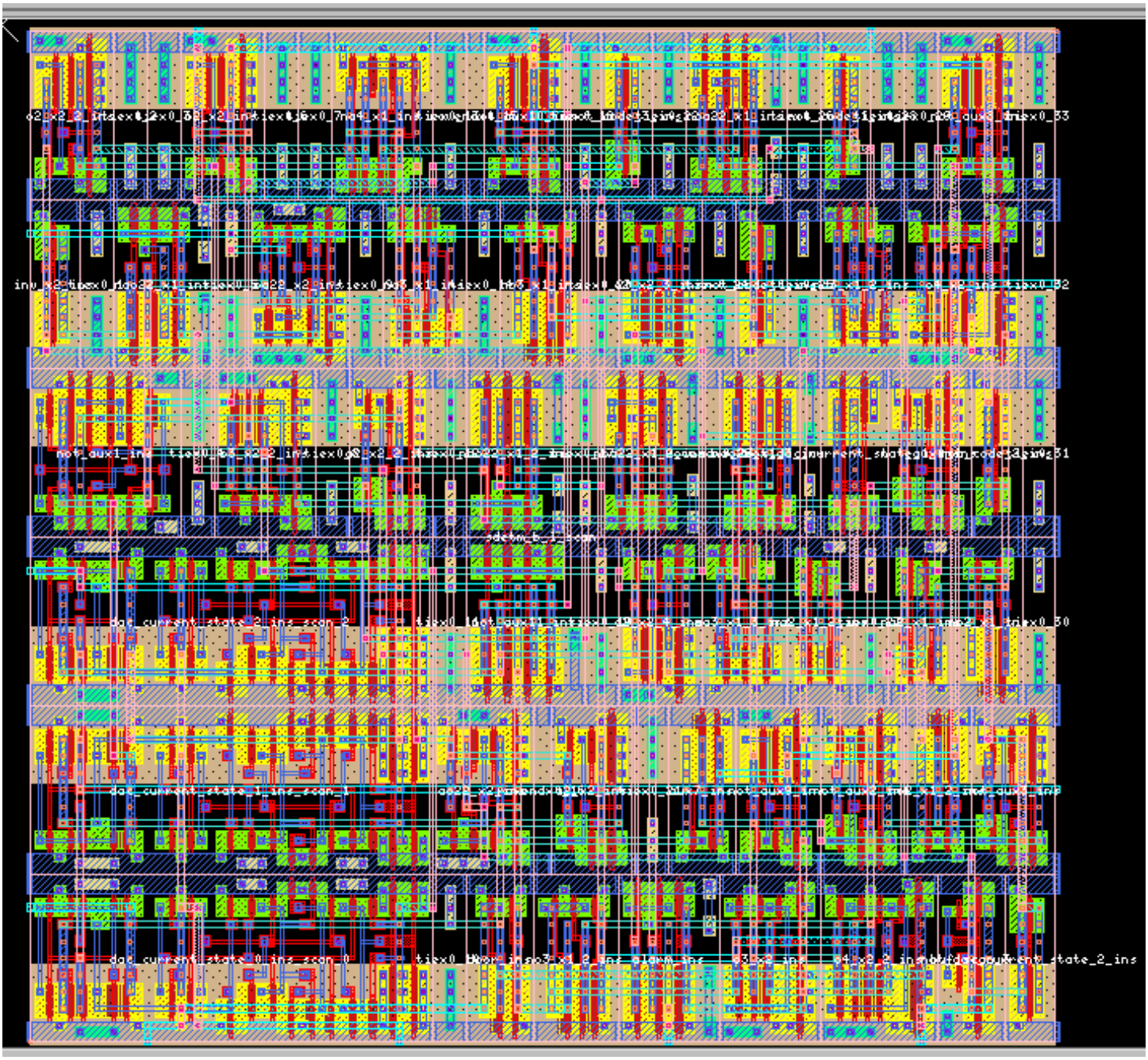
3- OCP Output Layout Flattened View using Dreal



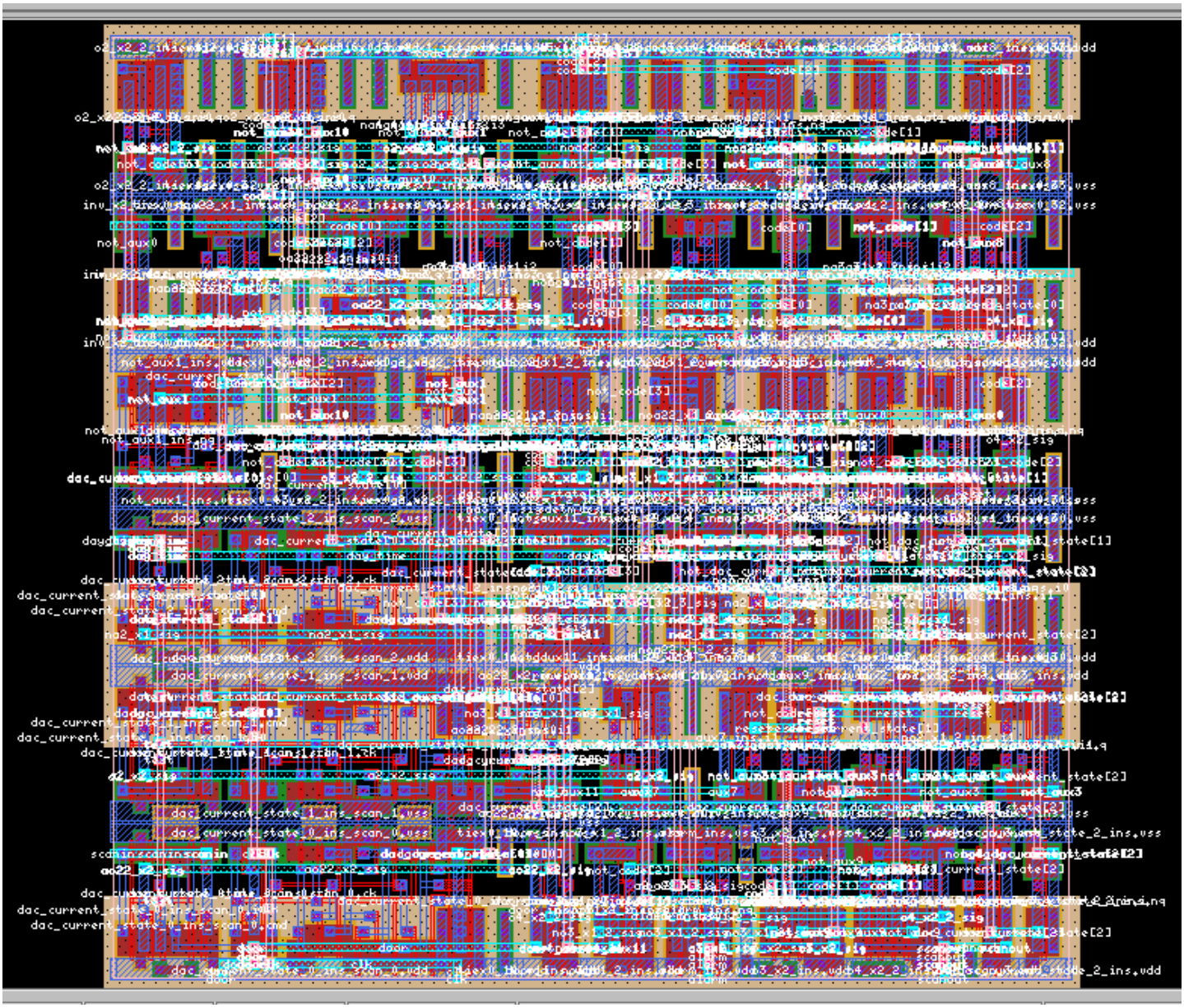
4- Nero Output Layout View using Graal



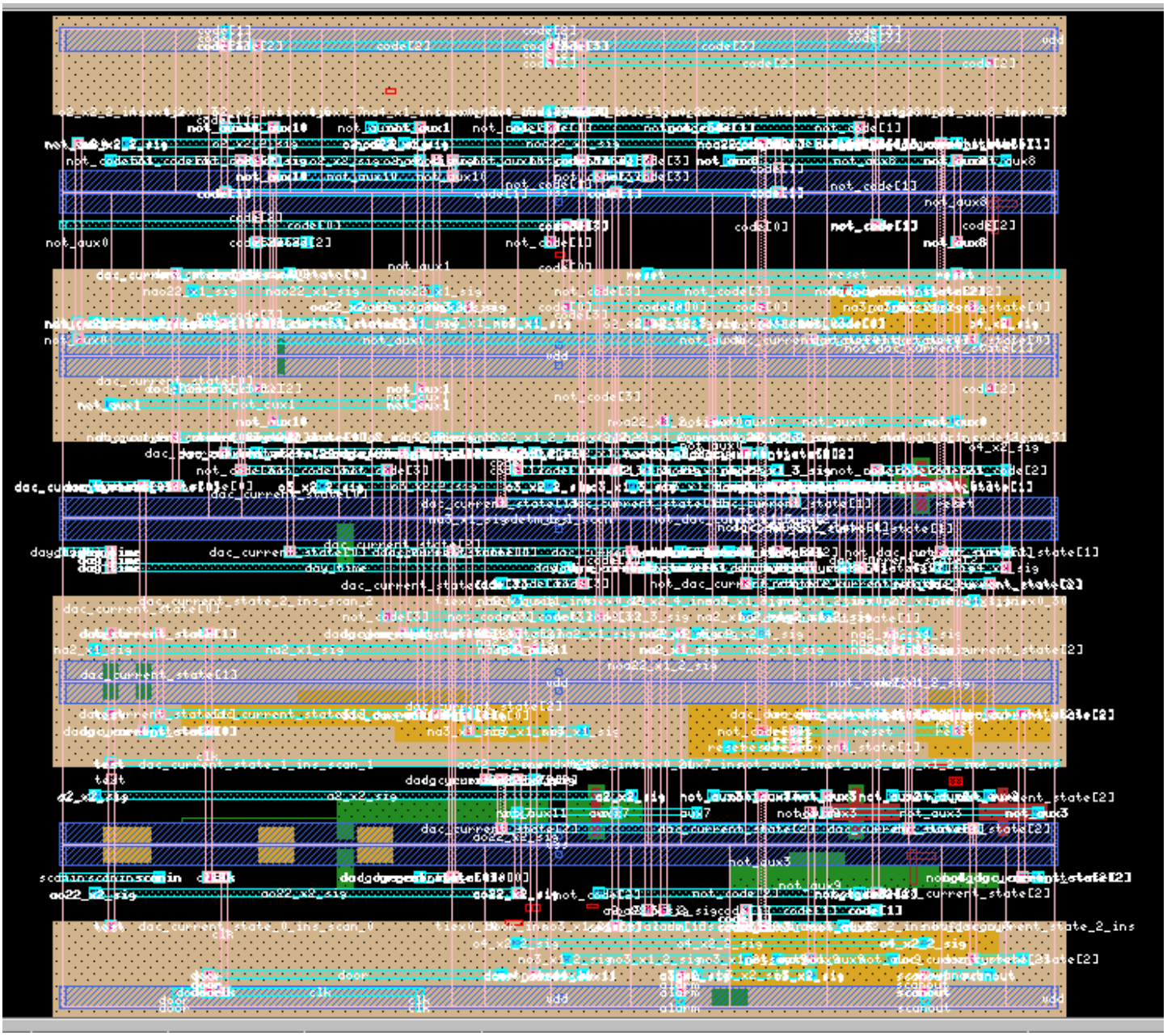
5- Nero Output Layout Flattened View using Graal



6- S2R Output Layout Flattened View using Dreal



7- S2R Output Layout View using Dreal



8- Appendix

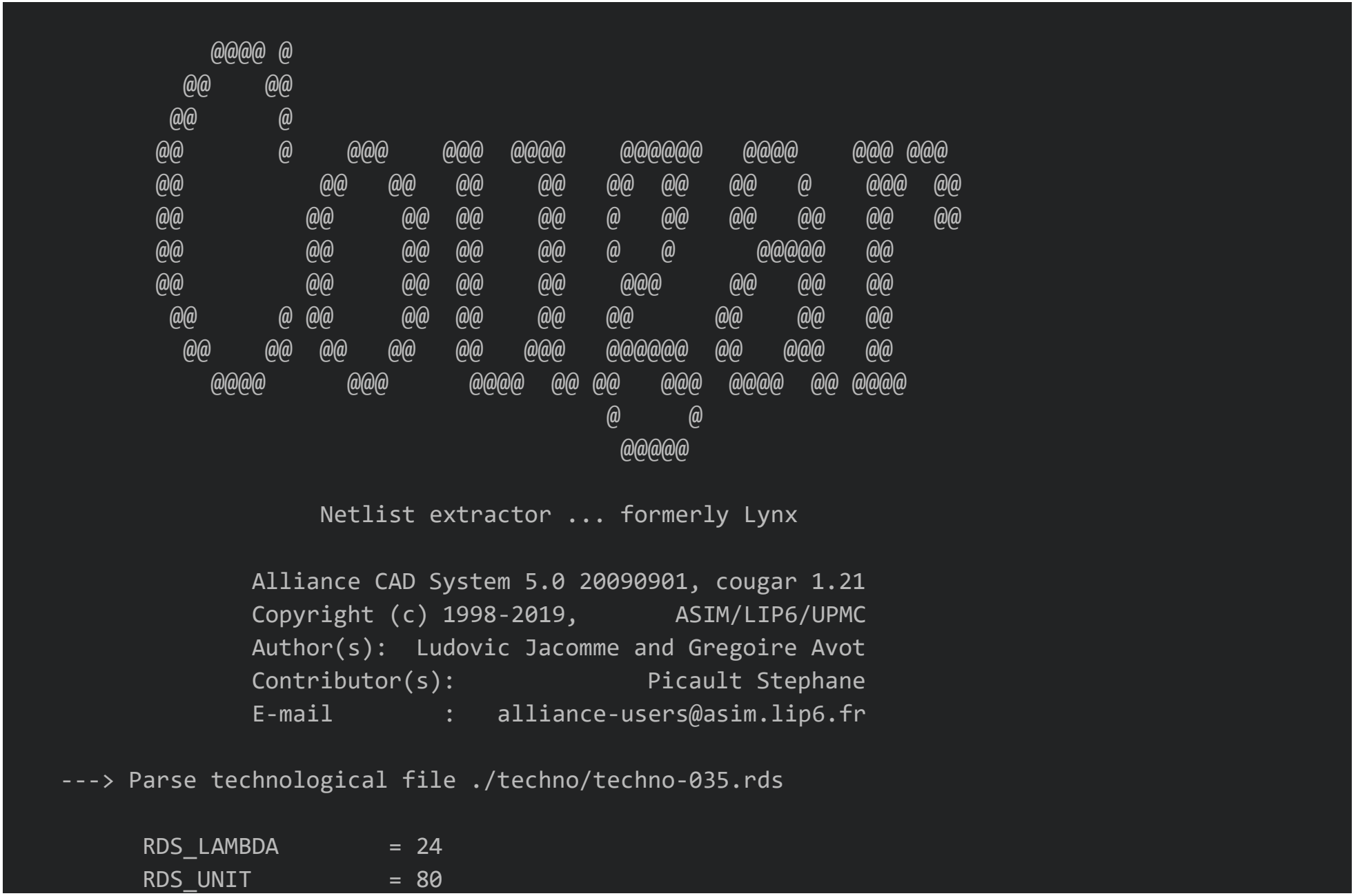
1- Makefile

```
sdetm_p.ap_ocp : sdet.ioc sdetm_b_l_scan.vst
    MBK_IN_LO=vst; export MBK_IN_LO; \
    MBK_OUT_PH=ap; export MBK_OUT_PH; \
    ocp -v -ring -ioc sdet sdetm_b_l_scan sdet_p > ocp.out

sdetm_b_l_scan.ap_nero : sdet_p.ap sdetm_b_l_scan.vst
    nero -V -p sdet_p sdetm_b_l_scan sdetm_b_l_scan > nero.out

%.al_cougar_lvx : %.ap
    MBK_OUT_LO=al; export MBK_OUT_LO; \
    RDS_TECHNO_NAME=./techno/techno-035.rds; \
    export RDS_TECHNO_NAME; \
    cougar -v $* > cougar_$*.out
    lvx vst al $* $* -f > lvx_$*.out

druc_core : sdetm_b_l_scan.ap
    RDS_TECHNO_NAME=./techno/techno-symb.rds; \
    export RDS_TECHNO_NAME; \
    druc sdetm_b_l_scan > druc_core.out

sdet_chip.cif : sdetm_b_l_scan.ap
    RDS_TECHNO_NAME=./techno/techno-035.rds; \
    export RDS_TECHNO_NAME; \
    RDS_OUT=cif; export RDS_OUT; \
    s2r -v -r sdetm_b_l_scan > s2r.out

_dreal : sdetm_b_l_scan.cif
    RDS_TECHNO_NAME=./techno/techno-035.rds; \
    export RDS_TECHNO_NAME; \
    RDS_IN=cif; export RDS_IN; \
    dreal -l sdetm_b_l_scan
```

2- .ioc file

```
LEFT(
   (IOPIN scanin.0 );
   (IOPIN day_time.0 );
   (IOPIN code(0).0 );    )
TOP(
   (IOPIN code(1).0 );
   (IOPIN code(2).0 );
   (IOPIN code(3).0 );    )
RIGHT(
   (IOPIN test.0 );
   (IOPIN reset.0 );    )
BOTTOM(
   (IOPIN door.0 );
   (IOPIN clk.0 );
   (IOPIN alarm.0 );
   (IOPIN scanout.0 );    )
```

3- Cougar logs



```
      RDS_PHYSICAL_GRID = 2
      MBK_SCALE_X       = 100

---> Extract symbolic figure sdetm_b_l_scan

    ---> Translate Mbk -> Rds

    ---> Build windows
    <--- 100

    ---> Rectangles    : 1613
    ---> Figure size   : (   -116,   -116 )
                         (  30616,  30116 )

    ---> Cut transistors
    <--- 0
    ---> Build equis
    <--- 65
    ---> Delete windows
    ---> Build signals
    <--- 65
    ---> Build instances
    <--- 82
    ---> Build transistors
    <--- 0
    ---> Save netlist

<--- done !
```

```
---> Total extracted capacitance
<--- 0.0pF
```

4- LVX logs

```
                    @@@@@@      @@@@    @@@ @@@@   @@@@
                      @@         @@      @   @@     @
                      @@         @@      @    @@   @
                      @@          @@    @      @@ @
                      @@          @@    @       @@
                      @@           @@  @        @@
                      @@           @@  @        @@@
                      @@            @@@         @  @@
                      @@      @     @@@        @    @@
                      @@     @       @        @      @@
                     @@@@@@@@@       @      @@@    @@@@

                           Gate Netlist Comparator

                  Alliance CAD System 5.0 20090901,   lvx 1.4
                  Copyright (c) 1992-2019,     ASIM/LIP6/UPMC
                  E-mail        : alliance-users@asim.lip6.fr



***** Loading and flattening sdetm_b_l_scan (vst)...

***** Loading and flattening sdetm_b_l_scan (al)...


***** Compare Terminals .............
***** O.K.  (0 sec)
```

```
***** Compare Instances ..........
***** O.K.  (0 sec)

***** Compare Connections ..............
***** O.K.  (0 sec)

===== Terminals .......... 14
===== Instances .......... 49
===== Connectors ......... 280


***** Netlists are Identical. ***** (0 sec)
```

5- Durc logs

```
                  @@@@@@@     @@@@@@@                    @@@@ @
                    @@   @@     @@   @@                 @@    @@
                    @@    @@    @@    @@               @@      @
                    @@     @@   @@    @@  @@@  @@@@  @@       @
                    @@     @@   @@   @@    @@    @@  @@
                    @@     @@   @@@@@      @@    @@  @@
                    @@     @@   @@  @@     @@    @@  @@
                    @@     @@   @@   @@    @@    @@  @@
                    @@    @@    @@   @@    @@    @@   @@      @
                    @@   @@     @@    @@   @@   @@@    @@    @@
                  @@@@@@@     @@@@@   @@@   @@@@  @@     @@@@

                              Design Rule Checker

                   Alliance CAD System 5.0 20090901,  druc 5.0
                   Copyright (c) 1993-2019,     ASIM/LIP6/UPMC
                   E-mail        : alliance-users@asim.lip6.fr

Flatten DRC on: sdetm_b_l_scan
Delete MBK figure : sdetm_b_l_scan
Load Flatten Rules : ./techno/techno-symb.rds

Unify : sdetm_b_l_scan

Create Ring : sdetm_b_l_scan_rng
Merge Errorfiles:
```

```
Merge Error Instances:
instructionCourante : 000     0     1     2     3     4     5     6     7     8     9    10
11    12    13    14    15    16    17    18    19    20    21    22    23    24    25    26
27    28    29    30    31    32    33    34    35    36    37    38    39    40    41    42
43    44    45    46    47    48    49    50    51    52    53    54    55    56
End DRC on: sdetm_b_l_scan
Saving the Error file figure
Done
8249

Some errors have been detected, see file: sdetm_b_l_scan.drc for detailled
```