# Project (2) Implementing EDF Schedular

### 1 Verifying the implementation using analytical methods

## **Calculating the System Hyperperiod**

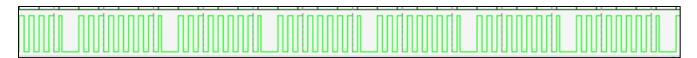
System hyperperiod = 100 msec

### **Calculating the CPU load**

#### Method (1):

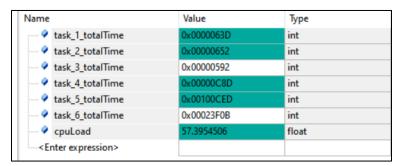
The CPU load can be calculated from the idle task as follows:

- The time the idle task was called during the hyperperiod = 1 \* 3 + 8 \*5 = 43 msec
- Idle task utilization = 43/100 = 0.43
- CPU utilization = 1 Idle task utilization = 57%



#### Method (2)

The CPU load is also calculated using the trace hook as shown below. It is found that it is as the one that is calculated analytically (in the previous section)



### Method (3)

Using the run-time analysis (shown below), it is found that the CPU load is approximately equals those calculated in the previous 2 methds

ART_Tx	4507	<1%
Load_2	44151	6%
IDLE	300417	42%
UART_Rx	1064	<1%
Button_1	299	<1%
Button 2	302	<1%
Load 1	350887	50%

# 2 CHECKING SYSTEM SCHEDULABILITY USING URM

The following table represents the execution time for each task calculated using the

Task Name	Execution time (msec)	Period (msec)	Task Utilization
T1 (button_1)	0.018	50	0.00036
T2 (button_2)	0.018	50	0.00036
T3 (UART_Tx)	0.015	100	0.00015
T4 (UART_Rx)	0.04	20	0.002
T5 (load_1)	5	10	0.5
T6 (Load_2)	12	100	0.12
Total Tasks utilization			0.623

Table 1: Tasks properties

- Utilization bound =  $n(2^{1/n} 1) = 0.735$
- $0.623 < 0.735 \rightarrow$  The system is schedulable

# 3 TIME DEMAND ANALYSIS

Referring to table 1, the time demand is calculated for each task as follows

1. Task (5) (Load-1) (Highest Priority Task)

Deadline	10
The time provided (msec)	5
(5 < 10) → Task (5) is schedulable	

03365

2. Task (4) UART Receiving Task

Deadline	20
The time provided (msec)	0.04 +(20/10) * 5 = 10.04
10.04 < 20 → Task (4) is schedulable	

3. Task (1): button (1) task

The time required (msec)	50
The time provided (msec)	0.018 + (50/10) * 5 + (50/20) *0.04 = 25.118
25.118 < 50 → Task (1) is schedulable	

4. Task (1): button (1) task

25.138 < 50 → Task (2) is schedulable	
The time provided (msec)	0.018 + (50/10) * 5 + (50/20) *0.04 + 0.018 = 25.136
The time required (msec)	50

### 5. Task (3): UART Transmitter

The time required (msec)	100
The time provided (msec)	0.015 + (100/10) * 5 + (100/20) * 0.04 + (100/50) *
	0.018 + (100/50) * 0.018 = 50.287
50.287 < 100 → Task (3) is schedulable	

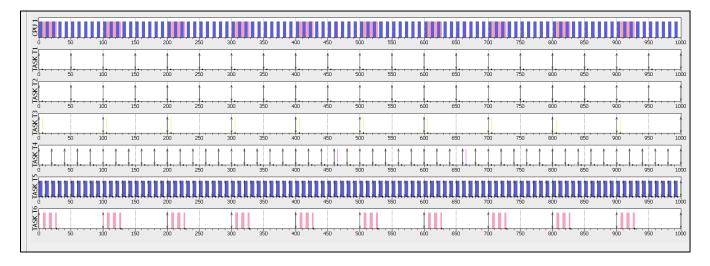
### 6. Task (6): Load - 2

The time required (msec)	100
The time provided (msec)	12 + (100/10) * 5 + (100/20) * 0.04 + (100/50) * 0.018 + (100/50) * 0.018 = 62.272
62.272 < 100 → Task (6) is schedulable	

It is concluded that the system is schedulable.

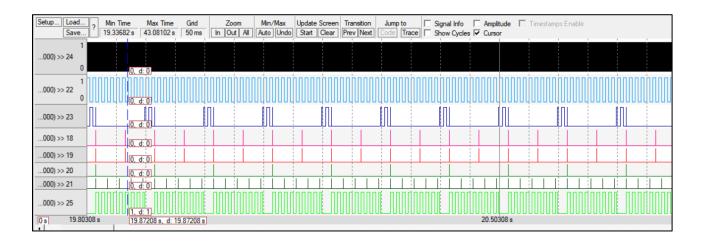
# 4 SIMSO

It is confirmed from the Simso that none of the tasks misses its deadline.



# 5 Verification using Keil simulator in run-time

## 5.1 CPU USAGE TIME USING TIMER 1 & TRACE MACROS



Drawing color	Task
	Tick
	Load (1)
	Load(2)
	Task 1 (button - 1)
	Task 2 (button - 2)
	UART Transmitter task
	UART Receiver
	Idle task

The CPU load is verified using the trace Macros as shown below:

