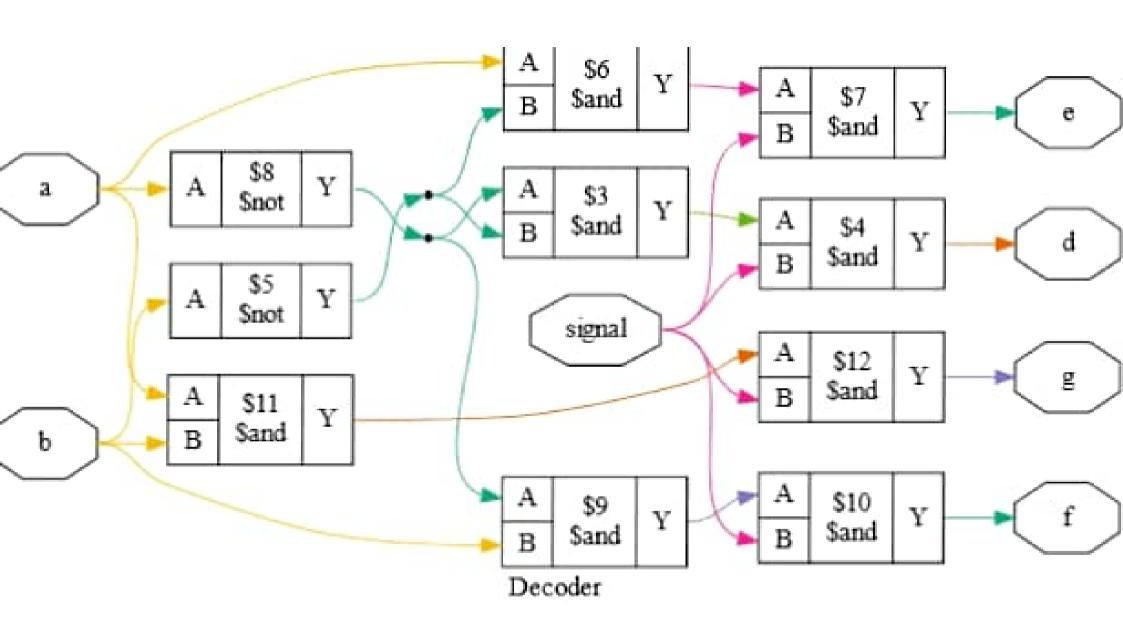
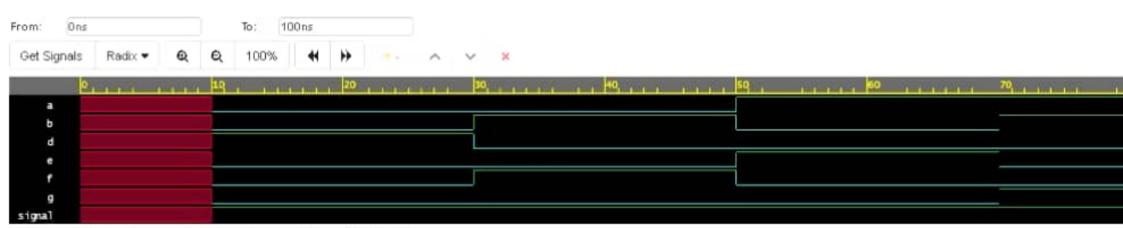
```
1 // Code your design here
 //Design module
 module Decoder (input wire a,
                 output wire
                 output wire
                 output wire
                 output wire
               (~a) & (~b) & signal;
                      (b)
                  & (b) & signal;
```

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```
// Code your testbench here
   // or browse Examples
   //test bench
4
  module dec_tb();
5
     reg a,b, signal;
8
     wire d.e.f.g:
8
     Decoder dec(.a(a).
0
                   b(b);
10
                   signal (signal);
11
12
                   .e(e),
13
14
                   .a(a)
15
                  'n
16
17
     initial
18
       begin
19
20
          #10
21
          a=1'b0; b=1'b0; signal = 1'b1;
22
          #20
23
          a=1'b0: b=1'b1: signal= 1'b1;
24
          #20
25
          a=1'b1: b=1'b0: signal= 1'b1:
28
27
          #20
          a=1'b1; b=1'b1; signal= 1'b1;
28
29
             #10
30
       end
34
     initial
32.1
33
       begin
          $dumpfile("dump.vcd");
34
         $dumpvars():
35 -
          #100
36
37
    $finish:
38 end
39 endmodule
40.3
```

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Note: To revert to EPWays opening in a new browser window set that option on your user name