

# An analog approach to compensate for OpAmp offset and finite gain in SC circuitry: A case study of a cyclic RSD ADC

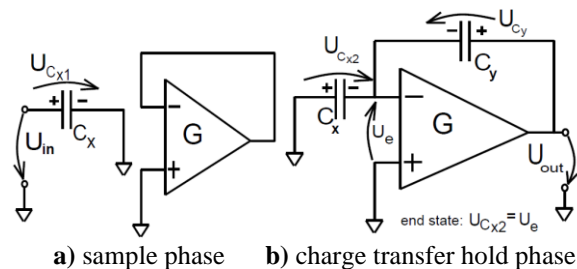
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**Abstract:** Design of high-resolution Nyquist rate A/D converter necessitates the usage of advanced circuit techniques to compensate for arising analog errors. In switched capacitor ADC, besides the well know techniques such as bottom plate sampling, mismatch-independent and redundant (RSD: 1.5bit/stage) conversion for the elimination of charge injection, capacitor mismatch, comparator and offset sensitivity, respectively, the most utilised circuit techniques are those for OpAmp's offset and finite gain errors cancellation. An alternative technique for compensation of the errors due to finite gain and offset of Opamp in SC circuits is proposed. This novel method features a charge addition and is compared to so far used approaches based on voltage addition [1],[2]. The concept and the results of a 5V CMOS implementation of cyclic RSD ADC with ratio-independent SC technique using this correction method are discussed.

**Key words:** cyclic/algorithmic analog-digital converter, switched capacitor circuit, amplifier's finite gain and offset.

## Introduction.

The most crucial design task of cyclic (algorithmic) and pipeline A/D converters (ADC) is the realization of an accurate multiplication by a factor of 2 for every bit cycle (loop gain = 2) or between every pipeline stage (inter-stage gain = 2), respectively, to complete the straight-forward division algorithm after each bit comparison [3]. The capacitance mismatch problem in switched-capacitor (SC) realizations can be avoided by the well known capacitance ratio-independent SC technique, e.g. [1]. However, the finite gain of an operational amplifier in every SC circuitry pushes the overall loop gain below the accurate value. In the case of a loop gain slightly lower than 2 (e.g. 1.95) an often used approach is digital calibration. Recently, [1],[2] introduced an effective approach of analog compensation for OpAmp-caused errors, the offset and the finite gain (G). The approach is based on sensing these errors in terms of voltage difference at the Op-Amp input and subsequently compensating the error by a voltage addition at the OpAmp input. We propose a different principle whereas the correction is performed by adding a charge amount (charge addition compensation), which allows a more precise adjustment of error cancellation.

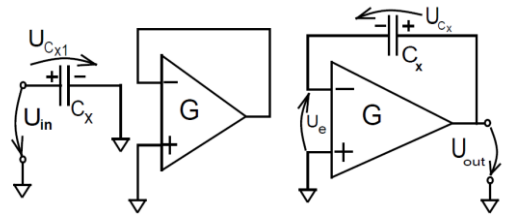


**Fig.1:** Origin of SC errors due to OpAmp's finite gain. In a settled state, the impact of OpAmp's offset and finite gain cause a loss sustained charge transfer from the sampling ( $C_x$ ) to the integration ( $C_y$ ) capacitor. This effect is caused by a remaining non-zero differential voltage at the input ( $U_e = U_{out} / G$ ), thus some

charge remains on  $C_x$  in the hold phase (Fig. 1b). Additionally, the same voltage  $U_e$  raises another error. The voltage which appears at the OpAmp's output is not the full voltage over the integration capacitance  $C_y$ , but is reduced by  $U_e$ . Both errors together can be ascertained from the charge balance equation (1) in the case of a charge transfer between  $C_x$  and  $C_y$  (Fig.1):

$$U_{out} = (U_{in} - U_e) \cdot \frac{C_x}{C_y} - U_e = U_{in} \cdot \frac{C_x}{C_y} - U_e \left( 1 + \frac{C_x}{C_y} \right) \quad (1)$$

Given that  $C_x = C_y$  (integrator with gain = 1), the error amounts to  $2 \cdot U_e$ , which can be compensated for by means of an auxiliary charge  $Q_k = 2 \cdot U_e \cdot C_x$  (2)



**Fig.2:** OpAmp's finite gain error in a ratio-independent sample-and-hold (S&H) switched capacitor circuit.

In the case of a ratio-independent SC S&H circuit with just a single  $C_x$  capacitor being reconnected into the feedback (Fig.2), the error share coming from non-ideal charge transfer does not arise. The only remaining error is due to the  $U_e$ -reduced output voltage

$$U_{outSH} = U_{Cx} - U_e = U_{in} - U_e \quad (3)$$

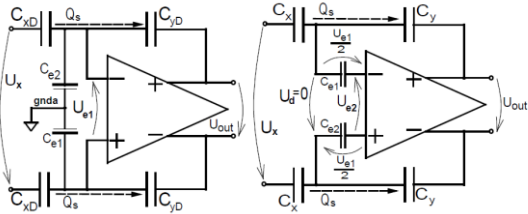
which can be compensated for by half the charge amount compared to (2):  $Q_{kSH} = U_e \cdot C_x$ . Mostly, the SC correction is based on error-sensing capacitors ( $C_e \approx C_x$ ), which will, however, withdraw from the working capacitors a charge similar to the error which

impedes a true correction. Therefore, common to all correction principles the error ( $U_{e1}$ ) must be determined in an earlier “predictive” phase, which simulates the actual load conditions using dummy capacitors ( $C_{xD}, C_{yD}$ ). The measured voltage  $U_{e1}$  is being used in the subsequent integration phase for the  $U_{e2}$ -error compensation. Despite of similar feedback circuitry in both phases, but due to additional prediction phase’ loading by  $C_e$  the error voltage  $U_{e2}$  is non-significantly larger than  $U_{e1}$ :

$$U_{e2} = U_{e1} \cdot (1 + \varepsilon) \quad \text{with} \quad \varepsilon = \frac{\sum C_e}{C_y} \cdot \frac{1}{G} \ll 1 \quad (4)$$

### Correction by voltage addition.

The correction approach in [1],[2] is likewise suitable for sampling (Fig.2) as well as for charge transfer SC integration (Fig.1). The error voltage stored on the  $C_e$ -capacitors is being reconnected serially and polarity-inversely into the OpAmp’s input paths and the error this way compensated. New virtual ground nodes with  $U_d = (U_{e2} - U_{e1}) \approx 0$  arise (see Fig. 3b). This way the whole charge from  $C_x$  can be transferred into  $C_y$  and at the same time the complete voltage drop over  $C_y$  occurs at the OpAmp’s output without any loss. The value of sensing  $C_e$  does not have any arithmetical influence on the correction algorithm.



a) error measure phase      b) compensation phase

**Fig.3:** Voltage addition based SC error compensation.

### Correction by charge addition.

In the innovative charge addition based correction the value of  $C_e$  is essential. This principle is particularly suited for fully differential circuitry and so will be explained here. During the predictive phase, both measuring capacitors  $C_{e1} = C_{e2}$  will be charged in shunt (Fig. 4a) up to the full differential voltage at the OpAmp’s input:

$$Q_e = U_{e1} \cdot (C_{e1} + C_{e2}) = 2 \cdot U_{e1} \cdot C_e \quad (5)$$

In the correction phase every  $C_e$  will be reconnected between the OpAmp’s input and the analog ground (midpoint potential  $V_{cm}$ ), as shown in Fig. 4b. In the initial moments of this phase, due to the parallel-serial switching of  $C_e$  capacitors a voltage doubling at the OpAmp’s inputs arises ( $2U_{e1}$ ). However, in the stable state OpAmp’s input differential voltage settles to a value of  $U_{e2}$ , impressed by amplifier’s degenerative feedback and the finite gain  $G$ . Thereby half of the charge  $2 \cdot U_{e1} \cdot C_e$  calculated in (5) is being transferred to both integration capacitors  $C_y$ , which compensates

the error. The exact calculation of the correction charge  $Q_k$  transferred into  $C_y$  in the case of  $C_{e1} = C_{e2} = C_e$  follows

$$Q_k = 2 \cdot C_e \cdot \left( U_{e1} - \frac{1}{2} U_{e2} \right) \quad (6)$$

This charge increases the voltage drop  $U_{Cy}$  additionally by a value

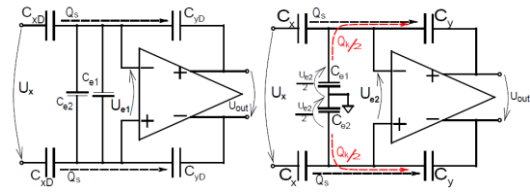
$$U_k = 2 \cdot \frac{C_e}{C_y} \cdot \left( U_{e1} - \frac{1}{2} U_{e2} \right) \quad (7)$$

To completely compensate for all arising errors this voltage  $U_k$  has to be equal to the error term in eq. (1):

$$2 \cdot \frac{C_e}{C_y} \cdot \left( U_{e1} - \frac{1}{2} U_{e2} \right) = U_{e2} \cdot \left( 1 + \frac{C_x}{C_y} \right) \quad (8)$$

and a general formula for the  $C_e$ -value can be derived:

$$C_e = (C_x + C_y) \cdot \frac{U_{e2}}{(2U_{e1} - U_{e2})} \quad (9)$$



a) error measure phase      b) compensation phase

**Fig.4:** Charge addition based SC error compensation.

Assuming the idealisation that  $U_{e1} \approx U_{e2} \approx U_e$  results in a sizing  $C_e \approx C_y + C_x$  for an integrating SC amplifier in Fig.1. If  $U_{e2} > U_{e1}$  (e.g. low amplifier gain  $G < 60$  dB or large charge withdraw into  $C_e$ ), the error compensation can be fine tuned by choosing  $C_e$ -value slightly larger than  $(C_y + C_x)$  in eq. (9). With  $U_{e2} = U_{e1} \cdot (1 + \varepsilon)$  from equation (4) follows:

$$C_e = 2 \cdot C_x \cdot \frac{1 + \varepsilon}{1 - \varepsilon} = 2 \cdot C_x \cdot (1 + \varepsilon') \quad (10)$$

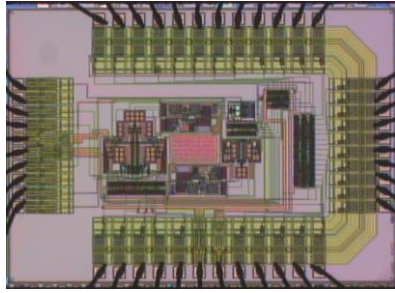
with  $\varepsilon' \ll 1$ . In our design procedure for the cyclic ADC the exact assignment for  $\varepsilon'$  has been made by transistor-level simulation, which allowed us to compensate additionally for other charge leakage originating from some second order effects.

Proceeding with the error calculation we can establish a relative error quotient  $\delta_r$  dependence on the OpAmp gain  $G$  and capacitance ratio  $\alpha = C_e/C_x$ , for  $C_y = C_x$ :

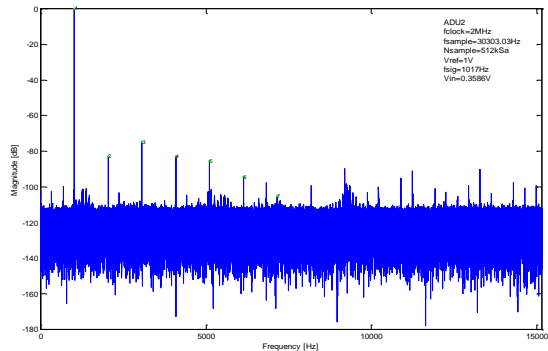
$$\delta_r = \frac{\Delta U_{out}}{U_{out}} = \frac{U_{out} - \frac{C_x}{C_y} U_{in}}{U_{out}} = \frac{G\alpha - 2\alpha^2 - 6\alpha - 4 - 2G}{G(4\alpha + 2 + G)} \quad (11)$$

Choosing an OpAmp’s gain, e.g. 80 dB, and demanding the error to be zero ( $\delta_r = 0$ ), yields the exact value for  $\alpha = C_e/C_x = 2.002403$ . By designing the error ca-





**Fig.6:** Chip photograph of the 2<sup>nd</sup> ADC prototype in 0.6µm CMOS X-FAB process in 1.3 mm<sup>2</sup> chip die.

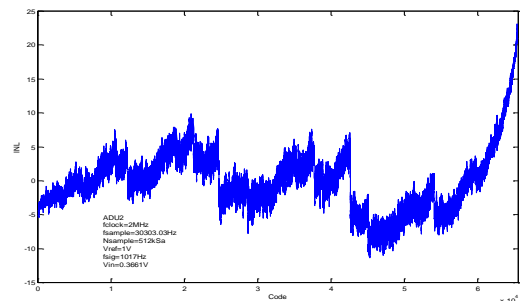


**Fig.8:** Spectral plot of the 2<sup>nd</sup> ADC for 1kHz sinus and 2MHz clock (30.3kS/s) and full-scale input (1V) featuring 66.34 dBc SINAD and -74.36 dBc THD.

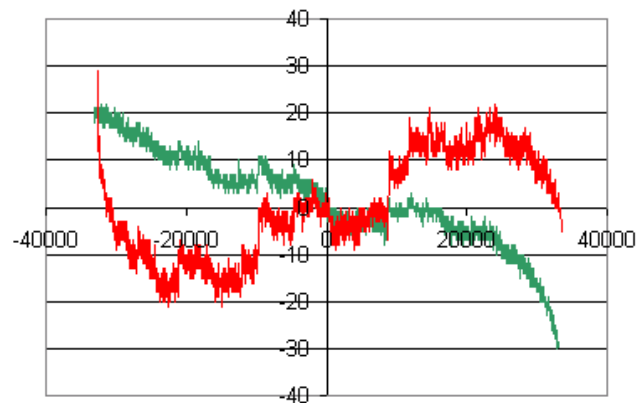
### Analysis and achieved results

The correction principle employed in the second ADC prototype proved functional as soon as the first dynamic and static measurements were taken. The characterisation of the ADC took place down to 16bit-level resolution. The charge based analog correction improves the suppression of harmonic distortion, so that the original THD of -69.8 dB changes to -74.4 dB, thus positively affects the overall ADC performance by increasing the SINAD (Noise & Distortion) from 65.77 dB to 66.8 dB, as shown in Fig. 8 at corresponding test set-up. This corresponds to an effective resolution of 10.8 bit. Furthermore, as the noise floor (SNR = 67.6 dB) represents the lower

bound for increasing this ADC's accuracy it is to be expected that a noise optimisation centred redesign would further improve the ADC. The integral non-linearity (INL) is found to meet the requirements for a 12-bit level accuracy within  $\pm 0.5$  LSB, as shown in Fig. 9. Static measurements not only show a lessening of non-linear distortion but also a reduction of the ADC's offset from initial 300 – 600 LSB units down to only 20 LSB units when using analog correction.



**Fig.9:** INL plot at identical test set-up to Fig. 8.



**Fig.10:** Comparison of LSB-error plots (beside a curve slope, the nonlinearity and the offset included,) while analog correction On (green) and Off (red).

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