

MRAM in 2024 – How we got there?

- Panel Discussion Chair: Satoru Araki, Sr.Dir, Prog/Prod Mgmt, Spin Transfer Technologies
- Goal: Visualize what we can expect, and what we need to work on
- Panelists:
 - Tom Coughlin President Coughlin Associates
 - Tom Andre VP Engineering Everspin Technologies
 - Andy Walker VP Product SpinTransfer Technologies
 - Jack Guedj CEO Numem
 - Jean-Pierre Nozieres CEO Antaios
 - Hiroaki Yoda Sr. Fellow Toshiba
 - Tetsuo Endoh Prof & Dir CIES, Tohoku Univ



MRAM in 2024

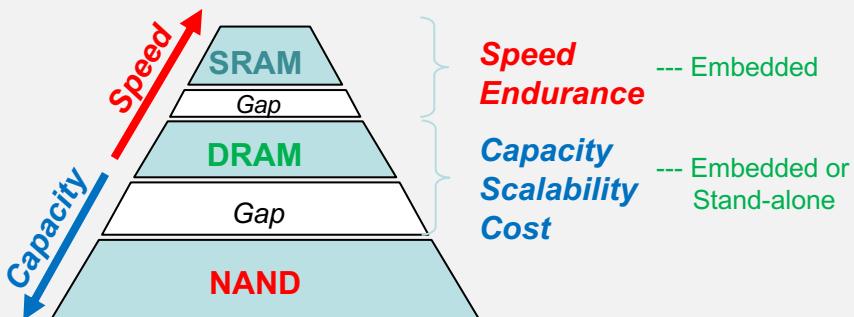
- What is the main segment for MRAM in 2024?
- Which application / market will drive it?
- What are the challenges?
- What technological breakthrough needed?

Two major domains for MRAM

Hierarchy: can MRAM fill in these gaps, or replace them?

Applications: three growing targets

Hierarchy



Application

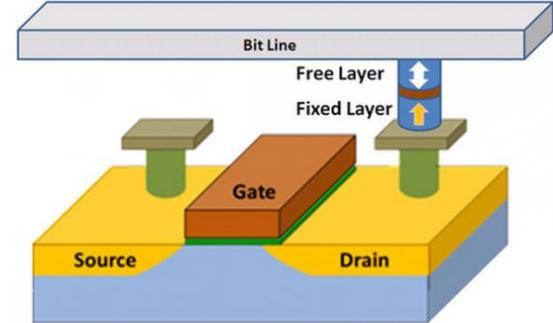
- Ultra-Low Power
 - Mobile
 - IoT & AI
- Speed
 - High Performance Computing



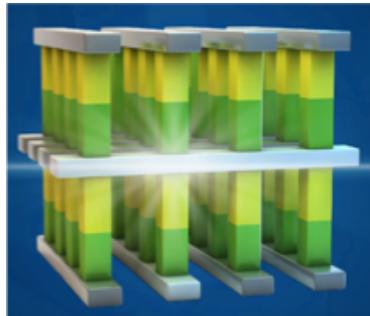
Panelist Views

SRAM – Speed, Endurance
SCM – Capacity, Cost

	Tom C	Tom A	Andy	Jack	Jean-Pierre	Yoda	Endoh
Main Segment	<ul style="list-style-type: none"> ▪ Emerging memory: MRAM, ReRAM, FeRAM, PCM 	<ul style="list-style-type: none"> ▪ NV-DRAM ▪ DRAM ▪ Embedded 	<ul style="list-style-type: none"> ▪ Apart from eNV: ▪ Novel LLC SRAM-replacement in compute chips 	<ul style="list-style-type: none"> ▪ UMA ▪ SRAM ▪ e-Flash 	<ul style="list-style-type: none"> ▪ e-Flash replacement ▪ Persistent DRAM 	<ul style="list-style-type: none"> ▪ Embedded (e-Flash,L3,& L2) 	<ul style="list-style-type: none"> ▪ e-Memory of Logic
Application / Market	<ul style="list-style-type: none"> ▪ Stand alone ▪ Embedded (replace SRAM, NOR) ▪ Emerging applications—AI, etc 	<ul style="list-style-type: none"> ▪ SSD, RAID ▪ HPC ▪ IoT, MCU Emb 	<ul style="list-style-type: none"> ▪ Apart from IoT: AI/ML 	<ul style="list-style-type: none"> ▪ IoT/Wearables ▪ AI ▪ Automotive ▪ Medical Devices 	<ul style="list-style-type: none"> ▪ High-end MCUs for IoT (handling large amounts of data) ▪ Data storage ▪ Mobile ▪ AI computing 	<ul style="list-style-type: none"> ▪ Any 	<ul style="list-style-type: none"> ▪ Mobile, IoT, Car Electronics, AI, Robot
Challenges	<ul style="list-style-type: none"> ▪ Integrating emerging memory manufacturing with CMOS ▪ Ramping volume so achieves cost competitiveness 	<ul style="list-style-type: none"> ▪ Scaling while maintaining endurance, DR ▪ High Vol Mfg 	<ul style="list-style-type: none"> ▪ Manufacturability 	<ul style="list-style-type: none"> ▪ Architecture designed to take advantage of MRAM ▪ Initial Adoption Rate 	<ul style="list-style-type: none"> ▪ Manufacturing cost (standalone) ▪ >Gb capacity ▪ RAM compatibility 	<ul style="list-style-type: none"> ▪ Reading for small node ▪ Coexistence of high-speed and endurance 	<ul style="list-style-type: none"> ▪ Improvement of MRAM ▪ Performance for each Application
Breakthru Needed	<ul style="list-style-type: none"> ▪ Integration of MRAM with CMOS manufacturing ▪ Balance of endurance and retention 	<ul style="list-style-type: none"> ▪ STT switching efficiency ▪ New Switching - SOT, VCMA, . - 8-10 yrs 	<ul style="list-style-type: none"> ▪ Endurance boosting for LLC ▪ Defectivity Root Cause/Corrective Action to drive up yields 	<ul style="list-style-type: none"> ▪ Gain a 10x speed up for wider use as 	<ul style="list-style-type: none"> ▪ SOT as a fast & infinitely endurant next-gen MRAM ▪ Change design/architecture paradigm 	<ul style="list-style-type: none"> ▪ Should work on new physics too 	<ul style="list-style-type: none"> ▪ Damage Control ▪ Scalable Material ▪ High TAT Process Tools



Emerging Memories Opportunities



Tom Coughlin
Coughlin Associates
www.tomcoughlin.com

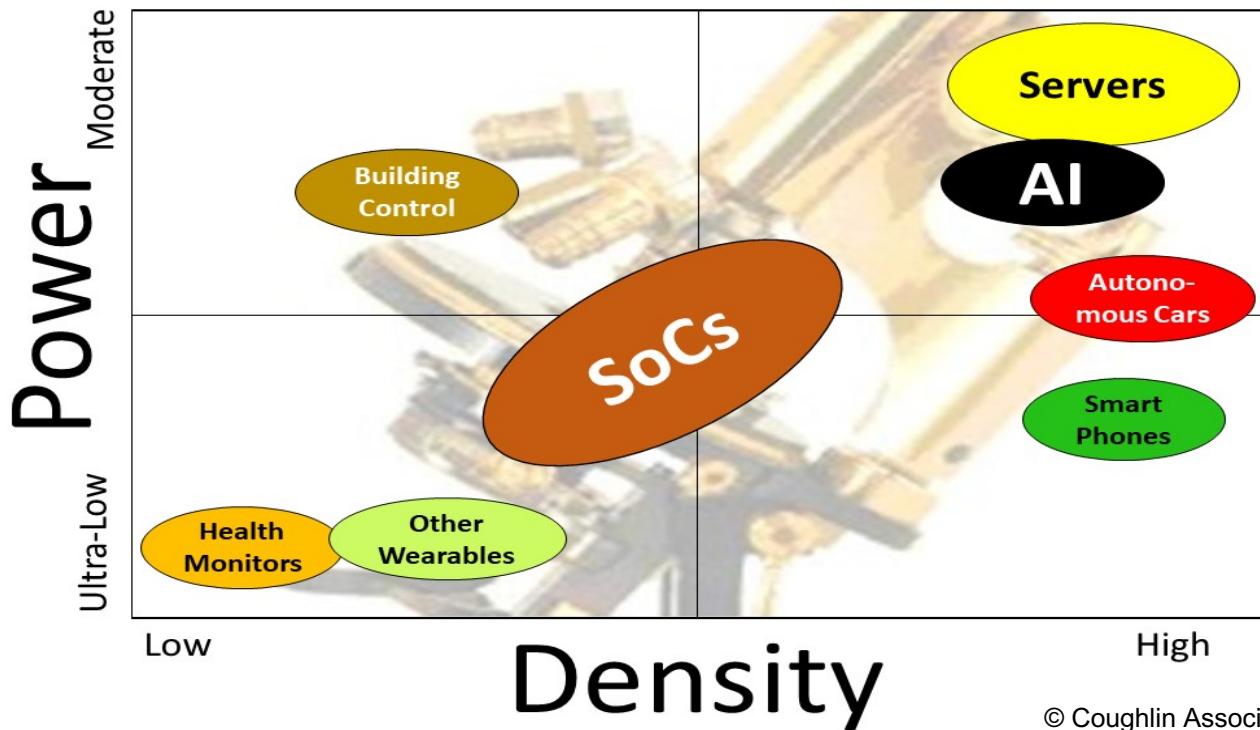


Tom Coughlin

Tom Coughlin has worked for over 36 years in the data storage industry. He has over 1000 publications and six patents. Tom is active with the IEEE, SMPTE, IDEMA, and other professional organizations. Dr. Coughlin is an IEEE Fellow. He is co-chair of the iNEMI Mass Storage Technical Working Group, Education Chair for SNIA SSSI, he is President Elect of IEEE-USA and a member of the IEEE Consultants Network of Silicon Valley. His publications include the Digital Storage Technology Newsletter, Media and Entertainment Storage Report and other reports. Tom is the author of Digital Storage in Consumer Electronics: The Essential Guide, now in its second edition with Springer. He has a regular Storage Bytes Forbes.com blog and does a digital storage column for the IEEE Consumer Electronics Magazine.

He is the founder and organizer of the Annual Storage Visions Conference as well as the Creative Storage Conference. Coughlin Associates provides market and technology analysis as well as data storage technical and market consulting.

Memory Density and Power Requirements by Application Category



© Coughlin Associates and Objective Analysis

Future Memory/Storage Hierarchy

© Coughlin Associates and Objective Analysis

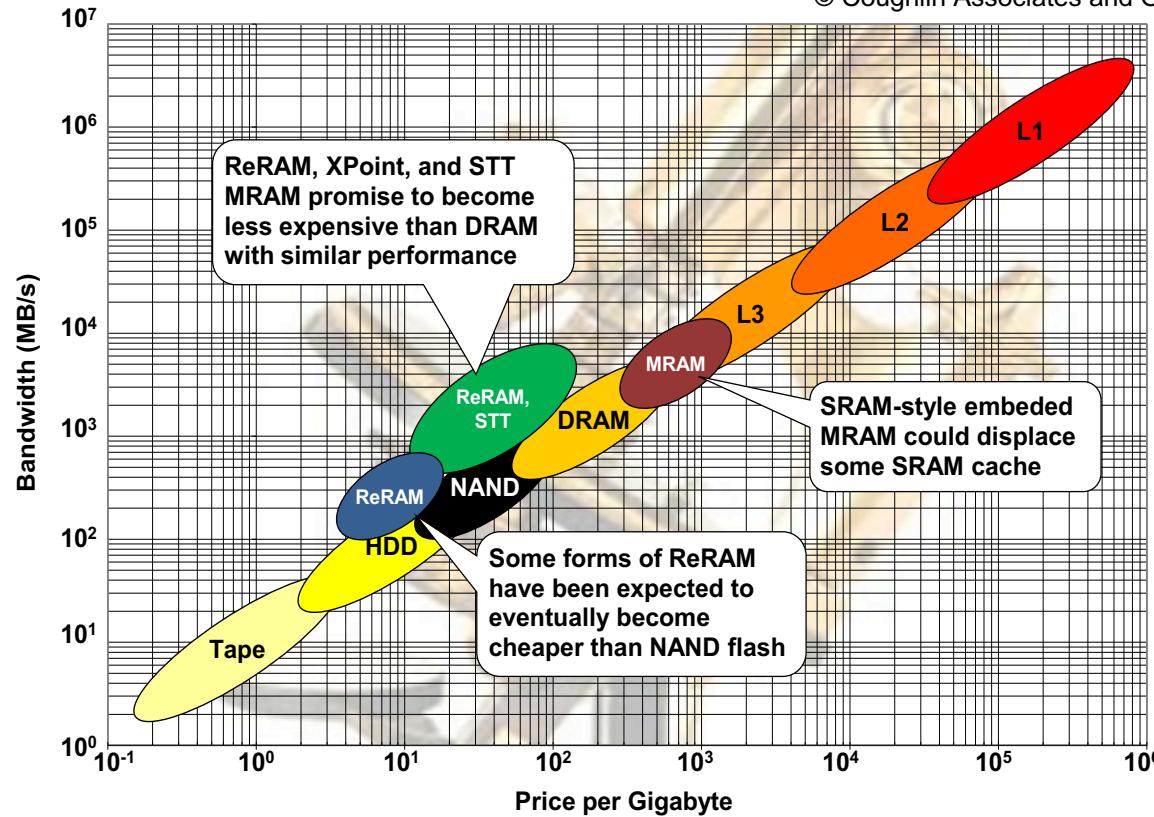
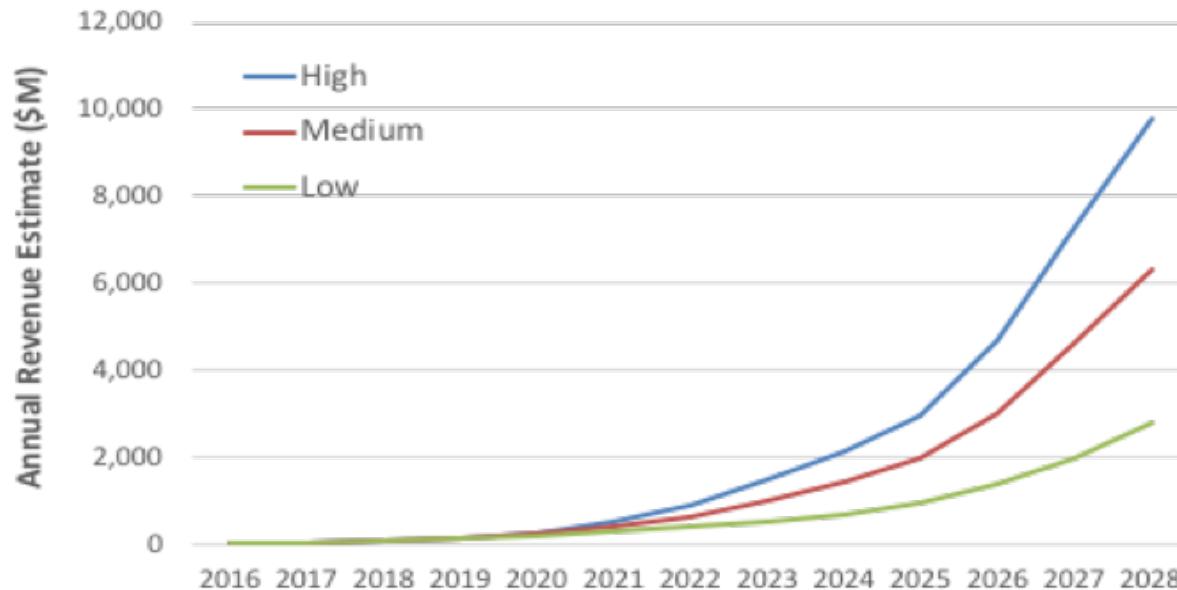


CHART OF HIGH, BASELINE AND LOW REVENUE ESTIMATES FOR EMERGING MEMORIES (\$M)

© Coughlin Associates and Objective Analysis

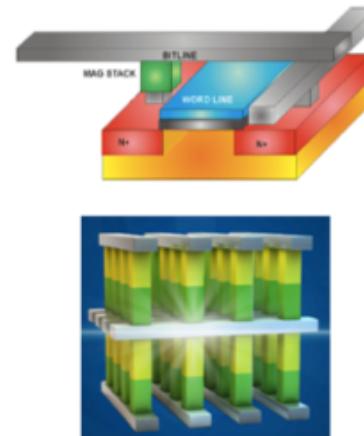


New Report on Emerging Memories

- Flash memory will remain a dominant solid-state memory for several generations with all manufacturers having moved to 3D flash.
- The 3D X-Point technology is poised to impact DRAM production while STT MRAM will impact SRAM, NOR and some DRAM.
- Resistive RAM (ReRAM) appears to be a potential replacement for flash memory sometime in the next decade.
- The memories addressed in this 161-page report, containing 31 tables and 111 figures, include PCM, ReRAM, FeRAM and MRAM Technology as well as a variety of less mainstream technologies.

EMERGING MEMORIES POISED TO EXPLODE

An Emerging Memory Report



COUGHLIN ASSOCIATES
San Jose, California
July 2018

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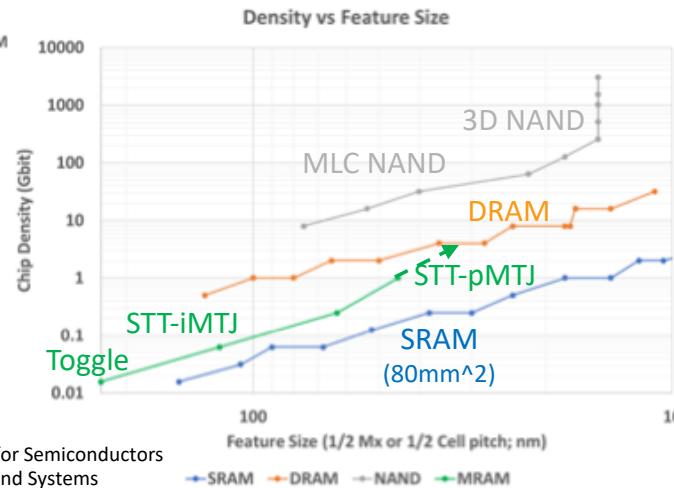
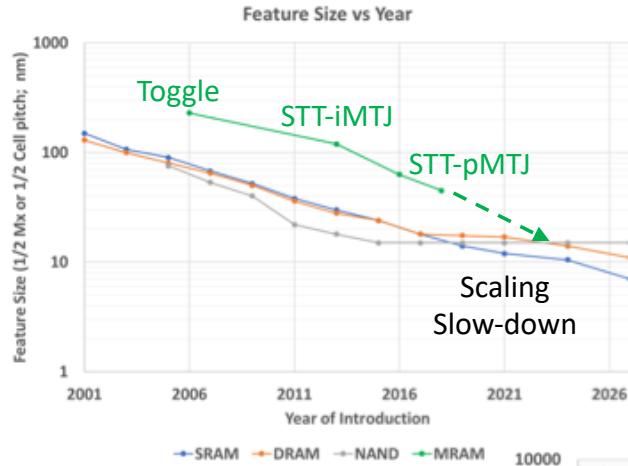


MRAM DEVELOPER DAY PANEL

MRAM DEVELOPER DAY PANEL

T. Andre 06 Aug 2018

Technology Scaling



- **MRAM has not reached the most advanced Feature size available**
 - Transistor technology for next generations is already in production
 - MRAM technology is on track to catch up by 2024
- **STT-MRAM is approaching DRAM Density vs Feature**
 - MRAM technology is on track to catch up with next generation
 - STT-MRAM optimized with increased Efficiency
 - New approaches (SOT, VCMA, ...) for longer term scaling



Source for SRAM, DRAM, NAND:
The International Technology Roadmap for Semiconductors
The International Roadmap for Devices and Systems

Applications Driving MRAM Development

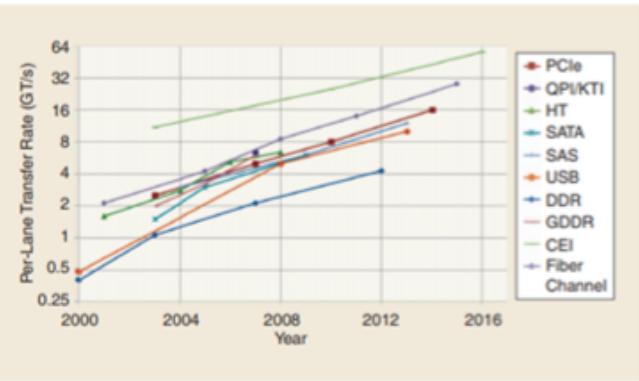
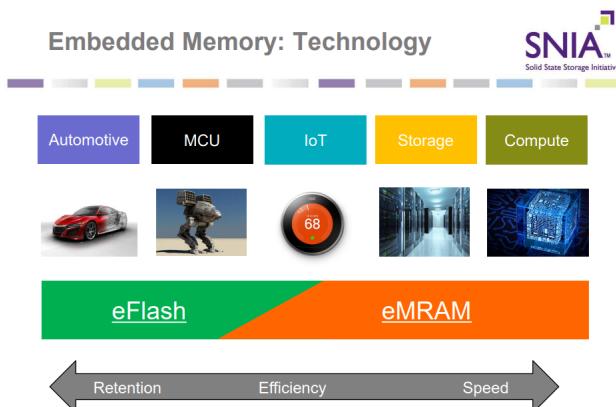


FIGURE 8: Per-pin data rate versus year for a variety of common I/O standards.
Trends in Solid State Circuits from ISSCC – Jan 2017

- **High Bandwidth Non-volatile Write Buffer**
 - MRAM uniquely offers non-volatility with:
 - High reliability
 - High bandwidth
 - High endurance
 - Low power/bandwidth
- **DRAM**
 - MRAM on track to catch up with DRAM scaling by 2024
 - DRAM market drives high volume manufacturing
- **Embedded MRAM**
 - Non-volatile memory at advanced nodes
 - Compute memory w/ lower standby power
 - Adaptable to different use cases





Spin Transfer Technologies

An Allied Minds Company

Magnetic Migration

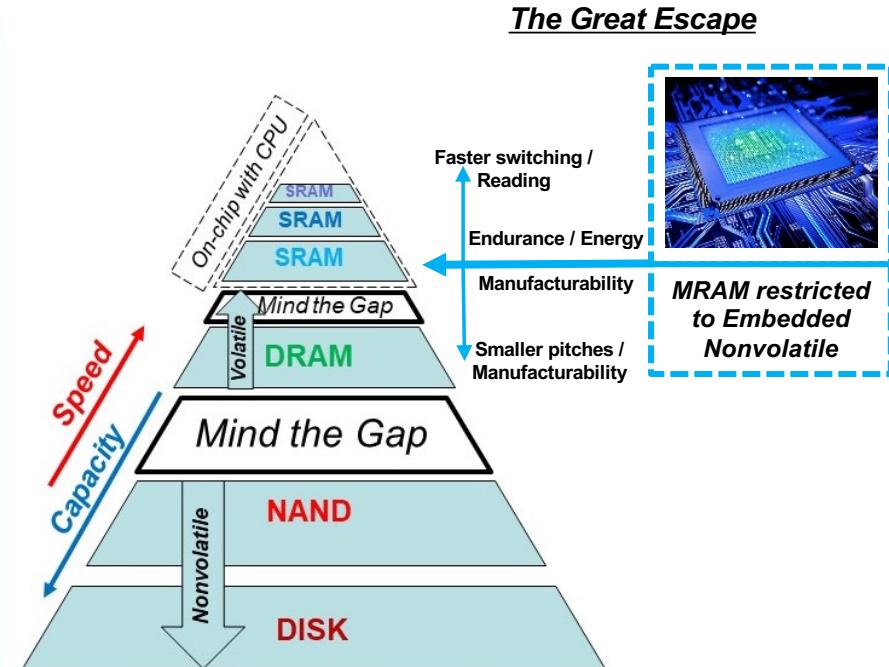
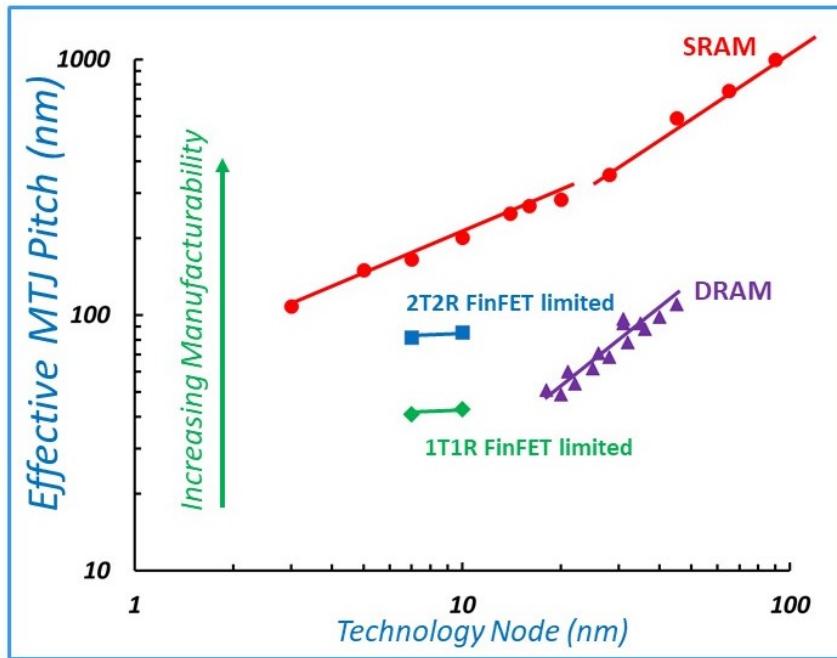
Andrew J. Walker PhD

MRAM Developer Day Panel

August 6, 2018

Magnetic Migration

- Effective Pitch as a Roadmap Guide to Magnetic Migration*





MRAM in 2024



- MRAM is now embedded into 80% of all digital and mixed signal SOCs
 - MRAM displaces SRAM in majority of the applications
 - SoC Designs/Architecture have now been modified to take full Advantage of MRAM
- MRAM Foundry and Memory Cores offerings range from ultra-low power to speed up to 1GHz
- MRAM Applications are widespread
 - Major Drivers: AI (both Von Neuman & Bio-Inspired), IoT, Wearables, Automotive, Mobile



Citius, Durius, Fortius

MRAM Developer Day

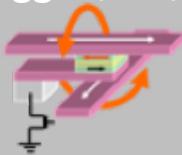
August 6, 2018

ANTAIOS MISSION STATEMENT: Develop SOT as “next-gen” MRAM Technology



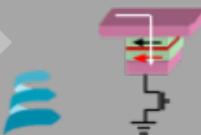
Gen.1

Toggle (2006)



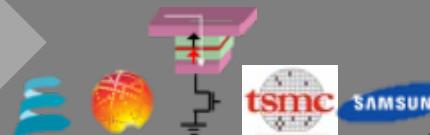
Gen.2

Planar STT (2012)



Gen.3

Perp. STT (2018)



Gen.4

SOT



Not Scalable
beyond 90nm
(write power)

Not Scalable
beyond 65/40 nm
(retention)

Fully scalable
Endurance-Retention-Speed tradeoff
→ **Limited persistence and/or endurance and/or speed**

Fully scalable
Infinite endurance
+ **high intrinsic speed**
= **persistent RAM compatible**

SOT solves STT shortfalls

APPLICATIONS & MARKETS BY 2024 ?

2 value propositions for MRAM

– When **power consumption** is key

- IoT : For sure, through eFlash replacement
- Mobile : Should be OK by 2024 (larger capacities, small nodes)
Fusing RAM and NVM in one single memory with SOT ?

– When **reliable buffering / caching** is needed

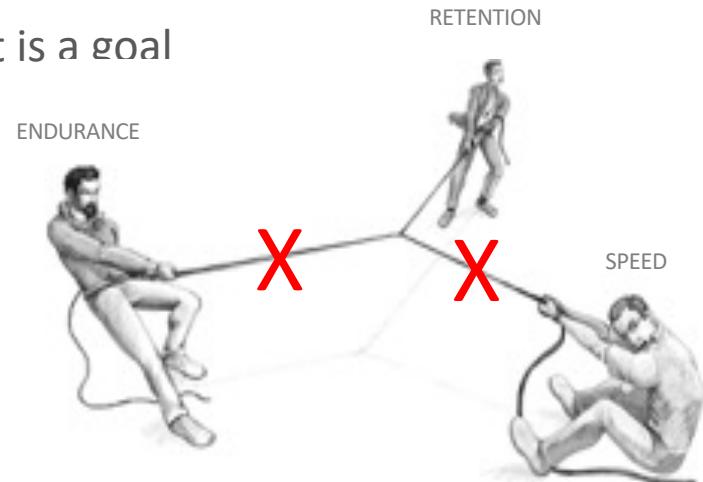
- Data storage : Already served by ES - Will grow when capacity/cost improve
SOT (better performances) will further expand market
- AI chips : Killer benefits wrt eSRAM
STT good enough as-is, but SOT even better



CHALLENGES & BREAKTHROUGHS

- Different for standalone and embedded
 - Embedded → High capacity (>Gb)
Temperature if automotive market is a goal
 - Standalone → Very High capacity (10's of Gb)
Manufacturing cost
- Common to both
 - Meeting RAM requirements (speed, endurance)

→ SOT is the only solution !
 - Change chip/system architecture paradigm
(beyond 1-to-1 replacement)



CONCLUSION



AI



HPC



Storage



Mobile



IoT



Automotive

Dense, Low Power
wrt eSRAM
memory brings data closer to compute

Fast, Persistent
wrt DRAM
memory provides secured data buffering

Fast, dense
wrt eSRAM/eFlash
memory saves battery life

Fast, Low power
wrt eFlash
memory saves battery life

SOT is key to make this happen !



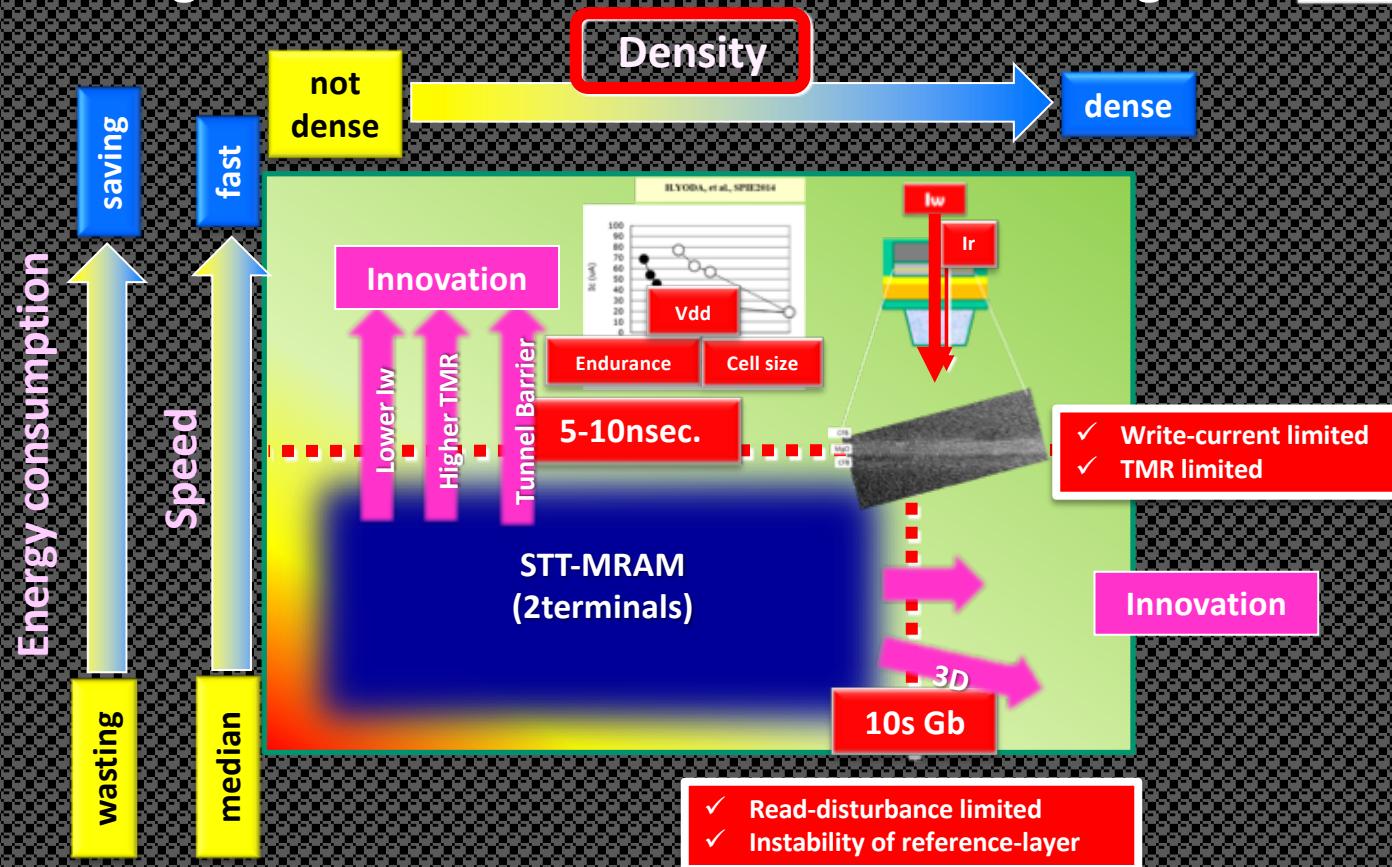
What is MRAMs in 2024?

Hiroaki Yoda

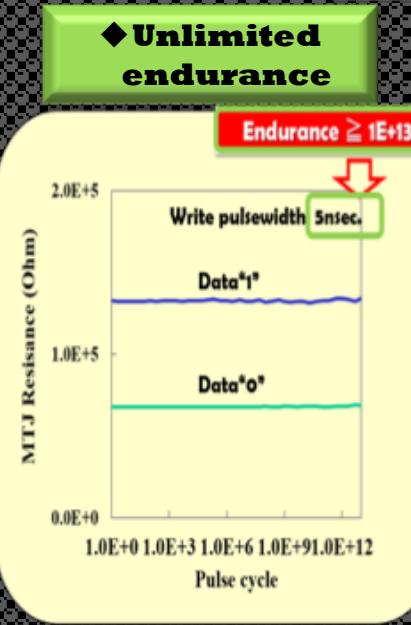
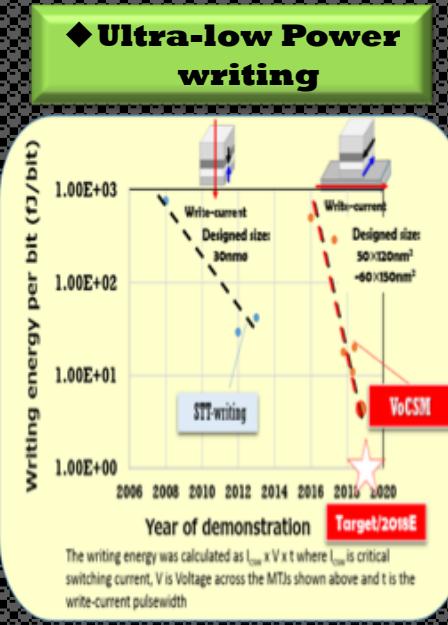
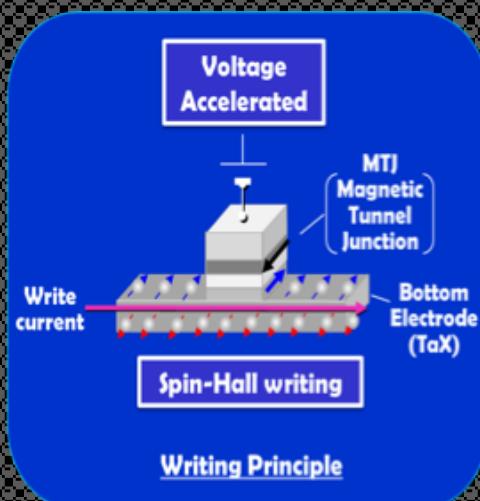
Corporate Research & Development Center,
Toshiba Corporation

Supported by The ImPACT Program of the Council
for Science, Technology and Innovation
(Cabinet Office, Government of Japan).

Positioning of STT-MRAM with the current technologies



Non-volatile Memory with Ultra-low Power, High-speed, and Unlimited Endurance



Patent

- ◆ Japanese patent P6270934, USP 9,881,660: High-density VoCSM (writing 8data with 2 write-pulses)
 - ◆ Japanese patent P6280195: High-Speed VoCSM (Complementary writing)
- Other 21 patents registered and other 27 patents pending

Publication

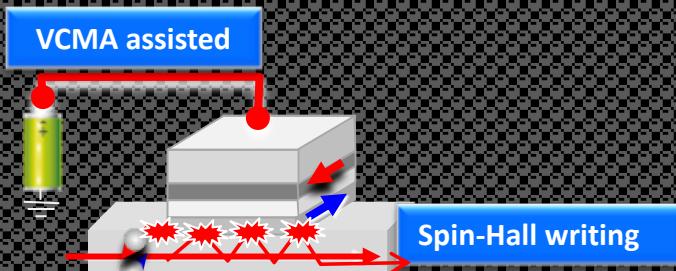
- ◆ Digests of 62nd IEDM, session 27.6, San Francisco, CA, 3–7 December, 2016
- ◆ Proceedings of IMW 2017, p. 165, Monterey, CA, 14 – 17 May, 2017
- ◆ IEEE Transactions on Magnetics, vol. 53, p. 3401104, 2017

More than 10 invited talks and other 20 conference talks.

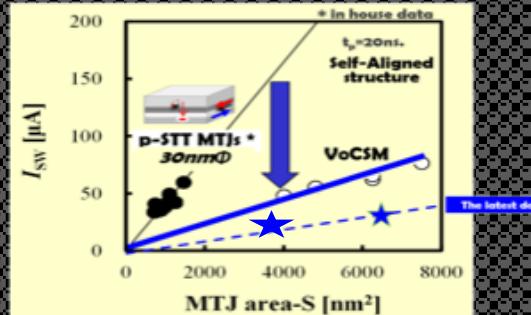
SOT(spin-Hall)-MRAM, VoCSM (3 terminal devices)



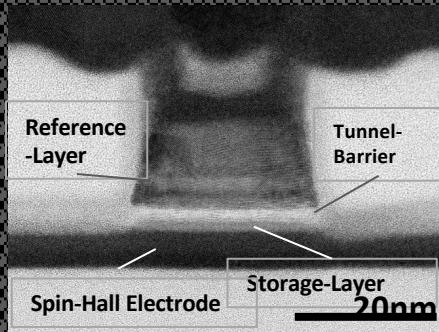
Ultra-high efficiency of writing



Proof of the high-efficiency of VoCSM



TEM image of the MTJ



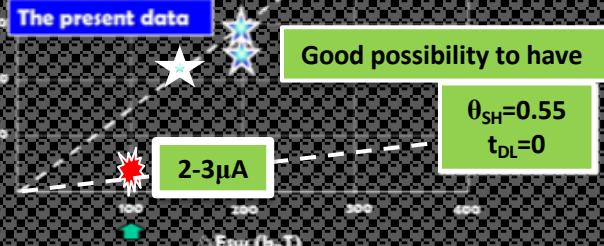
Prospect of I_{csw}

$$I_{csw}(\text{VoCSM}) = 4 \alpha_{eff}/\theta_{SH} \cdot E_{sw}(\text{oV}) \cdot t_p/W$$

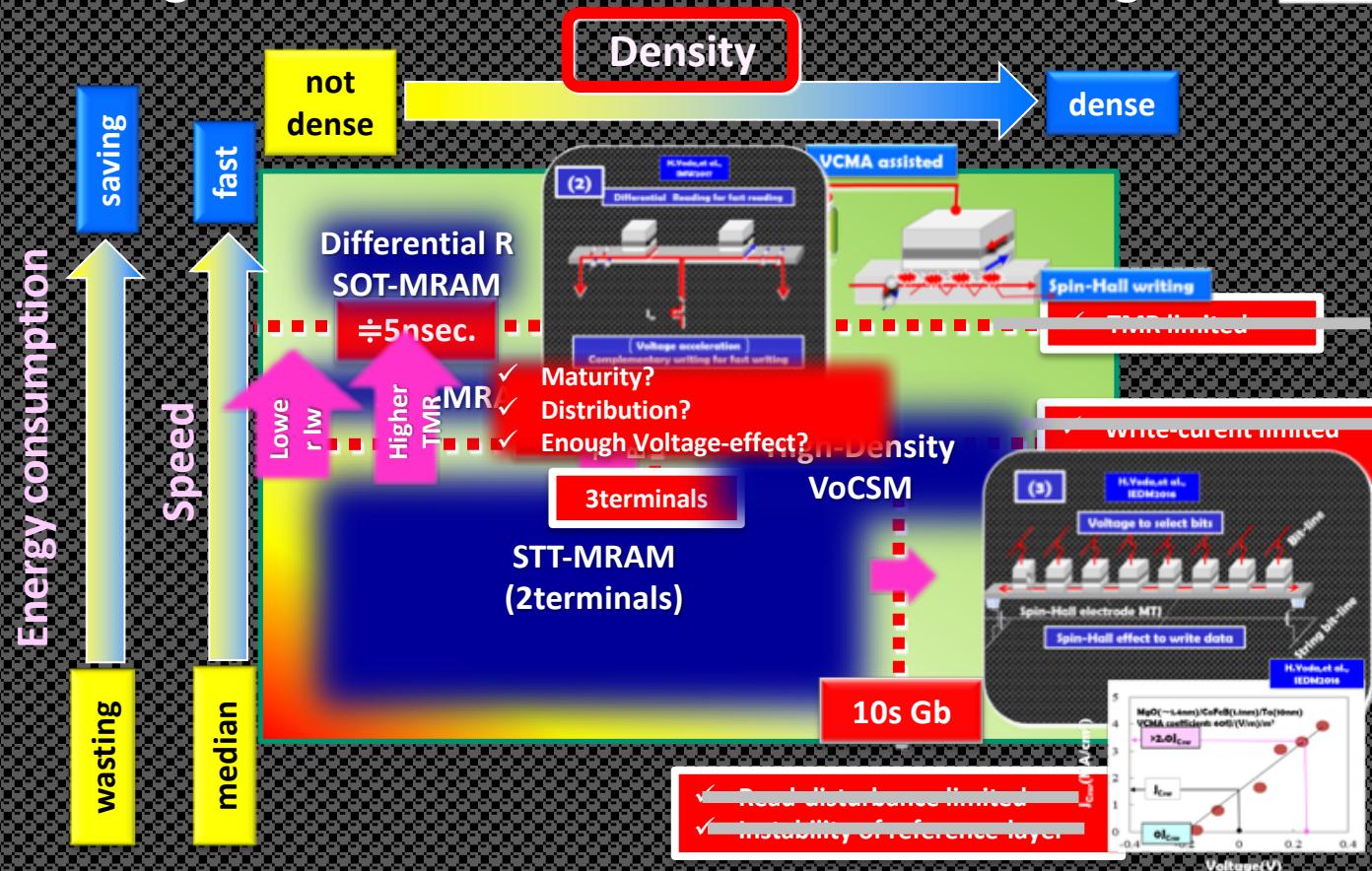
$$\theta_{SH}=0.14$$

$$t_{DL}=0$$

The present data



Positioning of STT-MRAM with the current technologies



Panelist Answer

	Yoda
Main Segment	Embedded (e-Flash,L3,& L2)
Application / Market	▪ Any
Challenges	Reading for small node Coexistence of high-speed and endurance
Breakthru Needed	▪ Yes
Etc	▪ Should work on new physics too

◆ What is the main segment for MRAM in 2024?

<My Position> e-Memory of Logic @ 2024



MRAM in 2024



	CMOS SRAM-LLC	MTJ STT-MRAM(S)		CMOS eFlash	MTJ STT-MRAM(F)		Other NVM	
	<1.1 V	<0.5 V	😊	12 V	<0.5V	😊	ReRAM	PCRAM
Write Current	10^{-5} A	10^{-5} A		10^{-4} A	10^{-5} A	😊	10^{-4} A	10^{-4} A
Write Speed	<10ns	<10 ns		10000 ns	<200 ns	😊	50 ns	100 ns
Read Speed	<5ns	<5 ns		30 ns	<25 ns		< 5 ns	< 5 ns
Retention	Volatile	1~Several Month	😊	10Years	10Years		10Years	10Years
Endurance	10^{15}	10^{15}		$10^{3\sim 4}$	$< 10^{8\sim 12}$	😊	10^6	$10^9 - 10^{12}$
Cell Size	160 ~ 280F ²	12 ~ 28F ²	😊	64 ~ 128F ²	6 ~ 14F ²	😊	6 ~ 10F ²	4 ~ 19F ²

①Low Power ②Small Cell Size

① Low Power ② High Speed Write
③ Better Endurance ④ Small Cell Size

◆ Which application / market will drive it?

<My Position> Mobile, IoT, Car Electronics, AI, Robot etc



◆ What are the challenges?

<My Position>

Improvement of MRAM Performance for each Application

For higher level cache: High Speed Write & Low Write Power
& 10^{15-16} Endurance

For e-Flash of Automotive Application: Excellent Thermal Stability (Δ)

For Main Memory : Scalability & High Density Array

◆ What technological breakthrough needed?

<My Position>

- 1) Damage Control Technology
- 2) Scalable Material Technology that can be used for mass production
- 3) High TAT Process Tools
- 4) CAD Technology including PDK
- 5) Circuit Technology such as NV-Logic

Most critical problem of MRAM is our mind.

⇒ **Tough Mind** to believe MRAM Potential



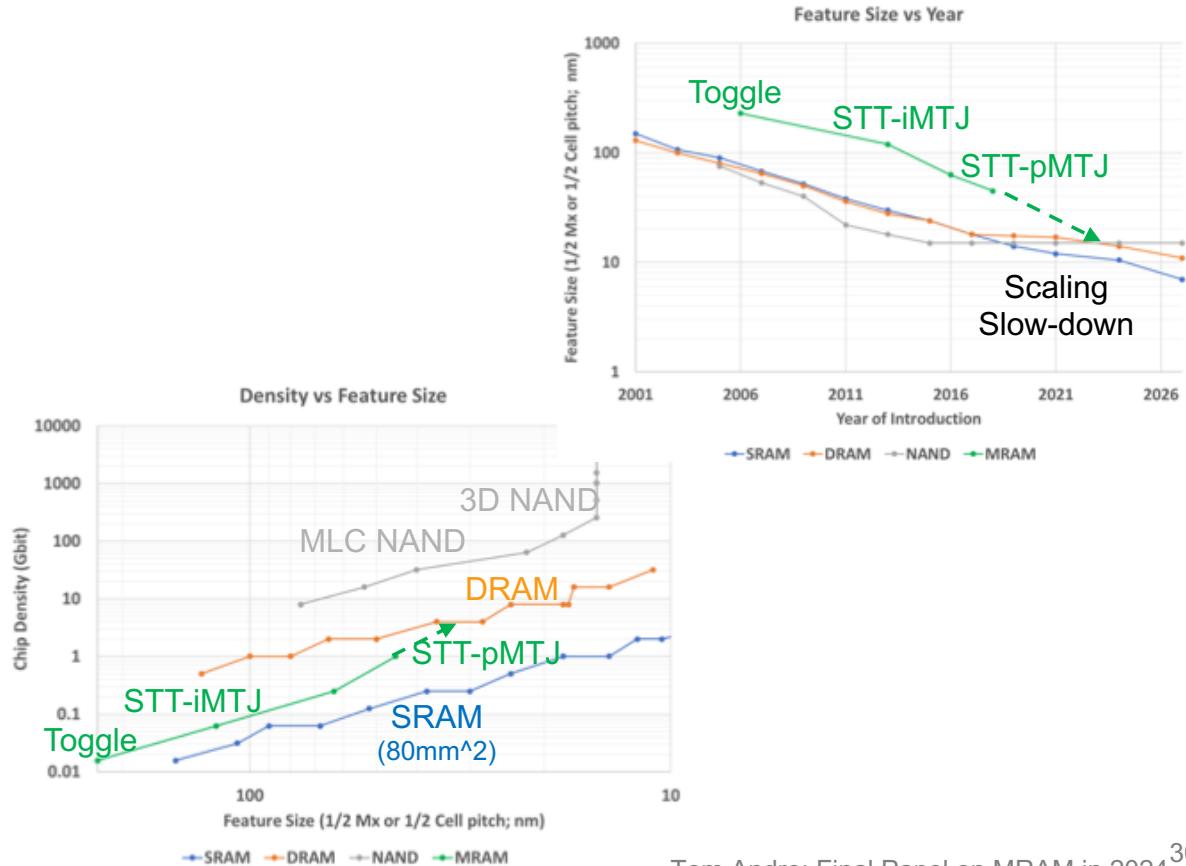


- *Back up*

MRAM Scaling

- **MRAM has not reached the most advanced Feature size available**
 - Transistor technology for next generations is already in production
 - MRAM technology is on track to catch up by 2024

- **STT-MRAM is approaching DRAM Density vs Feature**
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 - New approaches (SOT, VCMA, ...) for longer term scaling



Source for SRAM, DRAM, NAND:
 The International Technology Roadmap for Semiconductors
 The International Roadmap for Devices and Systems

MRAM Applications

- **High Bandwidth Non-volatile Write Buffer**

- MRAM uniquely offers non-volatility with:
 - High reliability
 - High bandwidth
 - High endurance
 - Low power/bandwidth

- **DRAM**

- MRAM on track to catch up with DRAM scaling by 2024
- DRAM market drives high volume manufacturing

- **Embedded MRAM**

- Non-volatile memory at advanced nodes
- Compute memory w/ lower standby power
- Adaptable to different use cases

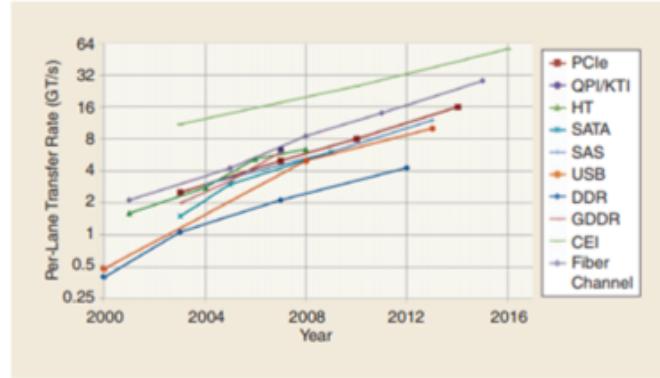


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Trends in Solid State Circuits from ISSCC – Jan 2017

Embedded Memory: Technology

