

Power

Outline

- ❑ Power and Energy
 - ❑ Dynamic Power
 - ❑ Static Power
-

Power and Energy

- Power is drawn from a voltage source attached to the V_{DD} pin(s) of a chip.

چون ترانزیستورهای اردویی برق را نزدیکی می‌سازند

- Instantaneous Power: $P(t) = I(t)V(t)$

- Energy:

$$E = \int_0^T P(t)dt$$

- Average Power:

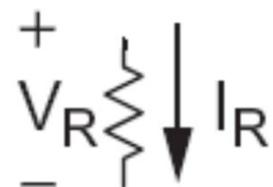
$$P_{avg} = \frac{E}{T} = \frac{1}{T} \int_0^T P(t)dt$$

Power in Circuit Elements

$$P_{VDD}(t) = I_{DD}(t)V_{DD}$$

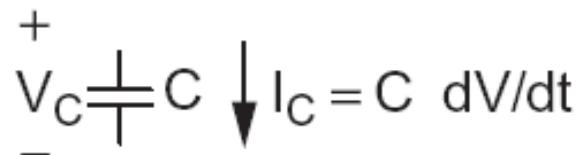


$$P_R(t) = \frac{V_R^2(t)}{R} = I_R^2(t)R$$



$$E_C = \int_0^{\infty} I(t)V(t)dt = \int_0^{\infty} C \frac{dV}{dt} V(t)dt$$

$$= C \int_0^{V_C} V(t)dV = \underline{\underline{\frac{1}{2}CV_C^2}}$$



Charging a Capacitor

- ## When the gate output rises

- Energy stored in capacitor is

$$E_S \equiv \frac{1}{2} C_S V_{DD}^2$$

- But energy drawn from the supply is

$$E_{VDD} = \int_0^{\infty} I(t) V_{DD} dt = \int_0^{\infty} C_L \frac{dV}{dt} V_{DD} dt$$

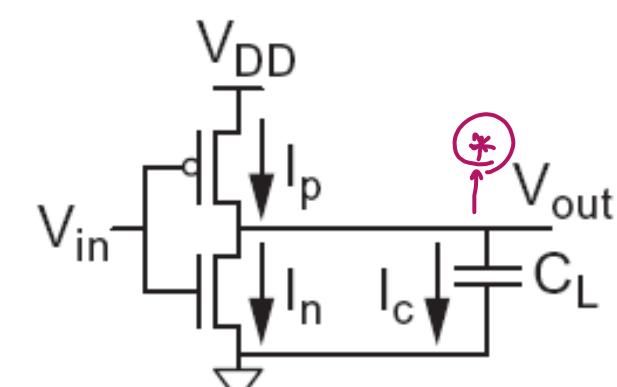
میزان داره دشارژ

$$= C_L V_{DD} \int_0^{\infty} dV = C_L V_{DD}^2$$

- Half the energy from V_{DD} is dissipated in the pMOS transistor as heat, other half stored in capacitor

- ## ☐ When the gate output falls

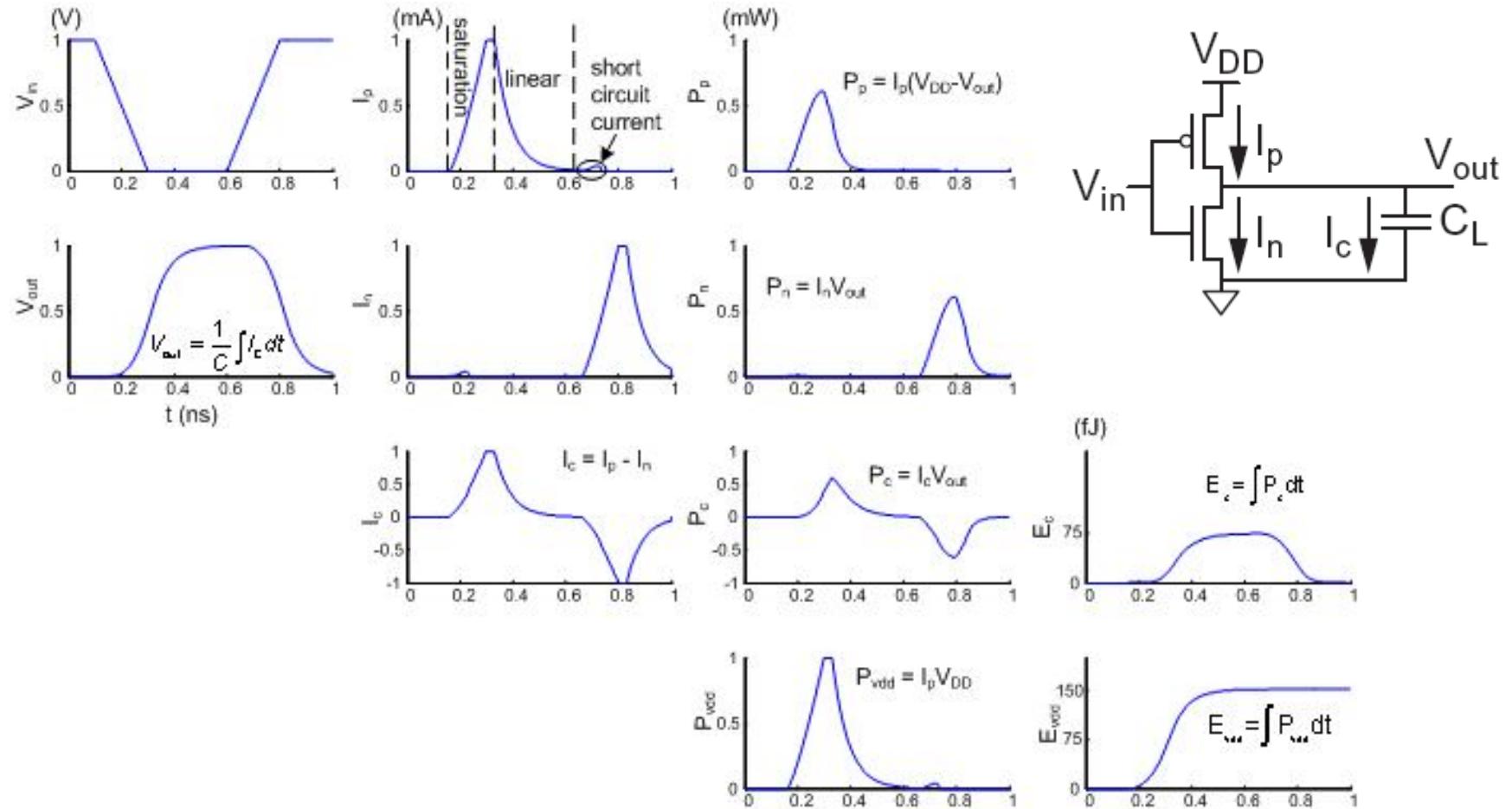
- Energy in capacitor is dumped to GND
 - Dissipated as heat in the nMOS transistor



نواب میں معرفہ زبانی صافی ہے \rightarrow ۱۷۶۱

Switching Waveforms

- Example: $V_{DD} = 1.0$ V, $C_L = 150$ fF, $f = 1$ GHz



Dynamic Power

Switching Power

$$P_{\text{switching}} = \frac{1}{T} \int_0^T i_{DD}(t) V_{DD} dt$$

چوب (نمای) ال بجهون از جی
ارزی میزد که وقتی برآشیم
لیکم صیغه توان

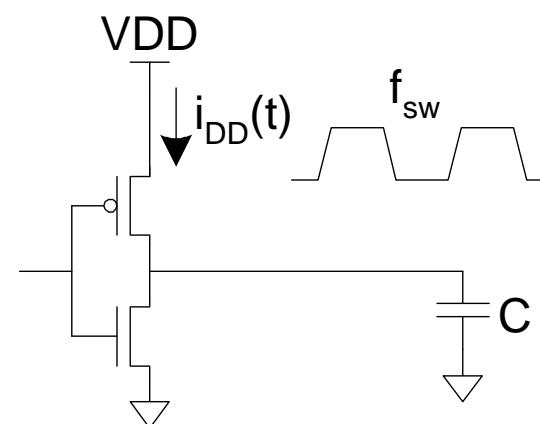
لیکم صیغه ای اسلام رکنی
برای از جی میزد
منجیزه بونه پسونه توان

$$= \frac{V_{DD}}{T} \int_0^T i_{DD}(t) dt$$

$$= \frac{V_{DD}}{T} [T f_{\text{sw}} C V_{DD}]$$

$$= C V_{DD}^2 f_{\text{sw}}$$

$$P_{\text{switching}} = f C V_{DD}^2$$



هرچی C بزرگتر باشے صیغه مصرف \rightarrow
توان ماهم بسته شیخ

CMOS VLSI Design 4th Ed.

7 همچنین قدر Switch $i_{DD}(t)$ \rightarrow
دو افراد زمان بسته شیخ \rightarrow $P_{\text{switch}} f \rightarrow$

توان مصرفی مونه هم بسته شیخ \rightarrow $P_{\text{switch}} V_{DD}^2 f$ افراد ایم V_{DD} داریم میلیم $i_{DD}(t)$ میزد C بزرگتر باشے صیغه مصرف \rightarrow

Activity Factor

- ❑ Suppose the system clock frequency = f
 - ❑ Let $f_{sw} = \alpha f$, where α = activity factor
 - If the signal is a clock, $\alpha = 1$
 - If the signal switches once per cycle, $\alpha = \frac{1}{2}$
 - ❑ Dynamic power:

$$P_{\text{switching}} = \alpha C V_{DD}^2 f$$

switching
→ If all times fsw
also with 0, 1, CLK & times

Short Circuit Current

- When transistors switch, both nMOS and pMOS networks may be momentarily ON at once
- Leads to a blip of “short circuit” current.
- < 10% of dynamic power if rise/fall times are comparable for input and output \rightarrow دو حالتی (short circuit) علاوه بر این
rise time و fall time که کوتاه باشند
- We will generally ignore this component

Dynamic Power \rightarrow پس از اینکه ترانزیستورها دستگیر شوند
 Switching Power \rightarrow پس از اینکه ترانزیستورها دستگیر شوند
 Short circuit Power \rightarrow < 10%

هر دوی از این دو قسمتی که می باشند
 ممکن است دو قسمتی که می باشند

Power Dissipation Sources

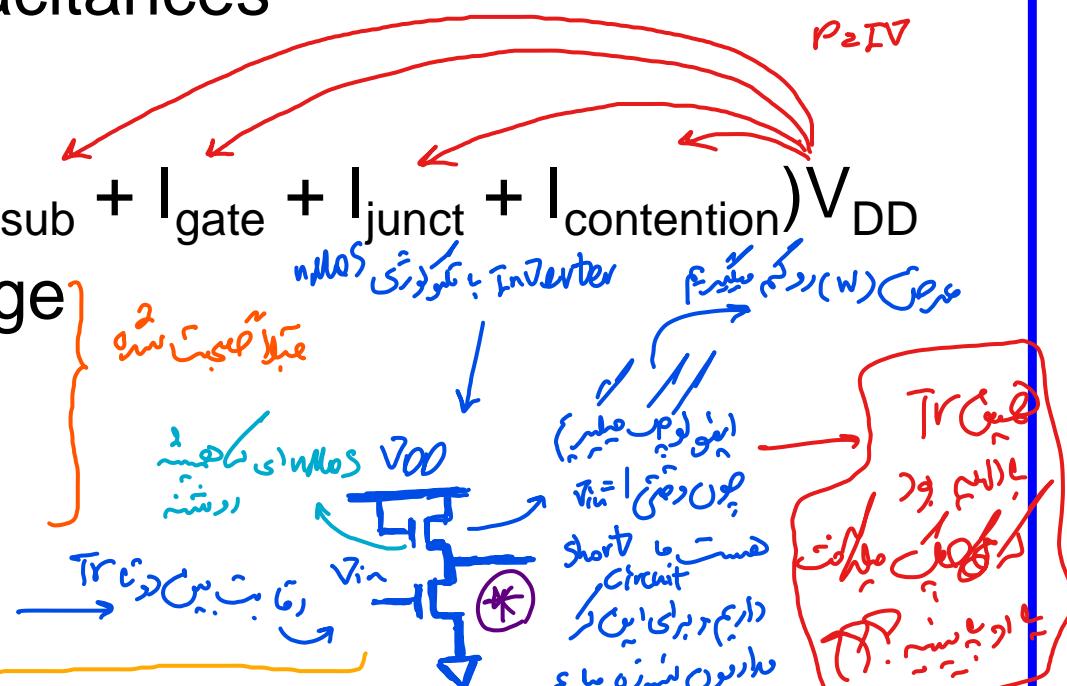
□ $P_{\text{total}} = P_{\text{dynamic}} + P_{\text{static}}$

□ Dynamic power: $P_{\text{dynamic}} = P_{\text{switching}} + P_{\text{shortcircuit}}$

- Switching load capacitances
- Short-circuit current

□ Static power: $P_{\text{static}} = (I_{\text{sub}} + I_{\text{gate}} + I_{\text{junct}} + I_{\text{contention}}) V_{\text{DD}}$

- Subthreshold leakage
- Gate leakage
- Junction leakage
- Contention current



Dynamic Power Example

- 1 billion transistor chip
 - 50M logic transistors

- Average width: 12λ برای حیثیت گذاری

- Activity factor = 0.1

- 950M memory transistors

- Average width: 4λ چون بزرگی داد drive عینک و شوک کن عرض

- Activity factor = 0.02 چون این 950 million TR را کمی نمی‌نمی‌شود

- 1.0 V, $\lambda = 25$ nm process با درصدی از صحته در هر لایه از متریال

- $C = 1 \text{ fF}/\mu\text{m}$ (gate) + $0.8 \text{ fF}/\mu\text{m}$ (diffusion) فرازهای draw و source

- $f = 10^{15} \text{ Hz}$

- Estimate dynamic power consumption @ 1 GHz.
Neglect wire capacitance and short-circuit current.

Solution

logic (مقدار) λ

Avg. width

$$\lambda = 25 \text{ nm} = 25 \times 10^{-9} \mu\text{m}$$

$$1 + 0.8 = 1.8$$

مقدار خارجی

diffusion

$$C_{\text{logic}} = (50 \times 10^6)(12\lambda)(0.025 \mu\text{m} / \lambda)(1.8 \text{ fF} / \mu\text{m}) = 27 \text{ nF}$$

$$C_{\text{mem}} = (950 \times 10^6)(4\lambda)(0.025 \mu\text{m} / \lambda)(1.8 \text{ fF} / \mu\text{m}) = 171 \text{ nF}$$

$$P_{\text{dynamic}} = [0.1 C_{\text{logic}} + 0.02 C_{\text{mem}}] (1.0)^2 (1.0 \text{ GHz}) = 6.1 \text{ W}$$

$$P_{\text{dynamic}} = \alpha_{\text{logic}} f C_{\text{logic}}^2$$

$$\alpha_{\text{memory}}$$

الآن باید دلخواهی اسکالاری هم کنیم

لذا می‌توانیم "HeatSync" (HeatSync) را در میان طبقه و اتصالات قرار دهیم

$$P = IV \Rightarrow I = 6.1 \text{ Amper} \rightarrow \text{جریان متوسط اینتریشن}$$

$$6.1 \text{ W}$$

لذا اسکالاری بعیی این در بررسی مطمئن می‌شود که توان برآورده شود

Dynamic Power Reduction

- $P_{\text{switching}} = \alpha C V_{DD}^2 f$
 - Try to minimize:
 - Activity factor
 - Capacitance
 - Supply voltage
 - Frequency
- *چیزی کی تغییر کرنے پر ممکن ہے*

Activity Factor Estimation

- Let $P_i = \text{Prob}(\text{node } i = 1)$
 - Activity factor $\bar{P}_i = 1 - P_i$
 - $\bar{P}_i = 1$ \rightarrow اینکه این نوک ایجاد نمی‌کند
 - $\bar{P}_i = 0$ \rightarrow اینکه این نوک باید ایجاد کند
 - $\alpha_i = \bar{P}_i * P_i \rightarrow (\bar{P}_i = 0) \text{ همچنان که } (P_i = 1) \text{ نیز همچنان که } (\bar{P}_i = 1) \text{ نیز همچنان که } (P_i = 0)$
 - If completely random data has $P = 0.5$ and $\alpha = 0.25$
 - Activity factor $\bar{P}_i = 0.5$ \rightarrow $0.5 \times 0.5 = 0.25$
 - Data is often not completely random
 - e.g. upper bits of 64-bit words representing bank account balances are usually 0
 - Activity factor $\bar{P}_i = 0$ \rightarrow $0 \times 0.5 = 0$
 - Data propagating through ANDs and ORs has lower activity factor
 - Depends on design, but typically $\alpha \approx 0.1$
 - Activity factor $\bar{P}_i = 0.1$ \rightarrow $0.1 \times 0.1 = 0.01$

Switching Probability

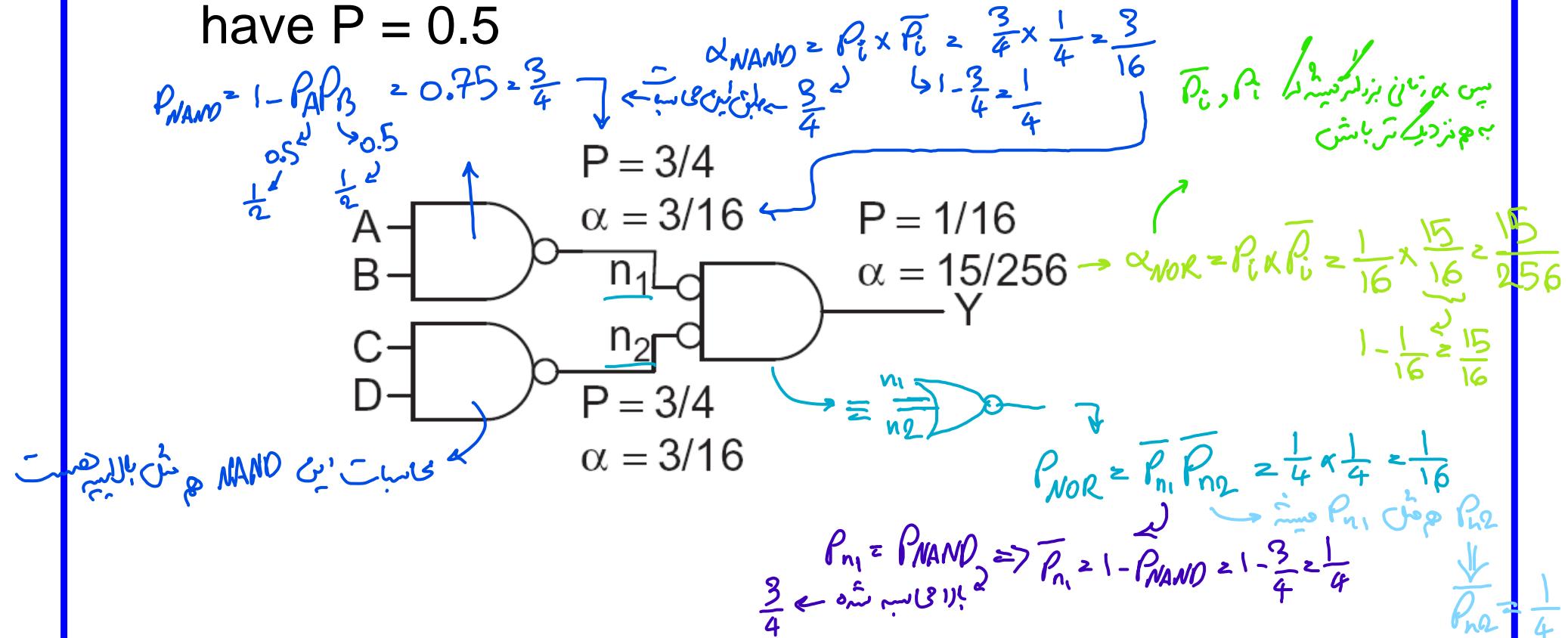
مُحَاجَّة لـ \bar{P}_Y احتمال تبديل و P_Y احتمال صفر بدل

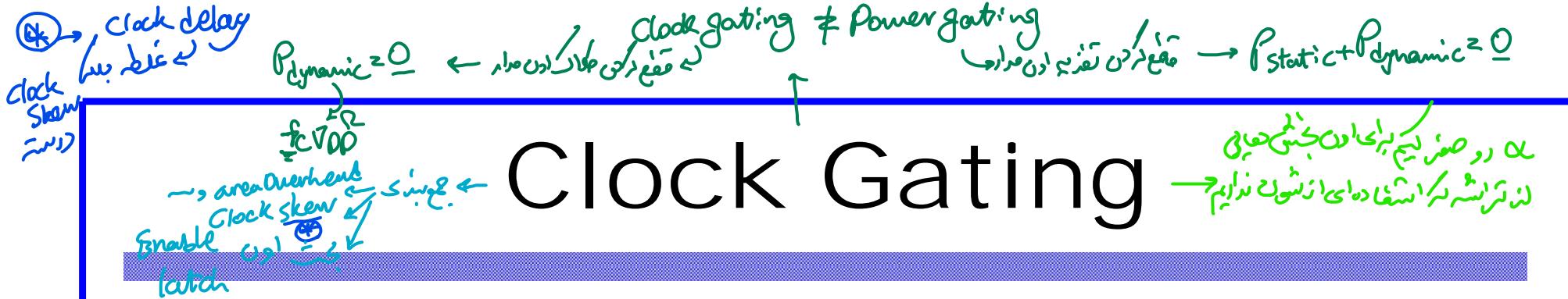
Gate	P_Y
AND2	$P_A P_B$ \rightarrow <i>مُحَاجَّة لـ AND</i> switching \rightarrow <i>مُحَاجَّة لـ AND</i>
AND3	$P_A P_B P_C$
OR2	$1 - \bar{P}_A \bar{P}_B \rightarrow 1 - \text{NOR}$
NAND2	$1 - P_A P_B \rightarrow 1 - \text{AND}$
NOR2	$\bar{P}_A \bar{P}_B$
XOR2	$P_A \bar{P}_B + \bar{P}_A P_B \rightarrow$ <i>مُحَاجَّة لـ XOR</i>

$\Rightarrow \oplus \equiv \overline{\oplus} \Rightarrow \bar{P}_A \bar{P}_B$

Example

- A 4-input AND is built out of two levels of gates
- Estimate the activity factor at each node if the inputs have $P = 0.5$

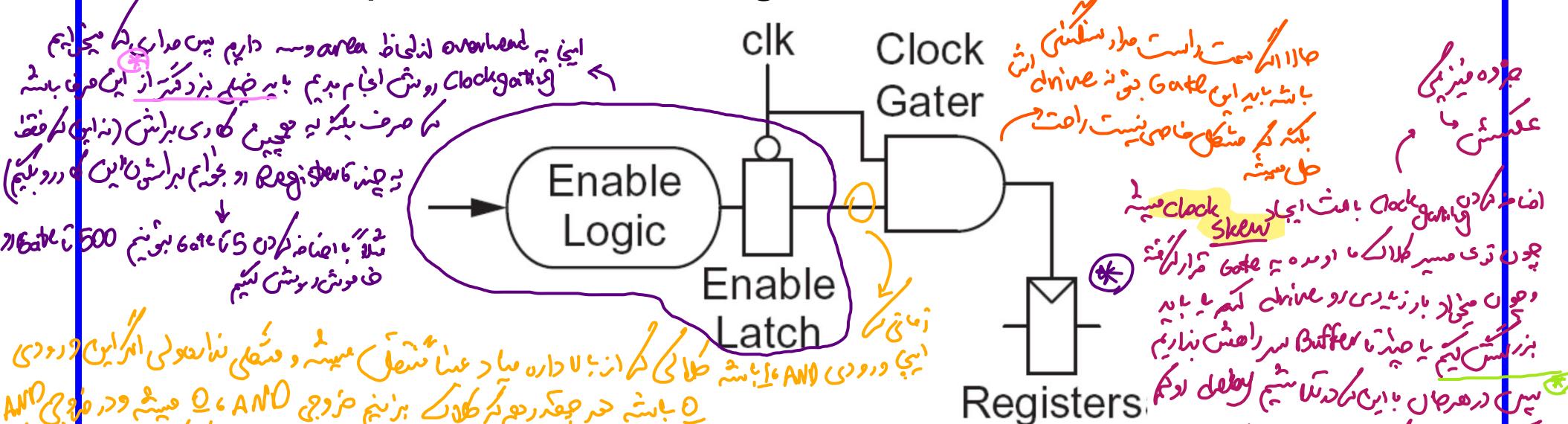




Clock Gating

لہ دو صفحہ یہی اور جسیں جیسا
لکھنور سے رہ اس قاداری ای ایشون نہ ایم →

- The best way to reduce the activity is to turn off the clock to registers in unused blocks
 - Saves clock activity ($\alpha = 1$)
 - Eliminates all switching activity in the block
 - Requires determining if block will be used



$$\Rightarrow f=0 \Rightarrow f_{\text{dynamic}}=0$$

Capacitance

□ Gate capacitance تیکو / میکرو الکترونیک

- Fewer stages of logic
- Small gate sizes

کم میزان خازن برای کاهش قیمت دستگاه Fab House

□ Wire capacitance

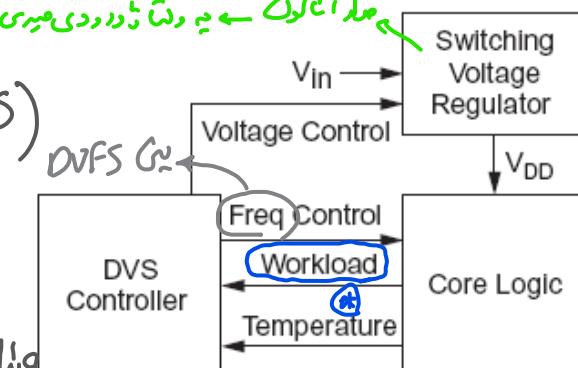
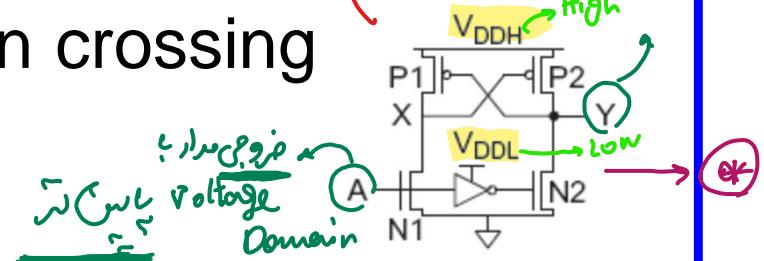
- Good floorplanning to keep communicating blocks close to each other
- Drive long wires with inverters or buffers rather than complex gates

Voltage / Frequency

- Run each block at the lowest possible voltage and frequency that meets performance requirements

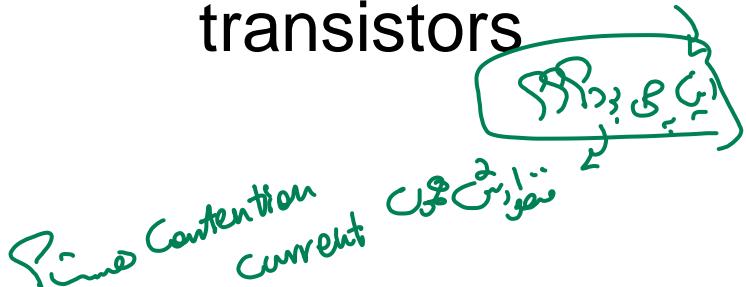
- ## □ Voltage Domains گزینه های که برای خوش دلی خاص خودشی در راه را می بینیم

- Provide separate supplies to different blocks
 - Level converters required when crossing
from low to high V_{DD} domains



Static Power

- Static power is consumed even when chip is quiescent.
 - Leakage draws power from nominally OFF devices
 - Ratioed circuits burn power in fight between ON transistors



Static Power Example

- ❑ Revisit power estimation for 1 billion transistor chip
- ❑ Estimate static power consumption

– Subthreshold leakage

معنی T_{th}

- Normal V_t :

$$10^{-7} \text{ A}$$

$$100 \text{ nA}/\mu\text{m} \rightarrow \text{Subthreshold leakage}$$

Subthreshold leakage

- High V_t :

$$10 \text{ nA}/\mu\text{m}$$

activity factor (α) ≈ 0.02

- High V_t used in all memories and in 95% of logic gates

$$5 \text{ nA}/\mu\text{m}$$

static power
high V_t

- Gate leakage

negligible

- Junction leakage

Solution

ی سب ت شبیه سلامیر \rightarrow ۱۲

$$W_{\text{normal-}V_t} = (50 \times 10^6)(12\lambda)(0.025\mu\text{m}/\lambda)(0.05) = 0.75 \times 10^6 \mu\text{m}$$

$$W_{\text{high-}V_t} = [(50 \times 10^6)(12\lambda)(0.95) + (950 \times 10^6)(4\lambda)](0.025\mu\text{m}/\lambda) = 109.25 \times 10^6 \mu\text{m}$$

$$I_{\text{sub}} = [W_{\text{normal-}V_t} \times 100 \text{ nA}/\mu\text{m} + W_{\text{high-}V_t} \times 10 \text{ nA}/\mu\text{m}] / 2 = 584 \text{ mA} \simeq 0.5 \text{ A}$$

$$I_{\text{gate}} = [(W_{\text{normal-}V_t} + W_{\text{high-}V_t}) \times 5 \text{ nA}/\mu\text{m}] / 2 = 275 \text{ mA}$$

$$P_{\text{static}} = (584 \text{ mA} + 275 \text{ mA})(1.0 \text{ V}) = 859 \text{ mW} \simeq 1 \text{ W}$$

فقط ۱ دات برای تو ان استاندارد صرف می شود
یعنی صریح ۱ صریح ۱ صریح نیست

Power Gating

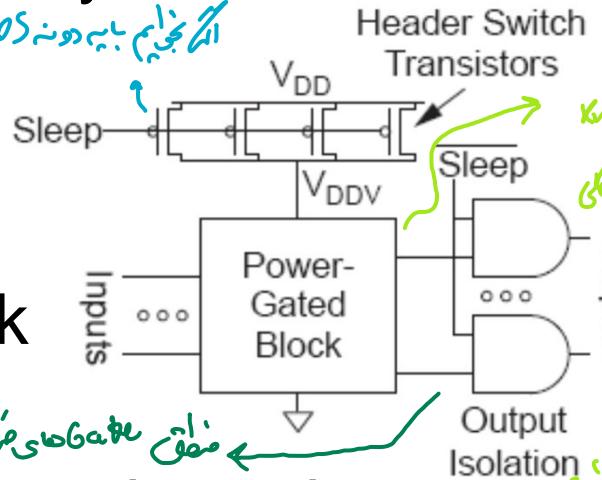
- Turn OFF power to blocks when they are idle to save leakage التي لا تُستعمل مدة طويلة PMOS مزدوج مداري PMOS مزدوج مداري

- Use virtual V_{DD} (V_{DDV})
 - Gate outputs to prevent invalid logic levels to next block

- Voltage drop across sleep transistor degrades performance during normal operation

- Size the transistor wide enough to minimize impact

- Switching wide sleep transistor costs dynamic power
 - Only justified when circuit sleeps long enough



Homework Assignments

- ❑ Chapter 5: 5.1, 5.4, 5.7, 5.10
 - ❑ For Tuesday 1402/9/21

ارجاع مکالمہ میں سب سے پہلے سے switching power میں ملکہ میں باس پڑھ دیں

پس اگر مداروں ہے اند (زنگ) باشہ گزینہ باتی توی
نامہ (Critical Path) بودہ (م) یہ (زنگ) قیمتی طبقہ (مسودہ)
نامہ (Switching Rate) پائیں (اردی میں) م
خاموشی و اوشن کارڈ مدارش ای م بسٹہ

Power Gating overhead

1. Voltage drop (1)

2. Switching power for wide Trs (2)

3. Delay on outputs (3)

4. Input voltage (4)

5. area (5)

chip warping

برداشت تراشه

دریں حکمت ایں طریقہ رضی و سعیت