Amirkabir University of Technology
(Tehran Polytechnic)

Memory Technologies Course By

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Homework 2

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Teaching Assistants

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Description:

In recent years, deep convolutional neural networks (CNNs) have gained widespread adoption across various domains, including visual recognition, object detection, and semantic segmentation. Despite their remarkable accuracy, CNNs face challenges due to their significant computational demands and extensive data storage requirements, impacting both computational performance and energy efficiency. While graphics processing units (GPUs) have traditionally addressed computational complexity, their high energy consumption remains a concern.

The energy consumption of a CNN accelerator involves memory access and computational consumption. External DRAM access, in particular, is the most energy-intensive aspect. To enhance energy efficiency, reducing external DRAM access frequency is crucial, emphasizing the need to optimize data addressing for improved data reuse efficiency and overall energy performance.

According to important role of memory unit in CNN accelerators, this homework design targeted the concept of using SRAM and DRAM for CNN accelerators. It is noteworthy that there is no necessary for full understanding of convolutional neural networks and you just need to consider features of SRAM and DRAM and your knowledge which you gain in the class to solve these problems. If you want to learn more about this concept you can read following papers.

CAP-RAM (arxiv.org)

ATRIA: A Bit-Parallel Stochastic Arithmetic Based Accelerator for In-DRAM CNN Processing (arxiv.org)

A Survey of Accelerator Architectures for Deep Neural Networks - ScienceDirect

ISSCC2018_manuscript.pdf (mit.edu)

Theoretical Questions:

Question 1:

A semiconductor company is developing a CNN accelerator for use in industrial image processing systems. The CNN accelerator will be integrated into production line cameras for tasks such as defect detection, quality control, and object recognition. The company needs to decide whether to use SRAM or DRAM for the on-chip memory of the CNN accelerator.

According to the industrial CNN accelerator application, compare the suitability of SRAM and DRAM for on-chip memory. Consider factors such as access speed, power consumption, area efficiency, and ease of integration. Provide a recommendation based on the specific requirements and constraints of the CNN accelerator.

Based on the analysis, recommend whether SRAM or DRAM is more suitable for on-chip memory in the CNN accelerator. Justify your recommendation by aligning it with the specific requirements, performance goals, and constraints of the industrial image processing application. Discuss potential trade-offs and any additional considerations that influenced your decision.

Implementation Questions:

* The technology file is attached in the homework folder.

* You have to attach your code and waveform figure in your response file.

Question 1:

Design a 3*3 bank memory based on a 6T SRAM cell with a sense amplifier (SA) for reading data from the memory cell in Hspice and fill the corresponding rows in the table 1. Please append an output waveform to validate each SRAM cell.

Question 2:

Design a 3*3 bank memory based on a DRAM cell with a sense amplifier (SA) for reading data from the memory cell in Hspice and fill the corresponding rows in table 1. Please append an output waveform to validate each DRAM cell.

Note: you can use following like if you are not well familiar with how design this circuit.

Micromachines | Free Full-Text | Modeling of Statistical Variation Effects on DRAM Sense Amplifier Offset Voltage (mdpi.com)

Question 3:

Comparison these two types of memory based on your result.

Table I

	SRAM	DRAM
Read time		
Write time		
Total Power		