

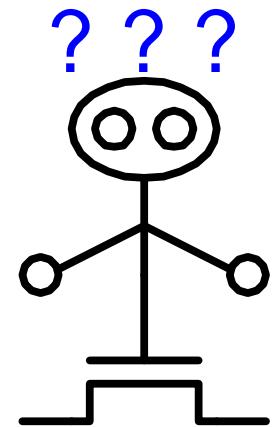
Review: Logical Effort

Outline

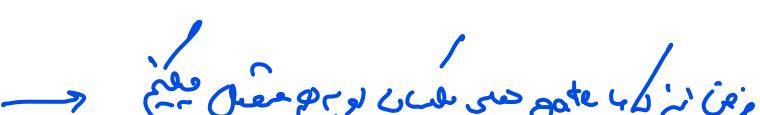
- ❑ Logical Effort
- ❑ Delay in a Logic Gate
- ❑ Multistage Logic Networks
- ❑ Choosing the Best Number of Stages
- ❑ Summary

Introduction

- Chip designers face a bewildering array of choices
 - What is the best circuit topology for a function?
 - How many stages of logic give least delay?
 - How wide should the transistors be?
- Logical effort is a method to make these decisions
 - Uses a simple model of delay
 - Allows back-of-the-envelope calculations
 - Helps make rapid comparisons between alternatives
 - Emphasizes remarkable symmetries



Delay in a Logic Gate

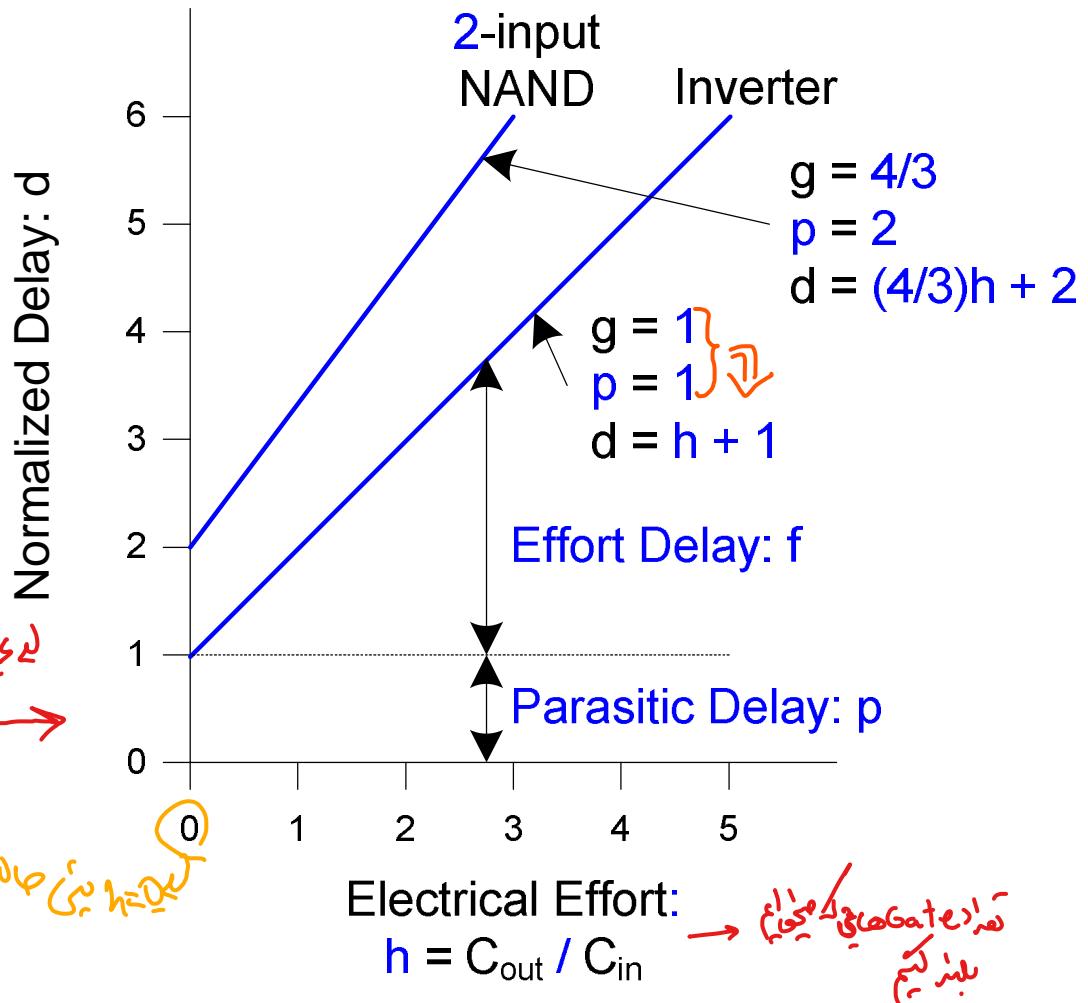
- Express delays in process-independent unit $d = \frac{d_{abs}}{d}$
- Delay has two components: $d = f + p$
 - f : *effort delay* = gh (a.k.a. stage effort)
 - Again has two components
 - g : *logical effort*
 - Measures relative ability of gate to deliver current
 - $g \equiv 1$ for inverter
 - h : *electrical effort* = C_{out} / C_{in} → 
 - Ratio of output to input capacitance
 - Sometimes called fanout
 - p : parasitic delay
 - Represents delay of gate driving no load
 - Set by internal parasitic capacitance

Delay Plots

$$\begin{aligned} d &= f + p \\ &= gh + p \end{aligned}$$

- What about NOR2?

مفهوم Effort Delay (جهد تأخير):
 $d = gh + p$
 عوامل Effort Delay:
 1. Logical Effort (جهد логики): g
 2. Parasitic Delay (جهد عوادت): p
 3. Electrical Effort (جهد كهربائي): h
 مفهوم Load (โหลด): C_{out}
 مفهوم Gate (گیت): C_{in}

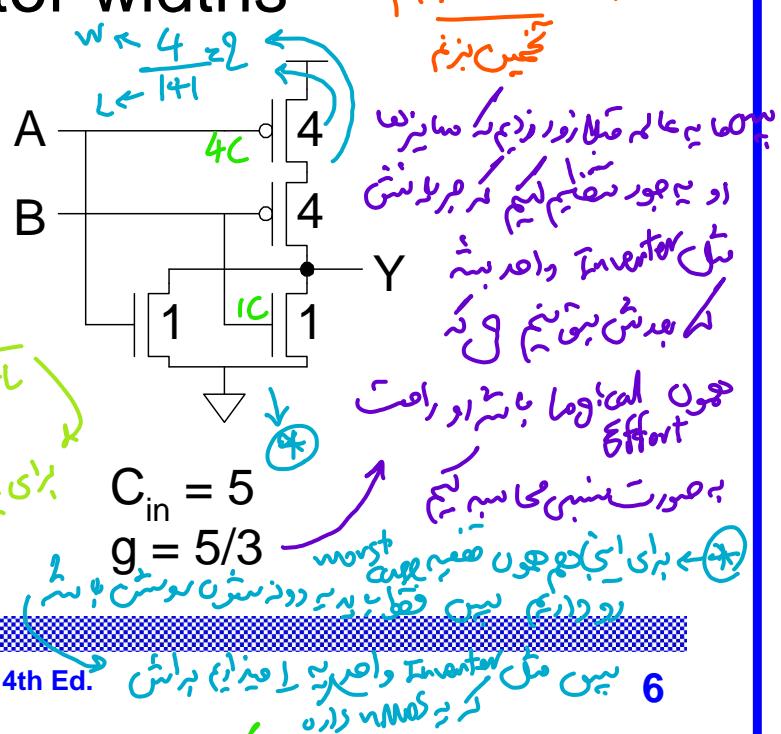
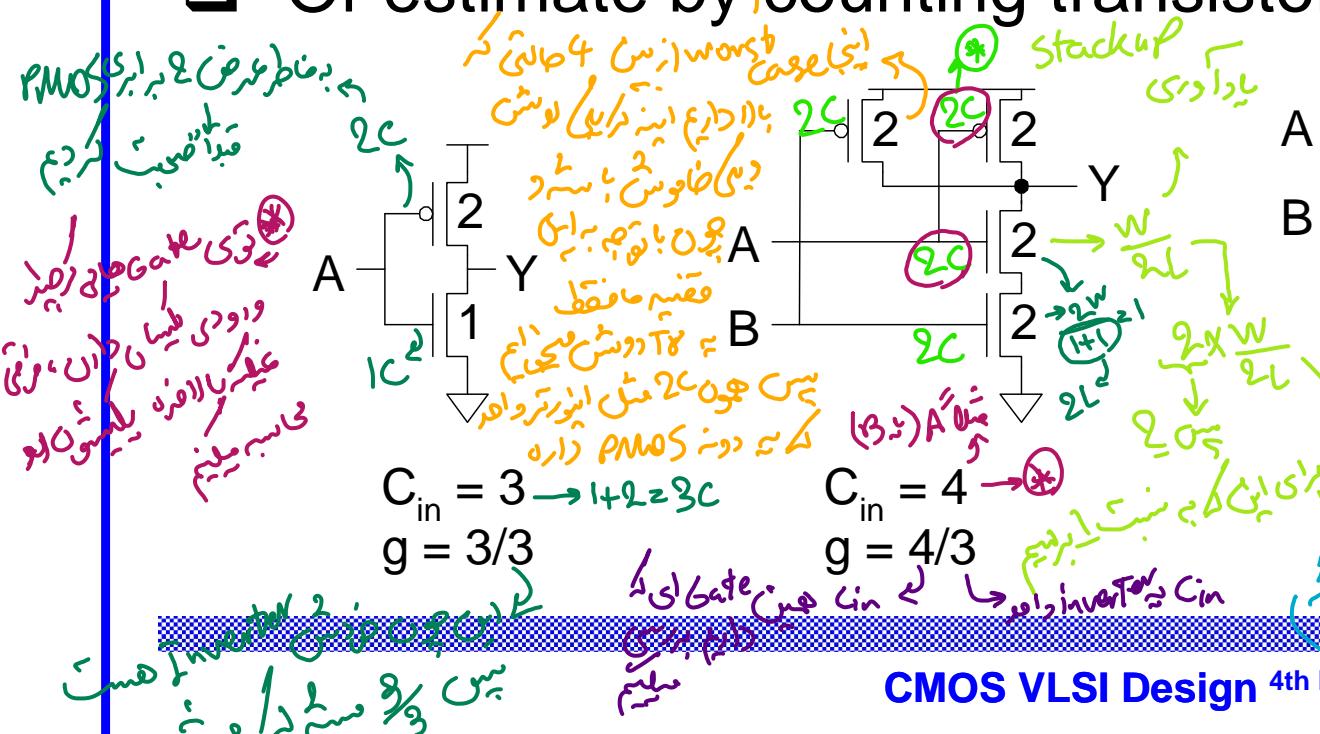


Computing Logical Effort

- DEF: *Logical effort is the ratio of the input capacitance of a gate to the input capacitance of an inverter delivering the same output current.*

- ## □ Measure from delay vs. fanout plots

- Or estimate by counting transistor widths



Catalog of Gates

- Logical effort of common gates

Gate type	Number of inputs				
	1	2	3	4	n
Inverter	1				سبیل مفہوم
NAND		4/3	5/3	6/3	<i>NOR 2 میں مفہوم NAND 3 میں مفہوم</i> (n+2)/3
NOR		5/3	7/3	9/3	تمام (2n+1)/3
Tristate / mux	2	2	2	2	2
XOR, XNOR		4, 4	6, 12, 6	8, 16, 16, 8	

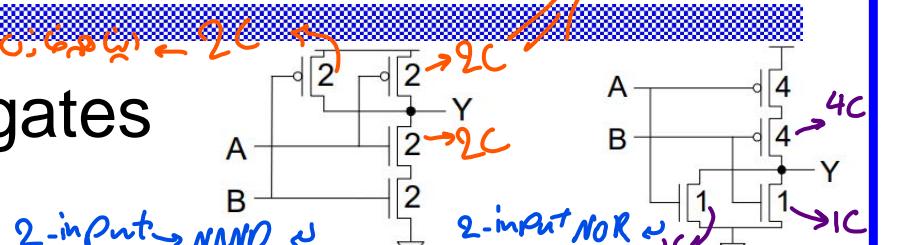
- Compare the growth rate for NAND and NOR!

Parasitic Delay

- ❑ Represents delay of gate driving no load:
 - Set by internal parasitic capacitance
 - ❑ Counts only direct diffusion capacitance on the output node:
 - e.g., unit inverter has 3 units of diffusion capacitance on the output
 - ❑ Definition: p_{inv} is the ratio of diffusion capacitance to gate capacitance of an inverter
 - Also called **normalized parasitic delay**
 - p_{inv} of an inverter is 1
 - ❑ Increasing transistor sizes reduces resistance but increases capacitance:
 - Parasitic delay is independent of gate size
 - ❑ This is inaccurate but it gives a general idea about the delay
- دستورات مذکورهای زیر مانند
بررسی میکنند که از های دودن
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Catalog of Gates

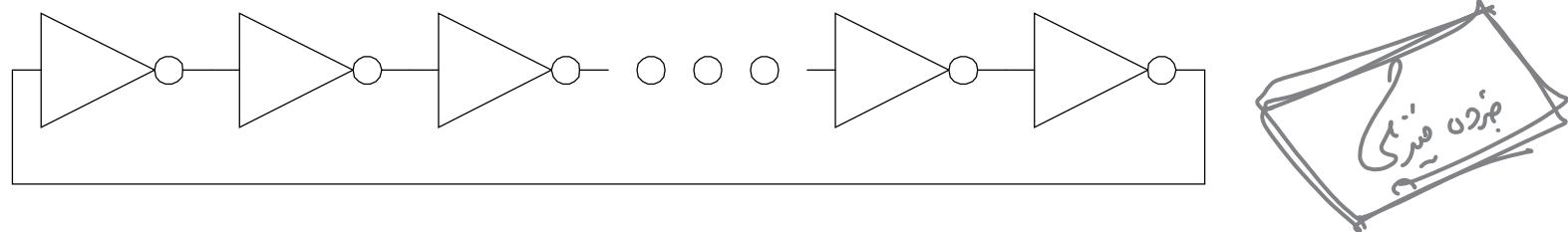
- Parasitic delay of common gates
 - In multiples of p_{inv} (≈ 1)



Gate type	Number of inputs				
	1	2	3	4	n
Inverter	$1 \rightarrow 2 \rightarrow 3$				
NAND	2	$2 \rightarrow 3$	3	4	n
NOR	2	$2 \rightarrow 3$	3	4	n
Tristate / mux	2	4	6	8	$2n$
XOR, XNOR		4	6	8	

Example: Ring Oscillator

- Estimate the frequency of an N-stage ring oscillator



Logical Effort: $g = 1$

Electrical Effort: $h = 1$

Parasitic Delay: $p = 1$

Stage Delay: $d = 2$

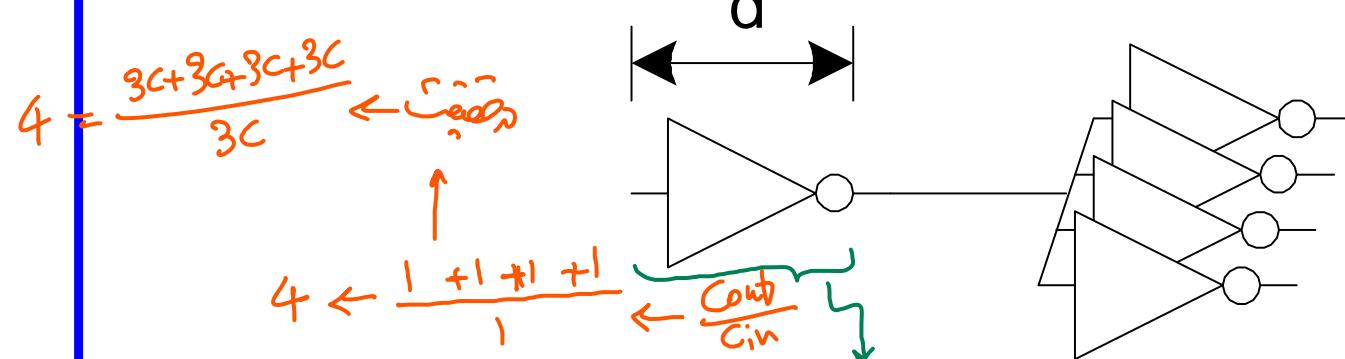
Frequency: $f_{osc} = 1/(2*N*d) = 1/4N$

31 stage ring oscillator in 65 nm process has frequency of ~ 2.7 GHz

اگر ایا میلت افت، مثل میزوه فیزیکی یا دن
شان ۳ تا ۴ بار سرعت بیش دل کن و یعنی N تا
۴ بار بیش

Example: FO4 Inverter

- Estimate the delay of a fanout-of-4 (FO4) inverter



Logical Effort: $g = 1$

Electrical Effort: $h = 4$

Parasitic Delay: $p = 1$

Stage Delay: $d = 5$

$$d = g h r p \Rightarrow d = 1 \times 4 + 1 = 5$$

The FO4 delay is about

300 ps in 0.6 μ m process

15 ps in a 65 nm process

Multistage Logic Networks

- Logical effort generalizes to multistage networks

- *Path Logical Effort*

$$G = \prod g_i$$

لیستهایی و داشته باشی برای Gate و ability Gate برای بار بود

- *Path Electrical Effort*

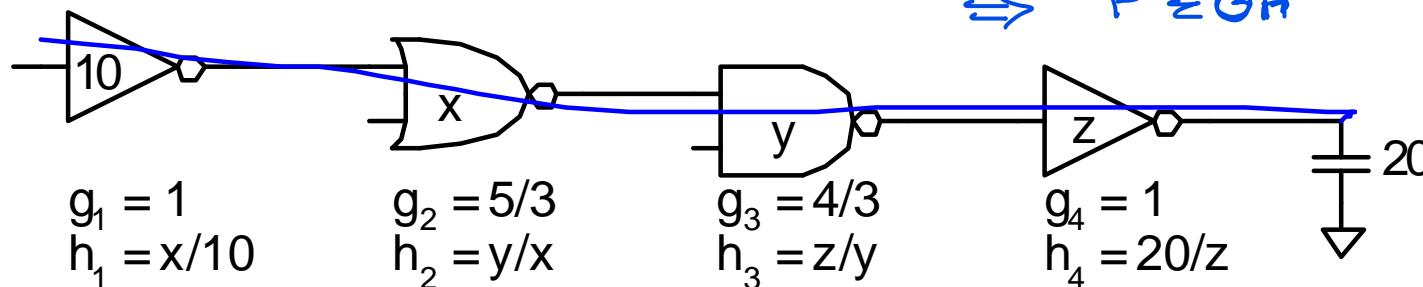
$$H = \frac{C_{\text{out-path}}}{C_{\text{in-path}}}$$

جهن محوت و تغییر های و سلسله های
ساده سینه مثلاً توانی مثل پیوند داریم

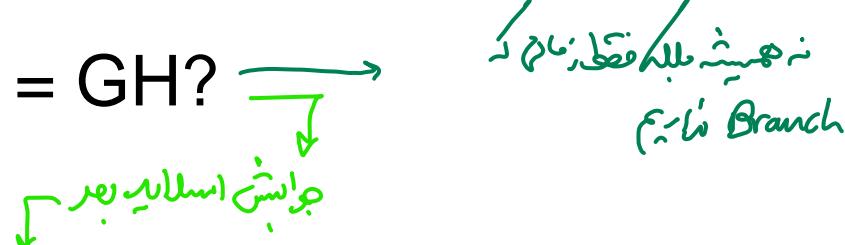
- *Path Effort*

$$F = \prod f_i = \prod g_i h_i$$

$$\Leftrightarrow F \approx GH$$



Multistage Logic Networks

- Logical effort generalizes to multistage networks
- *Path Logical Effort* $G = \prod g_i$
- *Path Electrical Effort* $H = \frac{C_{out-path}}{C_{in-path}}$
- *Path Effort* $F = \prod f_i = \prod g_i h_i$
- Can we write $F = GH$? 

Paths that Branch

- ❑ No! Consider paths that branch:

فیلتر

$$G = 1$$

$$H = 90 / 5 = 18$$

$$GH = 18 \rightarrow \frac{18 \times 1}{5} = 18$$

لذات (عین)

$$h_1 = \frac{(15 + 15)}{5} = 6$$

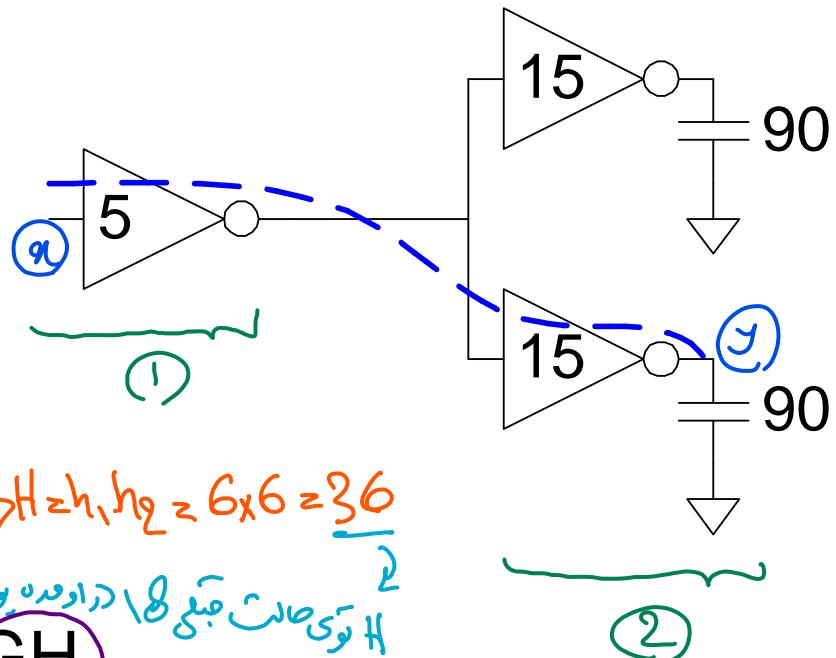
$$h_2 = \frac{90}{15} = 6$$

$$F = g_1 g_2 h_1 h_2 = 36 = 2GH$$

نوعی حالت جمیعی (رادیو وود)

پس از فریول مون را داشتیم

نیز $F = G$



وکی با جوہ این وصیفیات وکی اسلام پر چھپدی
 میادیں جویں قصیر ضرول A_1 ہیں فنیں
 اسیم B کے مقابلہ میں F اپنہ
 ضرول $A_2 = F$ کو لی بڑھ کر
 ضرول A_3 کے مقابلہ میں F رکھ کر قصیر میں

Branching Effort

□ Introduce *branching effort*

- Accounts for branching between stages in path

$$b = \frac{C_{\text{on path}} + C_{\text{off path}}}{C_{\text{on path}}}$$

مسیر دارای خطاین قی اسلایه قبل
مسیر که خطاین فزاره
پس توکشل میوی قبل

ایم مقصودش فرجهز مسیر موردنی هست
مقدور در سریوی هست

یه ضمیب ۲
لیشت هون
اچنافه سینه

$$B = \prod b_i$$

Note:

$$\prod h_i = BH$$

□ Now we compute the path effort

$$F = GBH$$

$$d = f + p \rightarrow d = \underbrace{gh}_{f} + p \rightarrow \text{این چیزها فرآیندهای چند مرحله‌ای هستند برای سیستم‌های} \\ \text{متعدد مرحله دارند و این رسمی نیست}$$

Multistage Delays

□ Path Effort Delay

$$D_F = \sum f_i$$

□ Path Parasitic Delay

$$P = \sum p_i$$

□ Path Delay

$$D = \sum d_i = D_F + P$$

این فرم بایه‌زدگی دارد که برای مقادیر

$$D_F \neq \sum f_i$$

Path Effort Delay

πf_i

این فرم باعث زدگی دارد که برای مقادیر

کلی ممکن است

توی اسوانوی های قبل عقد اول می اسیه صیغه ده معلوم بود و تعداد Stage ها (یعنی تعداد سطح) هم طبق حدارداده شده معلوم بود و سوال اینج بود که تا این سطح کمین موارد می خواهد است که بررسی شد. صلاحدو چو راه تفهیم می گویند تاکه لعنتیم (اکنون دو میلیون و نیم) پذیر صیغه دادم می گویند و نیم مسوال اینه که اچیه Stage بین اینها بینانی داشته باشند.

Designing Fast Circuits

$$D = \sum d_i = D_F + P$$

- Delay is smallest when each stage bears same effort

$$\hat{f} = g_i h_i = F^{\frac{1}{N}}$$

□ Thus minimum delay of N stage path is

$$D = NF^{\frac{1}{N}} + P$$

الله اولاً دلالة مثبتة مبنية على ازاي راحه
استفاده از این دلالة که کمینه لایه دست بداری
(ک)

همون داشتند که سیز
 سیز داریم \rightarrow حاجی هم نمیشون
 آنچه داشت، پیش از آنکه کنم که
حاجی هم نمیشون \rightarrow min شوی
 این (قیقا) \downarrow
 همین F و قیقا این آنچه داریم \rightarrow دیر
 همین و این مقدار بیش نمیشون

This is a **key** result of logical effort \min^2 D_f \downarrow $\sum f_i$

- Finds the fastest possible delay
- Doesn't require calculating gate sizes

Gate Sizes

- How wide should the gates be for least delay?

$$\hat{f} = gh = g \frac{C_{out}}{C_{in}}$$

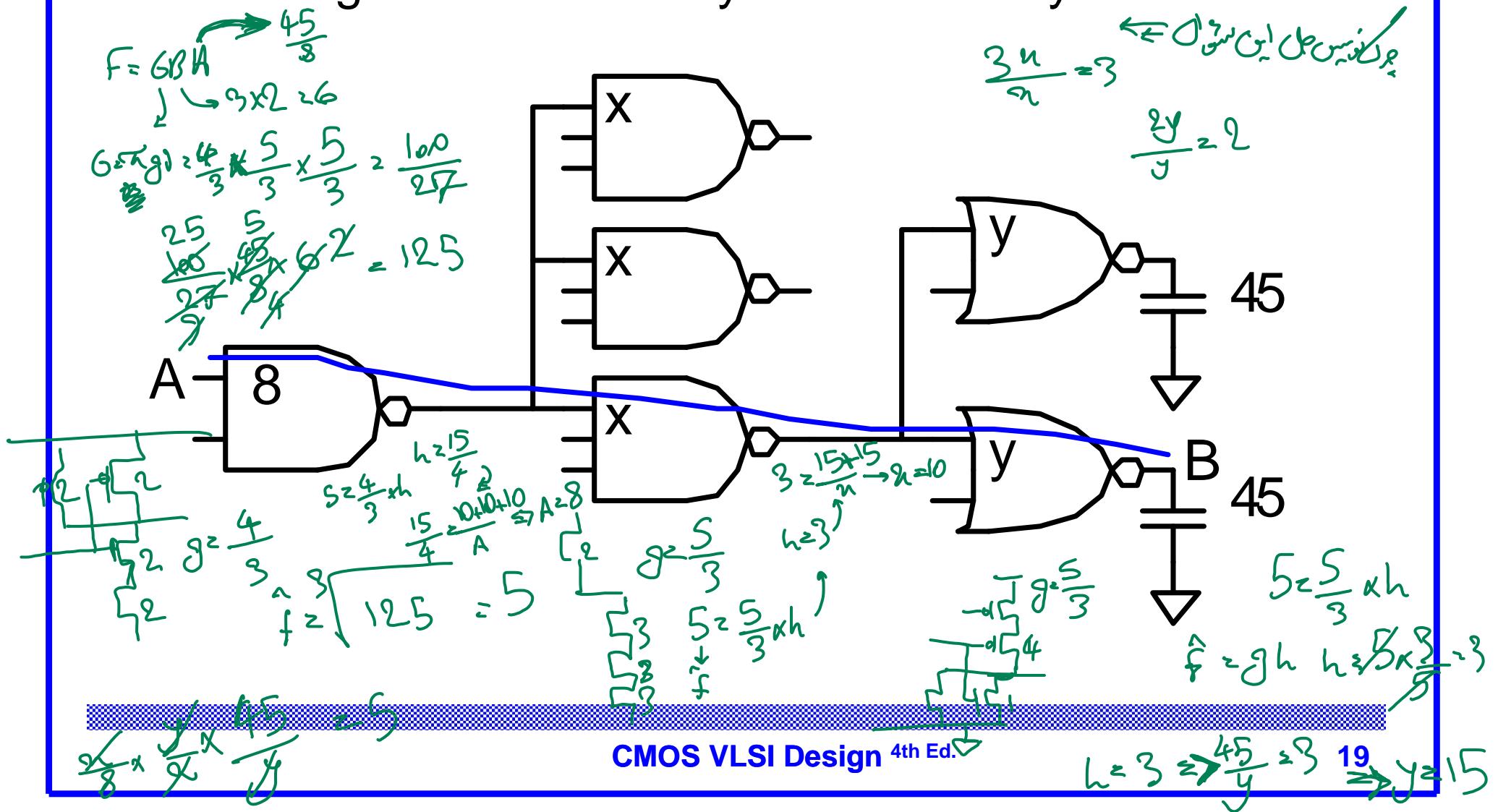
$$\Rightarrow C_{in_i} = \frac{g_i C_{out_i}}{\hat{f}}$$

میں کے یہ 06 و جزوی صیزی کے
وچھے load رہیں ہے، ازاً مزید یا بارہ
بہتر اور دفعہ سینمی قابو سیکھ کے نسبت W/L میں جو ہے

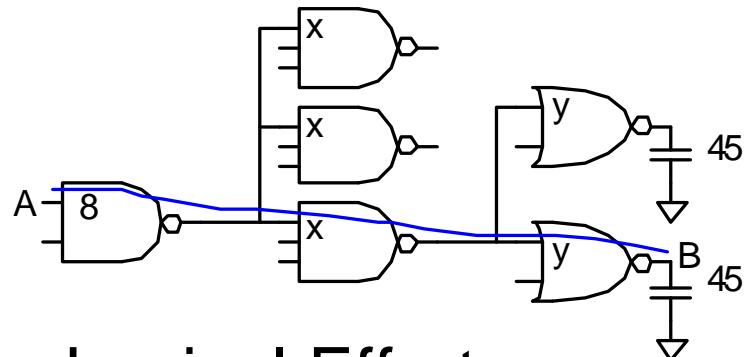
- Working backward, apply capacitance transformation to find input capacitance of each gate given load it drives.
- Check work by verifying input cap spec is met.

Example: 3-stage path

- Select gate sizes x and y for least delay from A to B



Example: 3-stage path



Logical Effort

$$G = (4/3) * (5/3) * (5/3) = 100/27$$

Electrical Effort

$$H = 45/8$$

Branching Effort

$$B = 3 * 2 = 6$$

Path Effort

$$F = GBH = 125$$

Best Stage Effort

$$125^{1/3} = 5$$

Parasitic Delay

$$P = 2 + 3 + 2 = 7$$

Delay

$$D = 3 * 5 + 7 = 22 = 4.4 \text{ FO4}$$

Example: 3-stage path

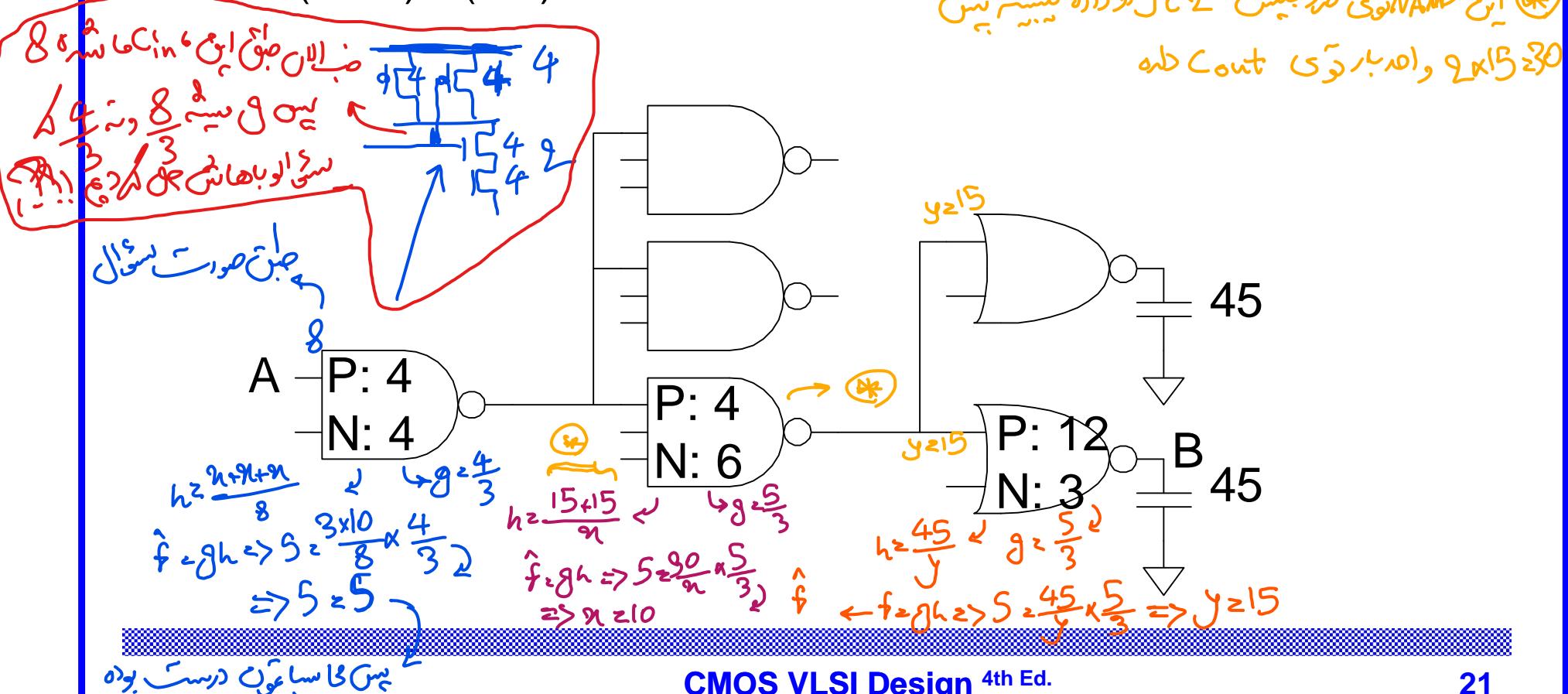
- ## ☐ Work backward for sizes

$$y = 45 * (5/3) / 5 = 15$$

$$x = (15*2) * (5/3) / 5 = 10$$

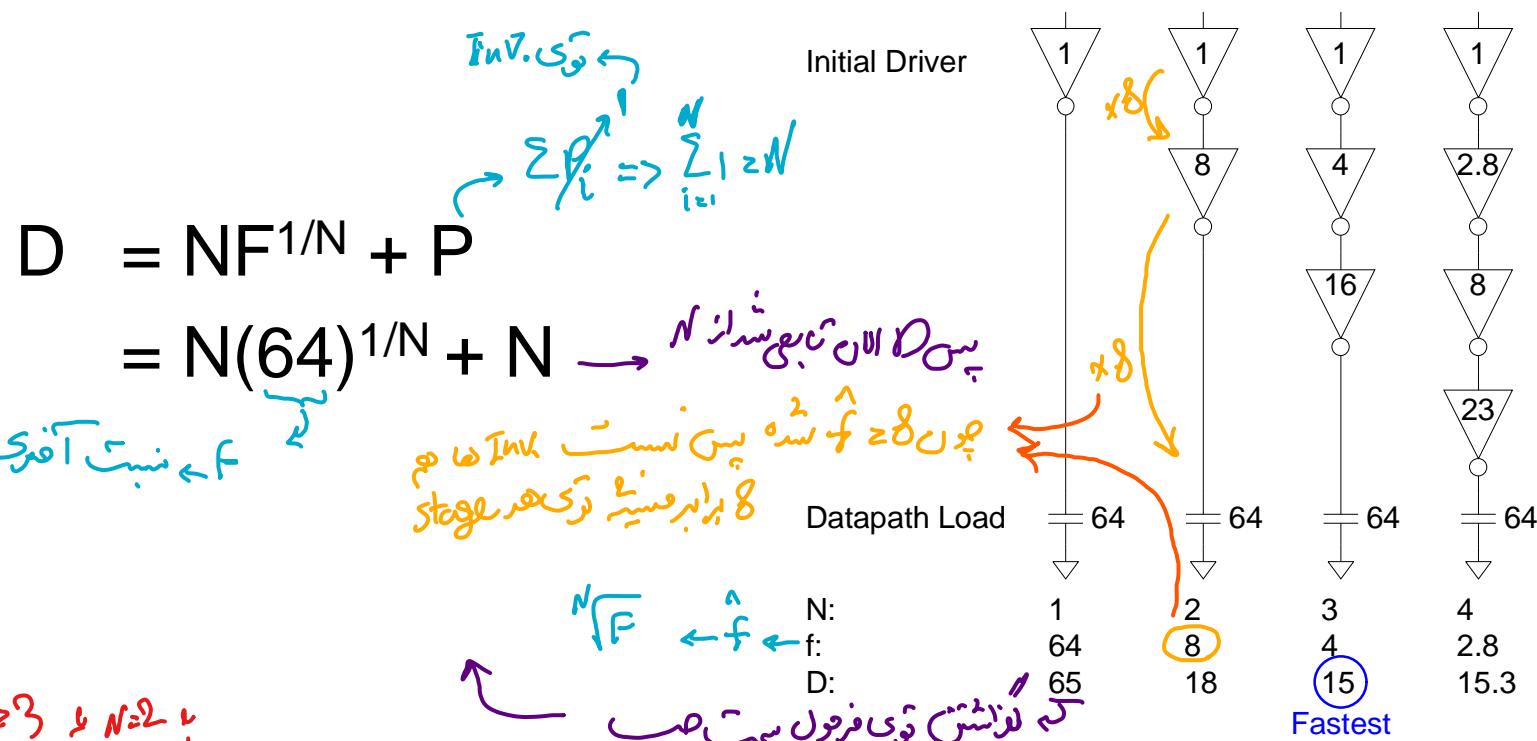
- ## Verify the first stage:

$$(10^*3/8) * (4/3) = 5$$



Best Number of Stages

- How many stages should a path use?
 - Minimizing number of stages is not always fastest
 - Example: drive 64-bit datapath with unit inverter



Derivation

- Consider adding inverters to end of path *subStage 1 to N* (مجموع)

– How many give least delay?

$$D = NF^{\frac{1}{N}} + \sum_{i=1}^{n_1} p_i + (N - n_1) p_{inv}$$

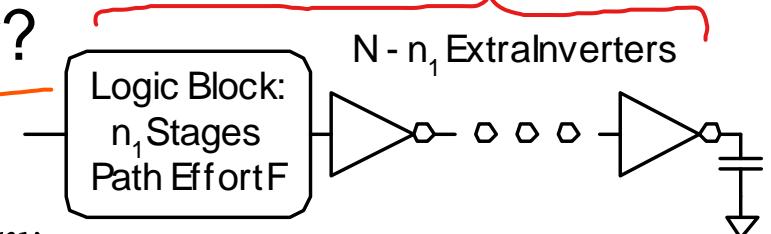
جہاز دیویون بون لیٹنگ inv. ڈیلیٹنگ

$$\frac{\partial D}{\partial N} = -F^{\frac{1}{N}} \ln F^{\frac{1}{N}} + F^{\frac{1}{N}} + p_{inv} = 0$$

سیب ڈیلی نتھے entremum شکستی

- Define best stage effort $\rho = F^{\frac{1}{N}}$

$$p_{inv} + \rho(1 - \ln \rho) = 0$$



Note: This equation assumes that all added inverters are unit inverters.

پر خوف، خوف (جیع نیت چون علی ائمہ
تھا بایر، بایر، بایر، بایر، بایر، بایر،
ھر stage ڈیلی خوب دفعے متعدد
میرفت تھی بیتھنے تھے (constant) پس سیل
تھی خاصی ھے نہ

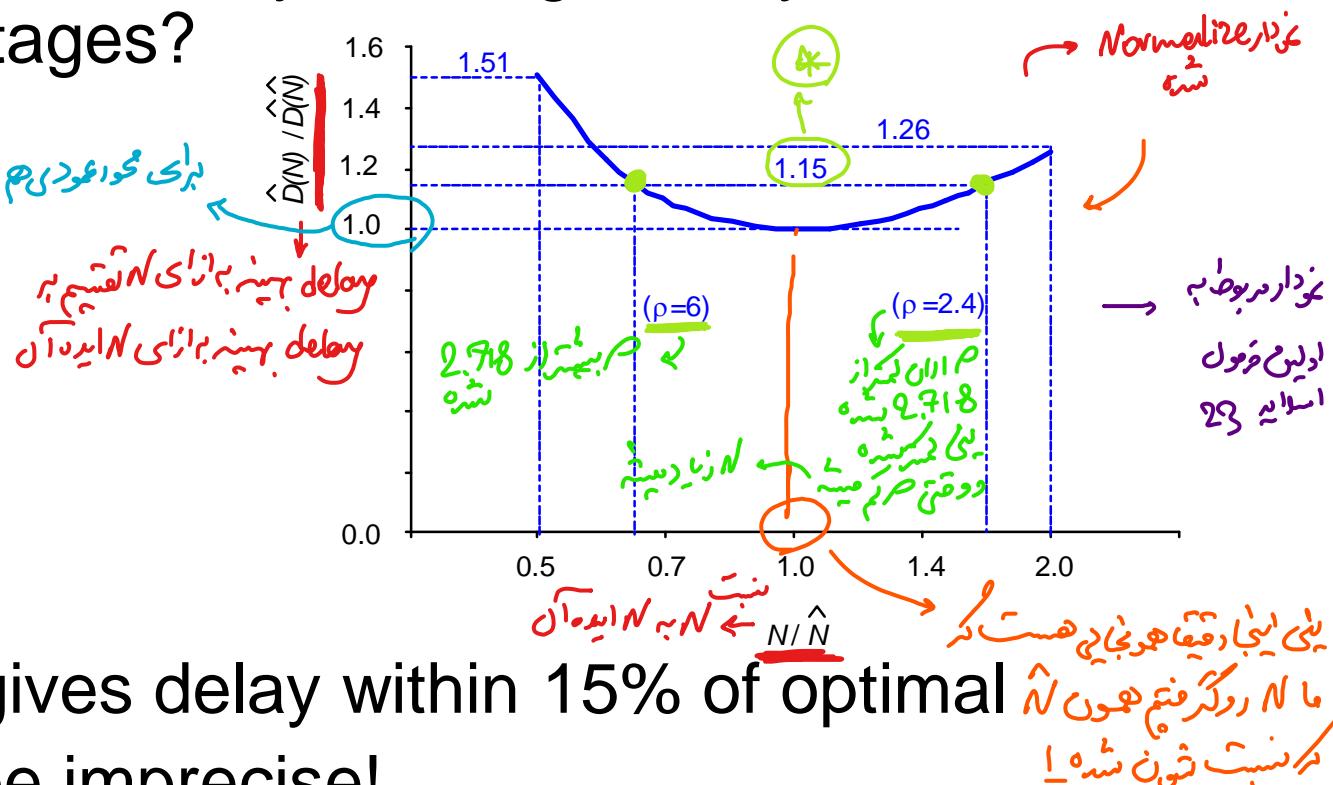
Best Stage Effort

- ❑ $p_{inv} + \rho(1 - \ln \rho) = 0$ has no closed-form solution
- ❑ Neglecting parasitics ($p_{inv} = 0$), we find $\rho = 2.718$ (e)
- ❑ For $p_{inv} = 1$, solving numerically gives $\rho = 3.59$
- ❑ \hat{N} can be found from $\hat{N} = \log_{\rho} F$
- ❑ Need to find an integer close to it:
 - Increasing ρ and decreasing \hat{N} => lower parasitic delay
 - Decreasing ρ and increasing \hat{N} => higher parasitic delay
- ❑ The first approach is usually taken

Sensitivity Analysis

- How sensitive is delay to using exactly the best number of stages?

برای محو عودی هم چون دستگاه مورفیک بفراره بین این \hat{N} و N داشته باشند
در بینین حالات ممکن است
و نمیشه شده



- $2.4 < \rho < 6$ gives delay within 15% of optimal
 - We can be imprecise!
 - Typically $\rho = 4$

Summary

❑ Method of Logical Effort:

- 1) Compute path effort $F = GBH$
- 2) Estimate best number of stages $N = \log_4 F$
Typically $P=4$
- 3) Sketch path with N stages
- 4) Estimate least delay $D = NF^{\frac{1}{N}} + P$
- 5) Determine best stage effort $\hat{f} = F^{\frac{1}{N}}$
- 6) Find gate sizes $C_{in_i} = \frac{g_i C_{out_i}}{\hat{f}}$

Homework Assignments

- ❑ Chapter 4: 4.5 to 4.10
- ❑ For Tuesday 1402/9/14