Stratix® V Featured Documentation – Quick Links Guide

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Contents

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Stratix® V Featured Documentation - Quick Links

This page provides links to some of the key Stratix® V documentation, organized by focused subject areas.

Featured Documents

Stratix V FPGA Product Table	Device overview	Datasheet
Stratix V Military Temperature Range Support Technical Brief	Stratix V Design Guidelines	Errata sheet
Stratix V Device Handbook: Volume 1: Device Interfaces and Integration	Stratix V Device Handbook: Volume 2: Transceivers	AN 644: Migration Between Stratix V GX and Stratix V GT Devices
Package and Thermal specifications	Device pin-outs	Pin connection guidelines

See All Stratix V Resources and Documentation

Device Handbook Sections

1. **Stratix V Device Handbook: Volume 1: Device Interfaces and Integration**
   - **Section I. Device Core**
     - Chapter 1. Logic Array Blocks and Adaptive Logic Modules
     - Chapter 2. Embedded Memory Blocks
     - Chapter 3. Variable Precision DSP Blocks
     - Chapter 4. Clock Networks and PLLs
   - **Section II. I/O Interfaces**
     - Chapter 5. I/O Features
     - Chapter 6. High-Speed Differential I/O Interfaces and DPA
     - Chapter 7. External Memory Interfaces
   - **Section III. System Integration**
     - Chapter 8. Configuration, Design Security, and Remote System Upgrades
     - Chapter 9. SEU Mitigation
     - Chapter 10. JTAG Boundary-Scan Testing
     - Chapter 11. Power Management
2. **Volume 2 - Stratix V Device Handbook: Transceivers**
   - Chapter 1. Transceiver Architecture
   - Chapter 2. Transceiver Clocking
   - Chapter 3. Transceiver Reset Control

- Chapter 4. Transceiver Configurations
- Chapter 5. Transceiver Loopback Support
- Chapter 6. Dynamic Reconfiguration

Power and Thermal Management

- PowerPlay Early Power Estimator User Guide
- Device-Specific Power Delivery Network (PDN) Tool 2.0 User Guide
- Power Delivery Network (PDN) Tool 2.0 for Stratix V, Arria V, Arria II GZ, Cyclone V, and Cyclone IV Devices
- AN 750: Using the Altera PDN Tool to Optimize Your Power Delivery Network Design

External Memory Interfaces

- External Memory Interface Handbook Volume 1: Intel FPGA Memory Solution Introduction and Design Flow: For UniPHY-based Device Families
- External Memory Interface Handbook Volume 2: Design Guidelines: For UniPHY-based Device Families
- External Memory Interface Handbook Volume 3: Reference Material: For UniPHY-based Device Families

Design Guidelines

- Stratix V Design Guidelines
- Stratix V GT Device Family Pin Connection Guidelines
- Stratix V ES, GS and GX Device Family Pin Connection Guidelines

Development Kits

- Stratix V GX FPGA Development Board Reference Manual
- Stratix V GX FPGA Development Kit User Guide
- Stratix V GX 100G Development Kit User Guide
- Stratix V Advanced Systems Development Board Reference Manual
- Stratix V Advanced Systems Development Kit User Guide
- DSP Development Board, Stratix V Edition, User Guide
- Signal Integrity Development Kit, Stratix® V GX Edition, User Guide
- Signal Integrity Development Kit, Stratix® V GT Edition User Guide
- Transceiver Signal Integrity Development Kit, Stratix® V GX Edition Reference Manual
- Transceiver Signal Integrity Development Kit, Stratix® V GT Edition Reference Manual
- USB-Blaster Download Cable User Guide
- Partner Boards

Software Documentation

- Intel Quartus Prime Standard Edition User Guides - Combined PDF
- All Software Documentation

IP Documentation

- Advanced SEU Detection Intel FPGA IP User Guide
- ALTLVDS IP Core User Guide
- CPRI Intel FPGA IP User Guide
- DisplayPort Intel FPGA IP User Guide
- Embedded Peripherals IP User Guide
- FIFO Intel FPGA IP User Guide
- JESD204B Intel FPGA IP User Guide
- Remote Update Intel FPGA IP User Guide
- Serial Lite III Streaming Stratix V FPGA IP Design Example User Guide
- Stratix V Avalon-MM Interface for PCIe Solutions: User Guide
- Stratix V Avalon-ST Interface for PCIe Solutions: User Guide
- Stratix V Avalon-ST Interface with SR-IOV PCIe Solutions: User Guide
- Triple-Speed Ethernet Intel FPGA IP User Guide
- V-Series Transceiver PHY IP Core User Guide
- All Stratix V Related IP Documentation

Application Notes

- AN 634: PHY IP Design Flow with Interlaken for Stratix V Devices
- AN639: Inferring Stratix V DSP Blocks for FIR Filtering Applications
- AN 644: Migration Between Stratix V GX and Stratix V GT Devices
- AN 645: Dynamic Reconfiguration of PMA Controls in Stratix V Devices
- AN 664: Using the Stratix V Reconfiguration Controller to Perform Dynamic Reconfiguration
- AN 670: Thermal Solutions to Address Height Variation in Stratix V Packages
- AN 684: 100 Gbps CFP2 Design with Stratix V GT FPGAs
- AN 687: Implementing QPI Using the Transceiver Native PHY IP Core in Stratix V Devices
- AN 713: DC Coupling in Stratix V Devices
- AN 782: Interlaken IP Core Feature and Interface Differences Between Intel Stratix 10, Intel Arria 10, and Stratix V Devices
- AN 809: SerialLite III IP Core Feature and Interface Differences between Stratix 10, Arria 10, and Stratix V
- All Stratix V Related Application Notes