

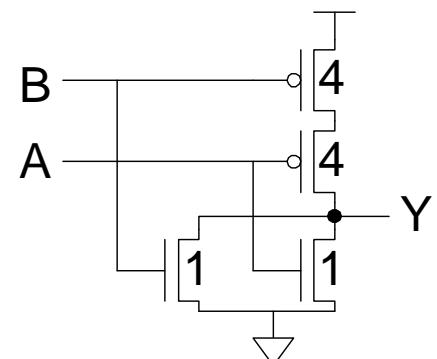
Combinational Circuit Design: Extended CMOS

Outline

- Pseudo-nMOS Logic
 - Dynamic Logic
 - Pass Transistor Logic
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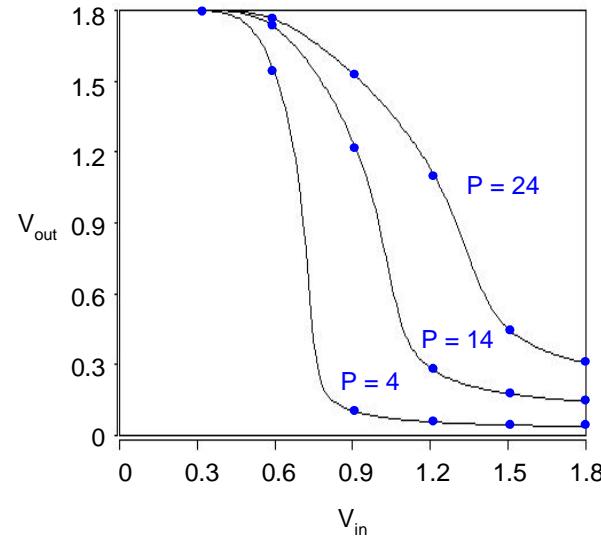
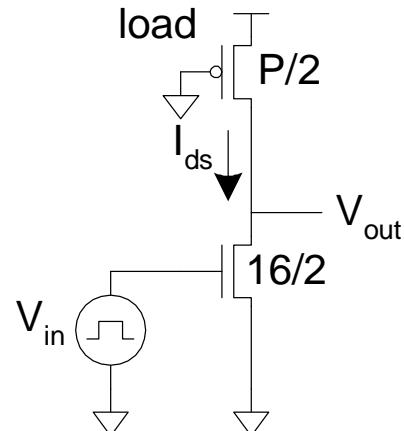
Introduction

- What makes a circuit fast?
 - $I = C \frac{dV}{dt} \rightarrow t_{pd} \propto (C/I) \Delta V$
 - Lower capacitance
 - Higher current
 - Smaller swing
- Logical effort is proportional to C/I
- pMOS is the enemy!
 - High capacitance for a given current
- Can we take the pMOS capacitance off the input?
- Various circuit families try to do this...



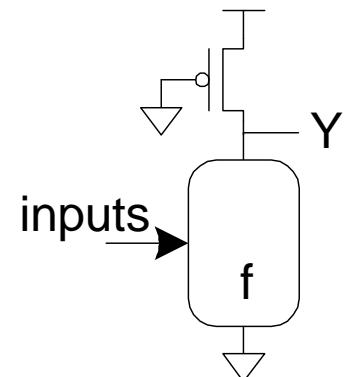
Pseudo-nMOS

- In the old days, nMOS processes had no pMOS
 - Instead, used pull-up transistor that is always ON
- In CMOS, use a pMOS that is always ON
 - *Ratio* issue
 - Make pMOS about $\frac{1}{4}$ effective strength of pulldown network

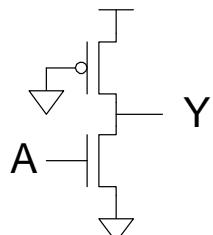


Pseudo-nMOS Gates

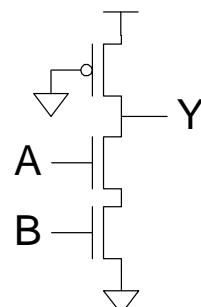
- Design for unit current on output to compare with unit inverter
- pMOS fights nMOS



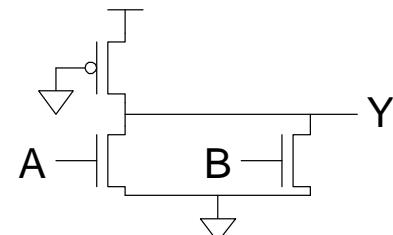
Inverter



NAND2



NOR2

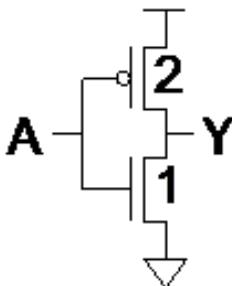


Pseudo-nMOS Gates

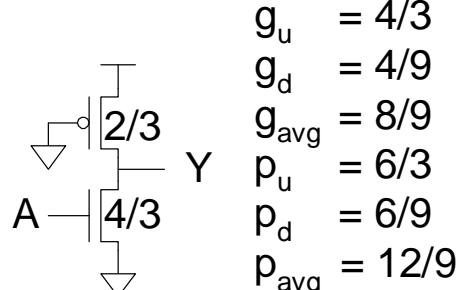
- The logical effort for each transition is computed as the ratio of the input capacitance to that of a complementary CMOS inverter with equal current for that transition.

- Pull down:

compare with

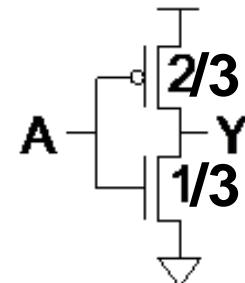


Inverter

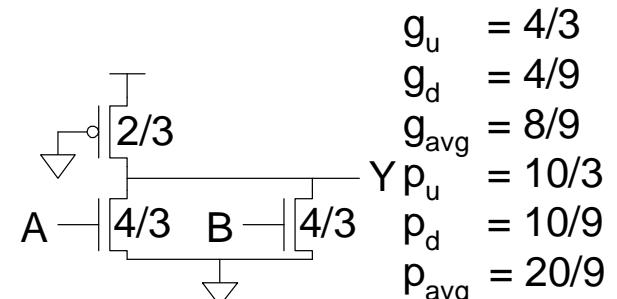
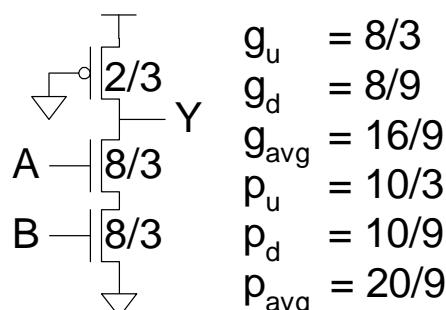


- Pull up:

compare with



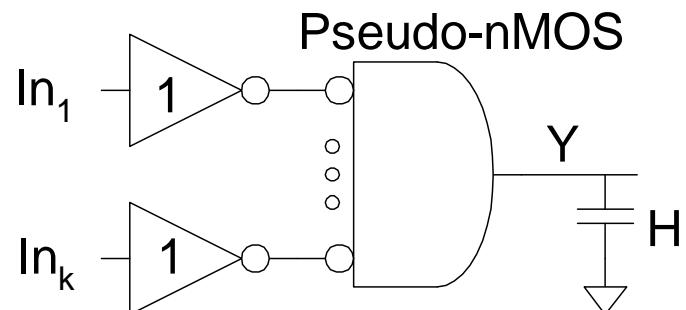
NOR2



Pseudo-nMOS Design

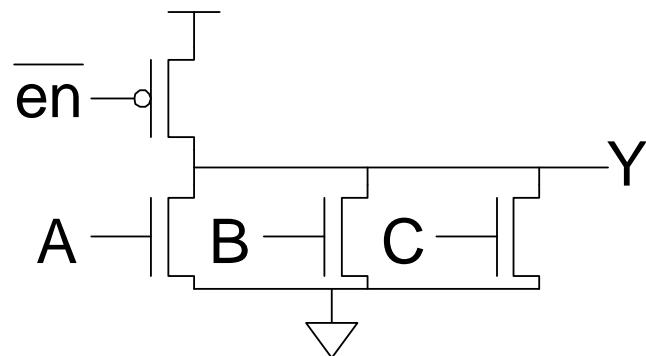
- Ex: Design a k-input AND gate using pseudo-nMOS. Estimate the delay driving a fanout of H

- $G = 1 * 8/9 = 8/9$
- $F = GBH = 8H/9$
- $P = 1 + (4+8k)/9 = (8k+13)/9$
- $N = 2$
- $D = NF^{1/N} + P$



Pseudo-nMOS Power

- ❑ Pseudo-nMOS draws power whenever $Y = 0$
 - Called static power $P = I_{DD}V_{DD}$
 - A few mA / gate * 1M gates would be a problem
 - Explains why nMOS went extinct
- ❑ Use pseudo-nMOS sparingly for wide NORs
- ❑ Turn off pMOS when not in use



Ratio Example

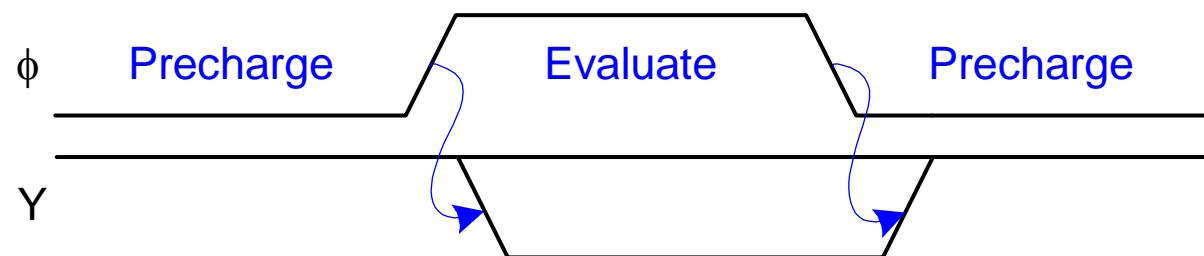
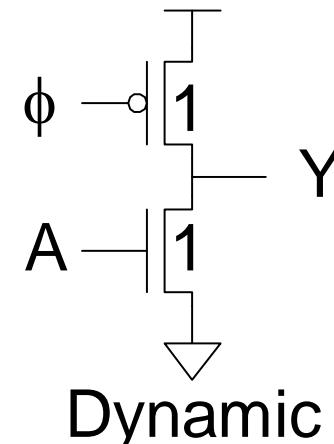
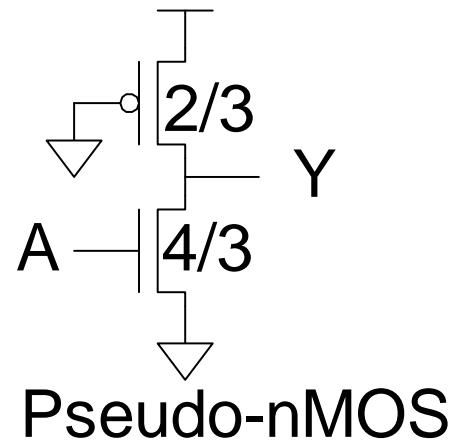
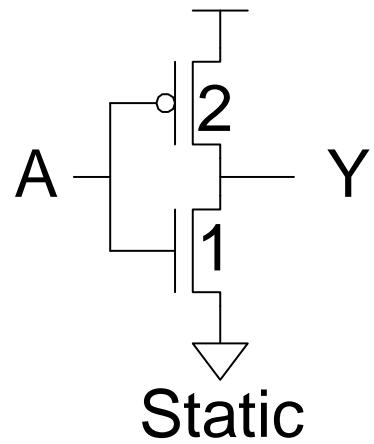
- A chip contains a 32 word x 48 bit ROM
 - Uses pseudo-nMOS decoder and bitline pullups
 - On average, one wordline and 24 bitlines are high
- Find static power drawn by the ROM
 - $I_{on-p} = 36 \mu A$, $V_{DD} = 1.0 V$
- Solution:

$$P_{\text{pull-up}} = V_{DD} I_{\text{pull-up}} = 36 \mu W$$

$$P_{\text{static}} = (31 + 24)P_{\text{pull-up}} = 1.98 mW$$

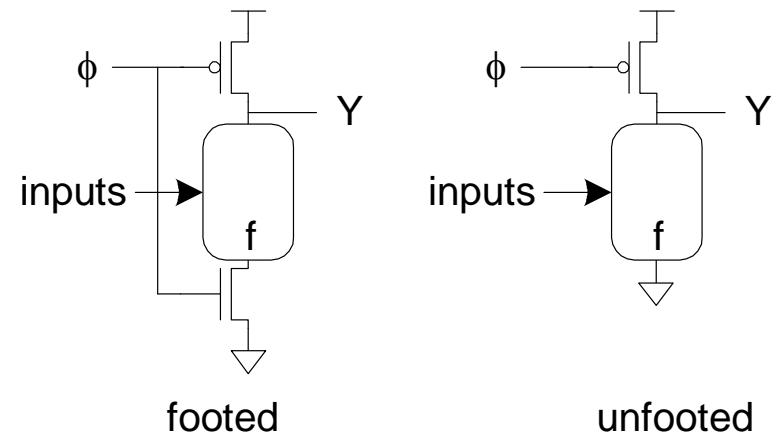
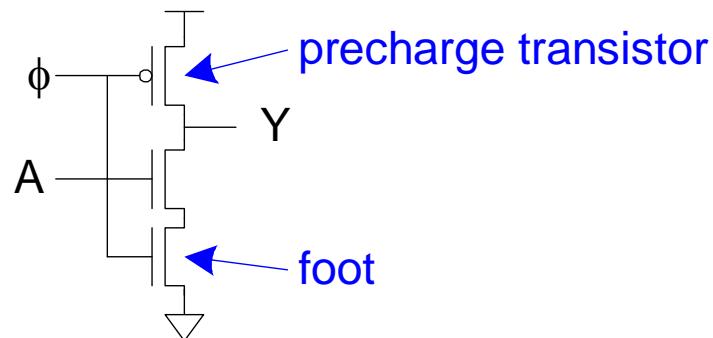
Dynamic Logic

- *Dynamic* gates use a clocked pMOS pullup
- Two modes: *precharge* and *evaluate*

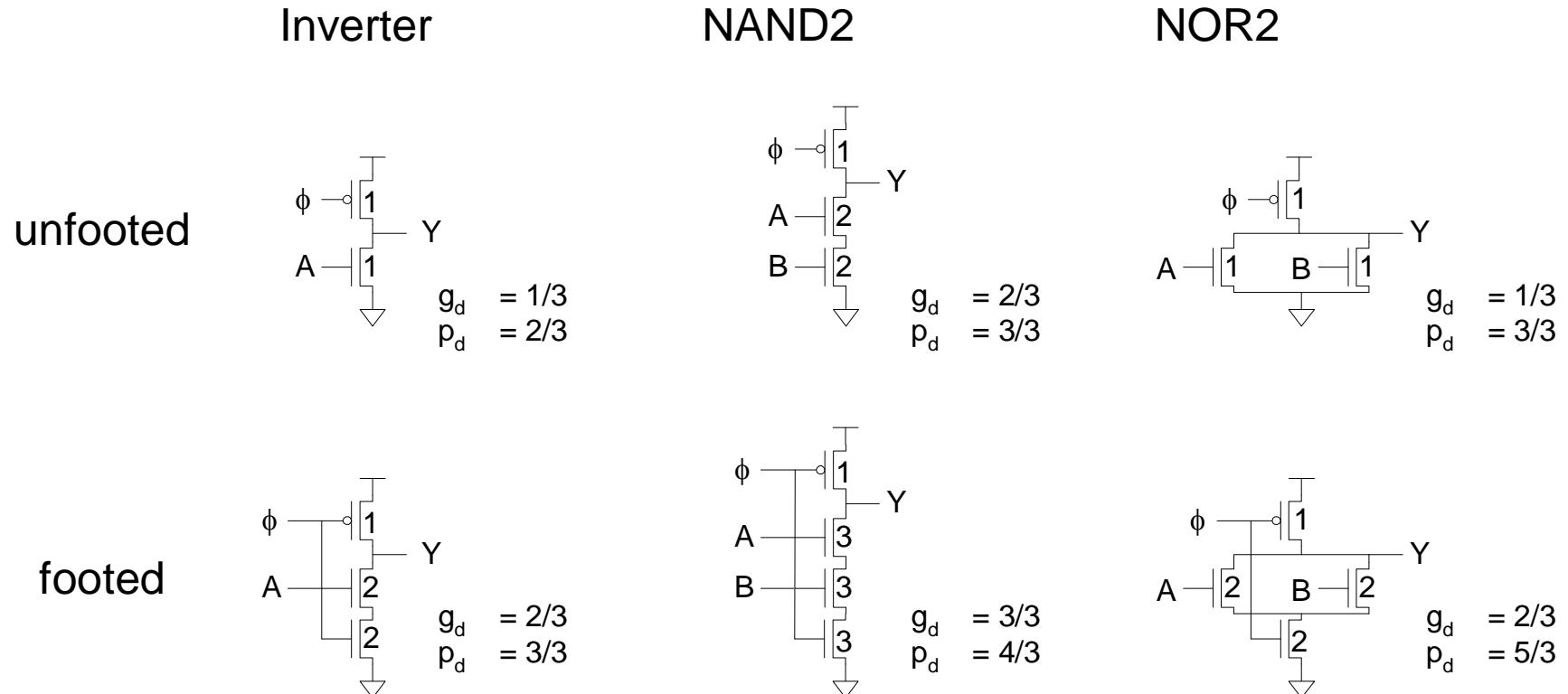


The Foot

- ❑ What if pulldown network is ON during precharge?
- ❑ Use series evaluation transistor to prevent fight.

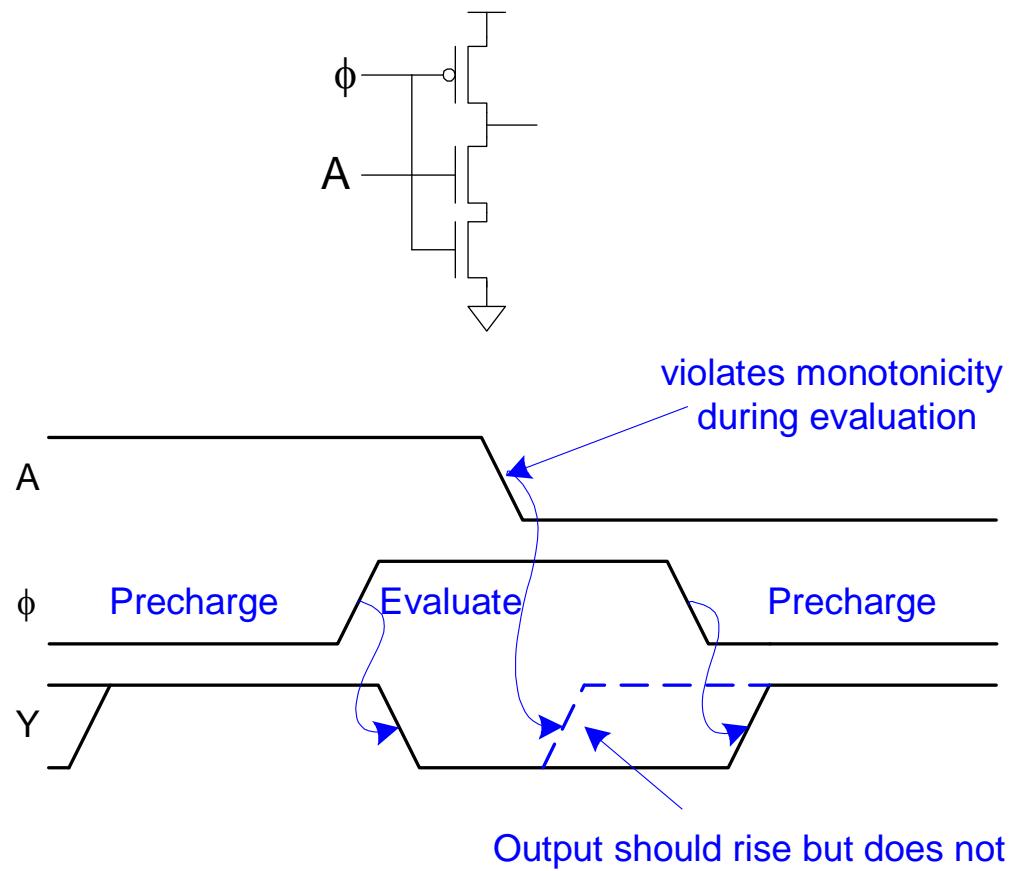


Logical Effort



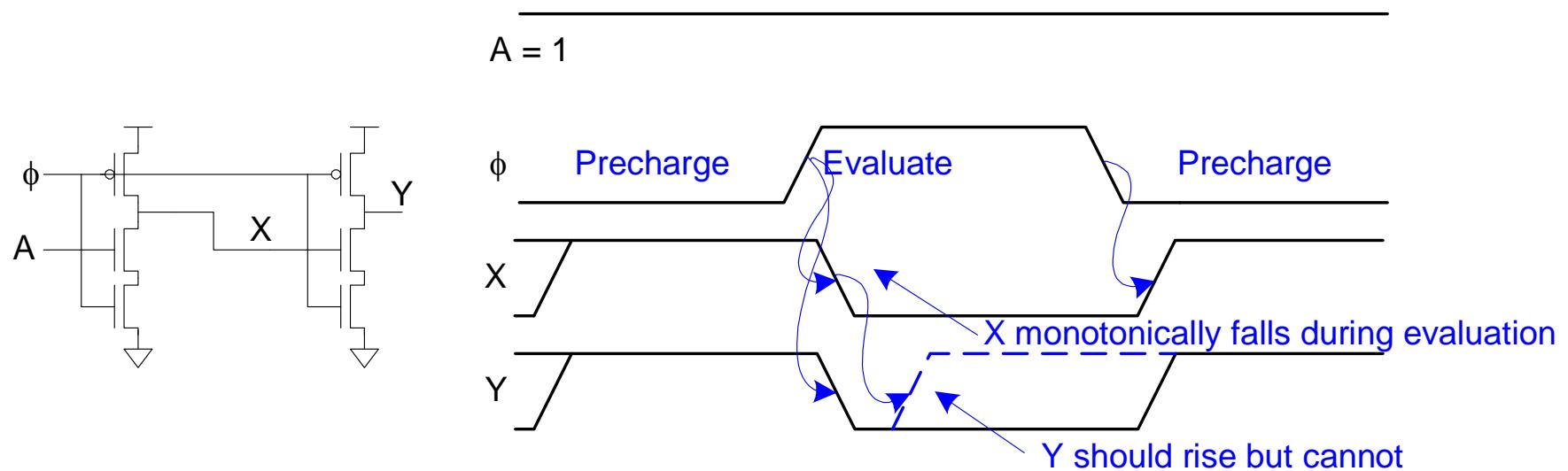
Monotonicity

- Dynamic gates require *monotonically rising* inputs during evaluation



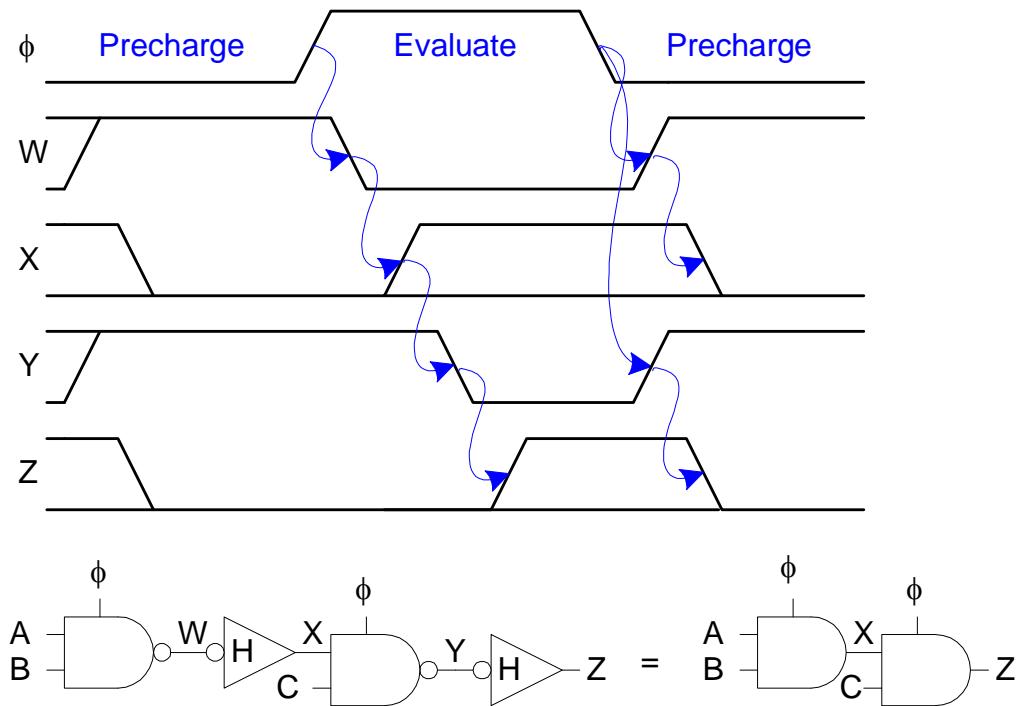
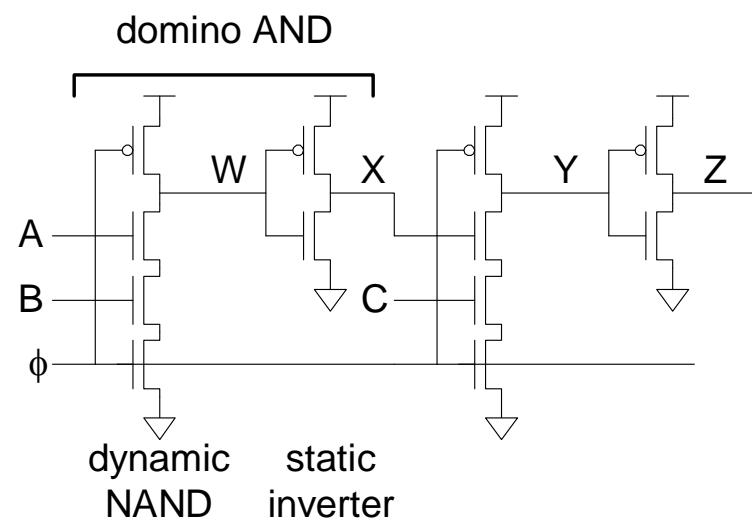
Monotonicity Woes

- ❑ But dynamic gates produce monotonically falling outputs during evaluation
- ❑ Illegal for one dynamic gate to drive another!



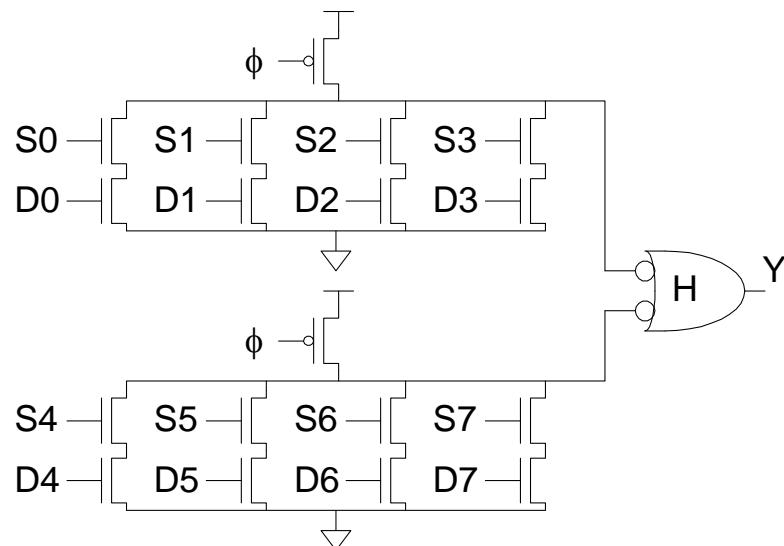
Domino Gates

- Follow dynamic stage with inverting static gate
 - Dynamic / static pair is called domino gate
 - Produces monotonic outputs



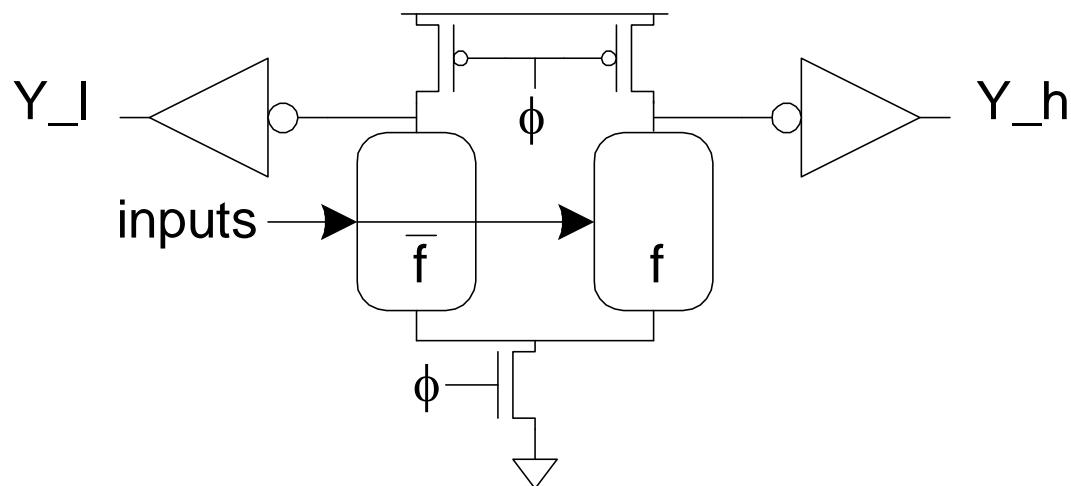
Domino Optimizations

- Each domino gate triggers next one, like a string of dominos toppling over
- Gates evaluate sequentially but precharge in parallel
- Thus evaluation is more critical than precharge
- HI-skewed static stages can perform logic
- Example: 8-bit MUX



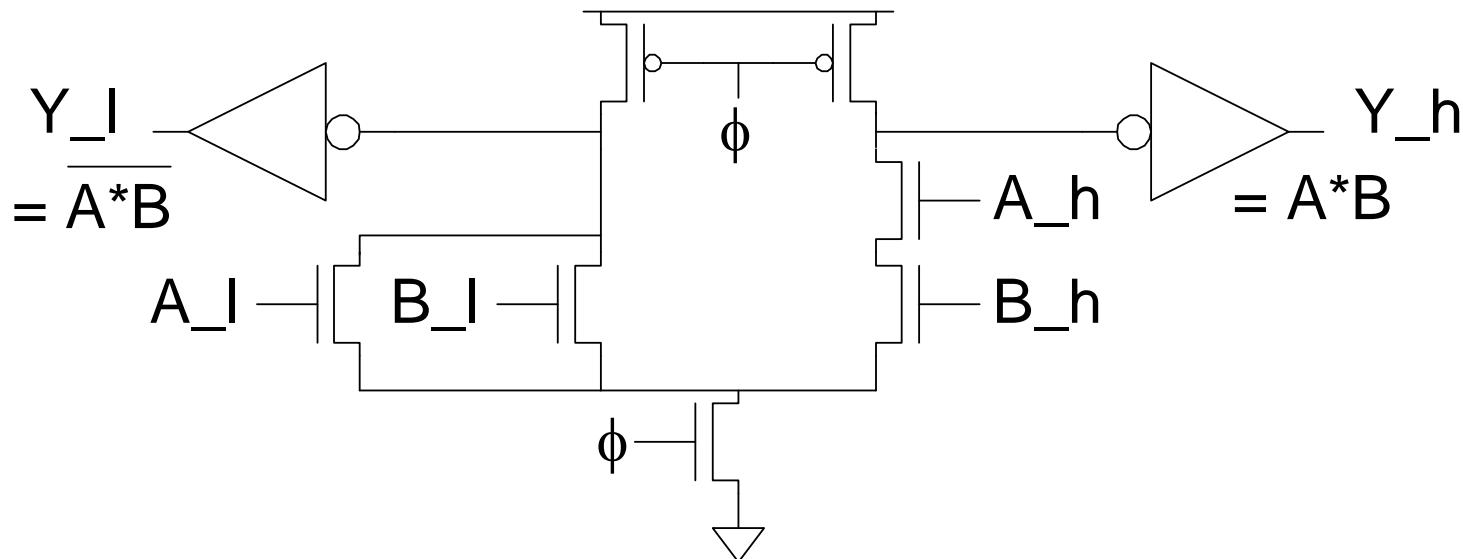
Dual-Rail Domino

- Domino only performs noninverting functions:
 - AND, OR but not NAND, NOR, or XOR
- Dual-rail domino solves this problem
 - Takes true and complementary inputs
 - Produces true and complementary outputs
 - Similar to Cascode Voltage Switch Logic (CVSL)



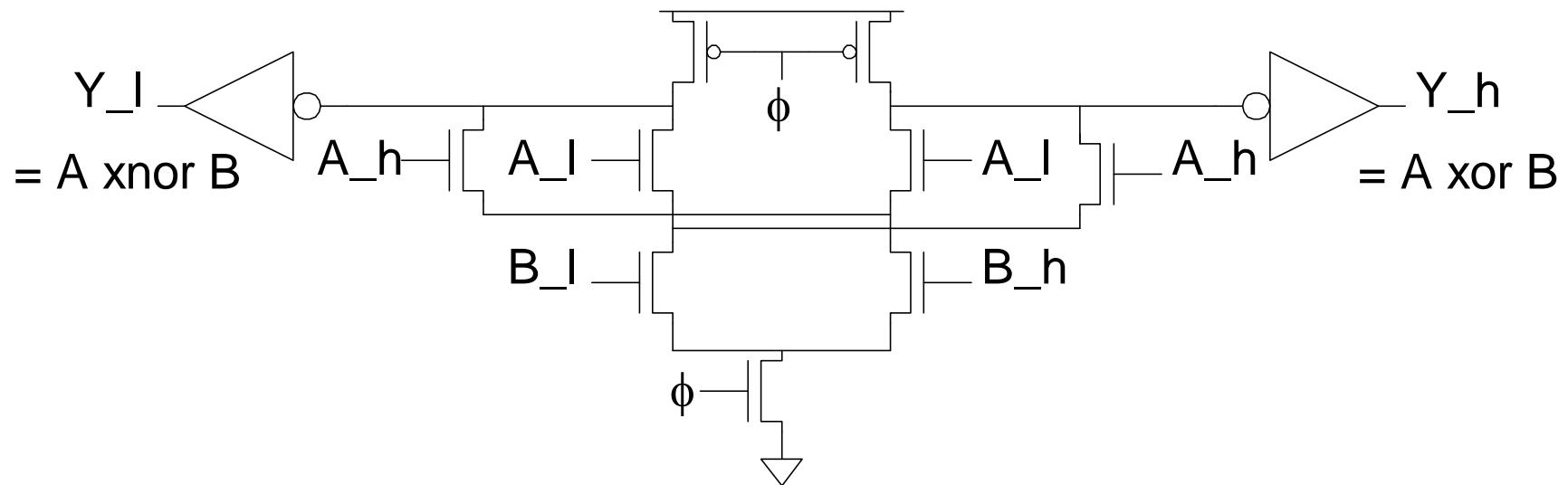
Example: AND/NAND

- Given A_h, A_I, B_h, B_I
- Compute $Y_h = AB, Y_I = \overline{AB}$
- Pulldown networks are conduction complements
- Observe the duality of PDN and PUN



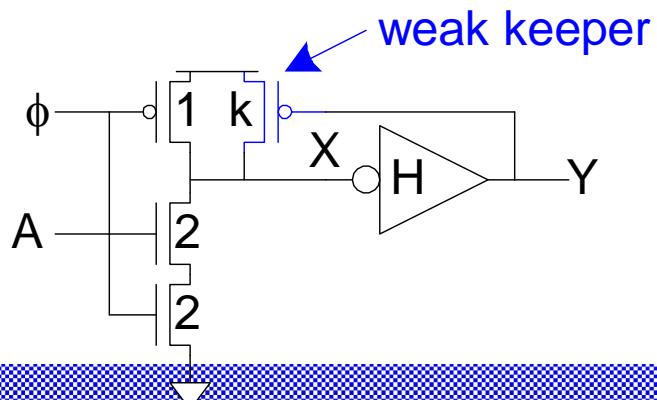
Example: XOR/XNOR

- ❑ Sometimes possible to share transistors
- ❑ Turns the duality into mirror image
- ❑ 13 transistor for two gates (excluding input inverters)



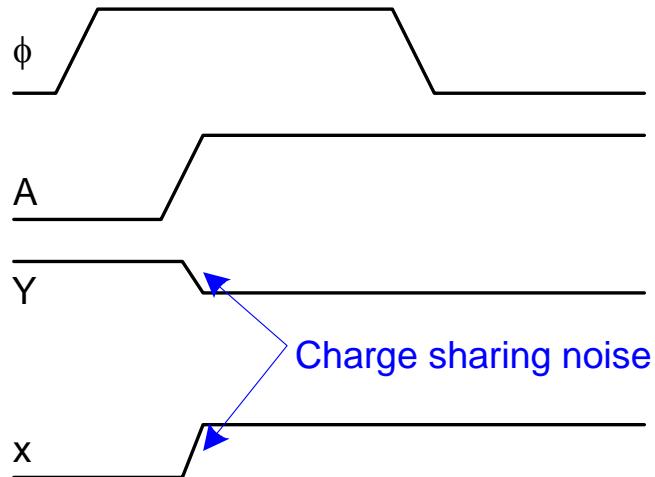
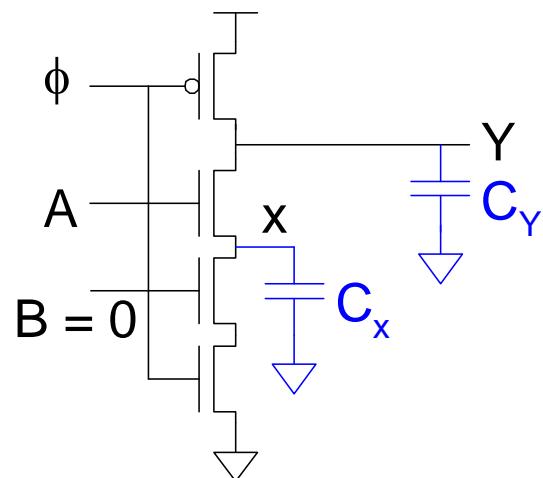
Leakage

- Dynamic node floats high during evaluation
 - Have to rely on output capacitors to hold 1
 - Transistors are leaky ($I_{OFF} \neq 0$)
 - Noise can turn input transistors on momentarily
 - Result: dynamic value of 1 will leak away over time
 - Formerly milliseconds, now nanoseconds
- Use keeper to hold dynamic node
 - Must be weak enough not to fight evaluation



Charge Sharing

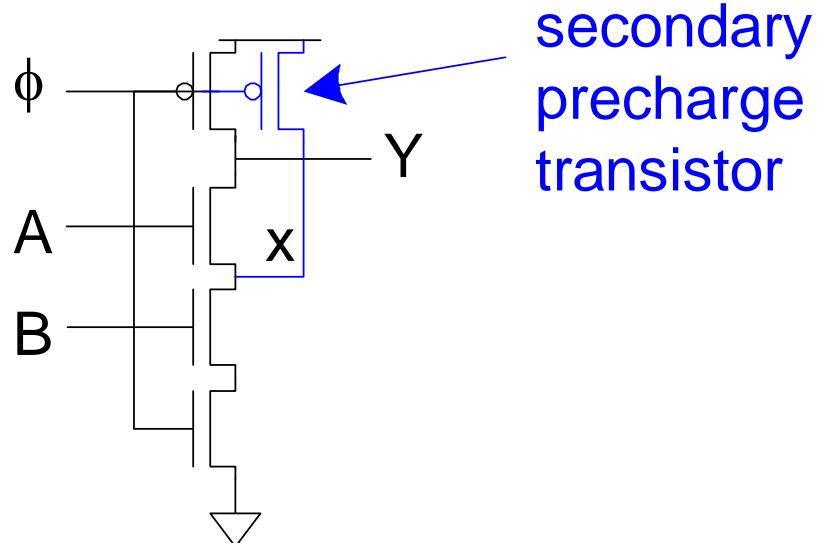
- Dynamic gates suffer from charge sharing



$$V_x = V_Y = \frac{C_Y}{C_x + C_Y} V_{DD}$$

Secondary Precharge

- Solution: add secondary precharge transistors
 - Typically need to precharge every other node
- Big load capacitance C_Y helps as well



Noise Sensitivity

- ❑ Dynamic gates are very sensitive to noise
 - Inputs: $V_{IH} \approx V_{tn}$
 - Outputs: floating output susceptible noise
- ❑ Noise sources
 - Capacitive crosstalk
 - Charge sharing
 - Power supply noise
 - Feedthrough noise
 - And more!

Power

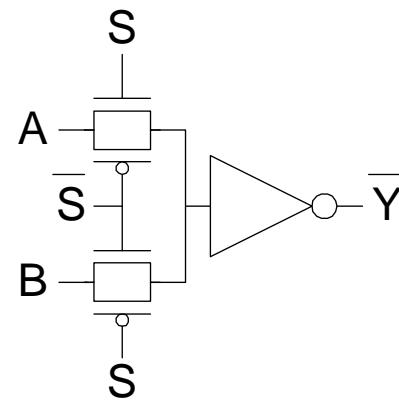
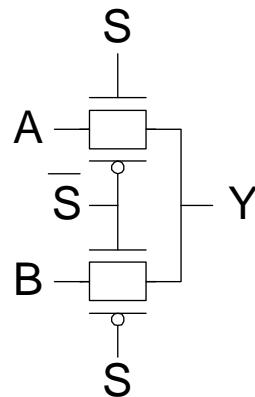
- ❑ Domino gates have high activity factors
 - Output evaluates and precharges
 - If output probability = 0.5, $\alpha = 0.5$
 - Output rises and falls on half the cycles
 - Clocked transistors have $\alpha = 1$
 - ❑ Leads to very high power consumption

Domino Summary

- ❑ Domino logic is attractive for high-speed circuits
 - 1.3 – 2x faster than static CMOS
 - But many challenges:
 - Monotonicity, leakage, charge sharing, noise
 - ❑ Widely used in high-performance microprocessors in 1990s when speed was king
 - ❑ Largely displaced by static CMOS now that power is the limiter
 - ❑ Still used in memories for area efficiency
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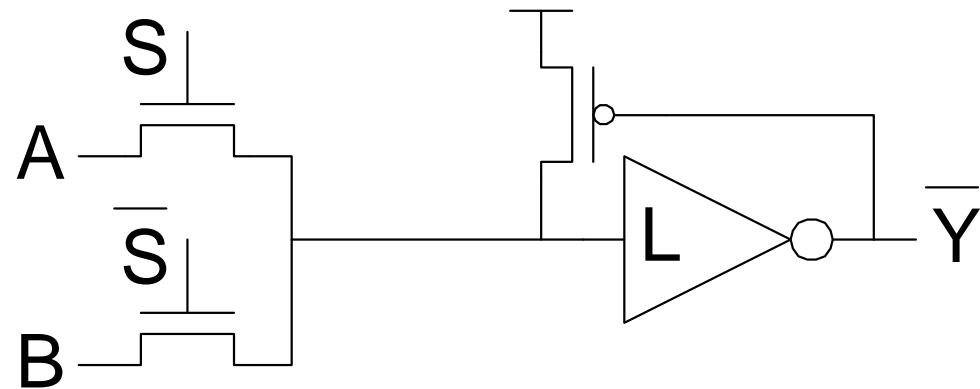
Pass Transistor Circuits

- Use pass transistors like switches to do logic
- Inputs drive diffusion terminals as well as gates
- CMOS + Transmission Gates:
 - 2-input multiplexer
 - Gates should be restoring



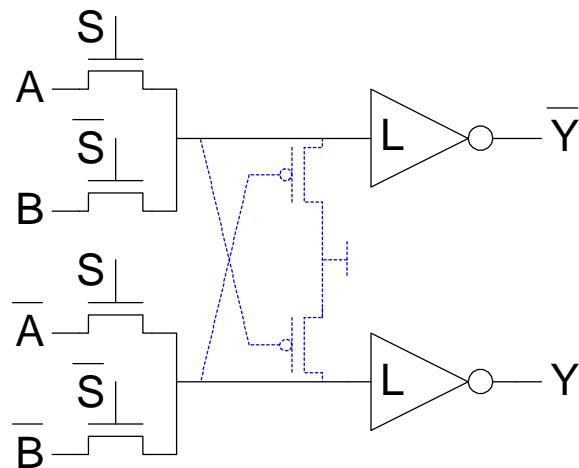
LEAP

- LEA_n integration with Pass transistors
- Get rid of pMOS transistors
 - Use weak pMOS feedback to pull fully high
 - Ratio constraint
 - $V_{OH} (=V_{DD}-V_t) \geq V_{IH} (\approx V_t) \Rightarrow V_{DD} \geq 2V_t$



CPL

- Complementary Pass-transistor Logic
 - Dual-rail form of pass transistor logic
 - Avoids need for ratioed feedback
 - Optional cross-coupling for rail-to-rail swing



Pass Transistor Summary

- ❑ Researchers investigated pass transistor logic for general purpose applications in the 1990's
 - Benefits over static CMOS were small or negative
 - No longer generally used
- ❑ However, pass transistors still have a niche in special circuits such as memories where they offer small size and the threshold drops can be managed

Homework Assignments

- Chapter 9:
 - 9.35
 - 9.38 (In part a, consider NAND-only implementation as well as complex gate. Also, in addition to comparing the number of transistors, calculate and compare the delays too)
 - 9.42
- For Tuesday 1402/10/19