

Combinational Circuit Design

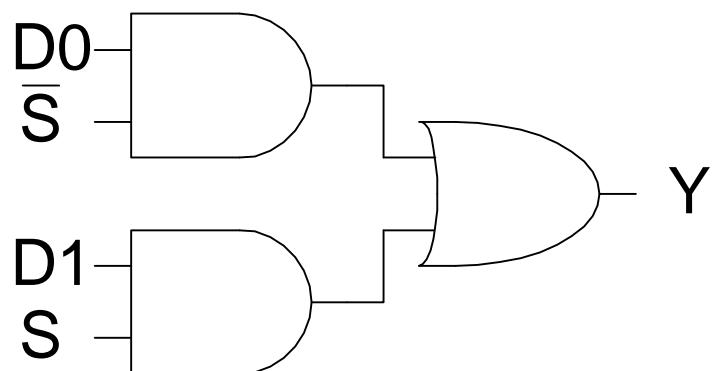
Outline

- Static CMOS Compound Gates
- Tradeoff Between Delay and Area
- Input Ordering
- Asymmetric Gates
- Skewed Gates
- Best P/N ratio

Example 1

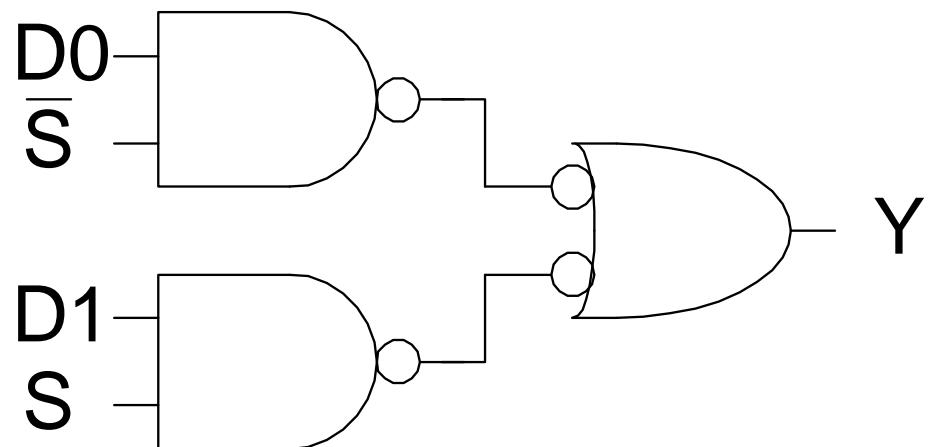
```
module mux(input  S, D0, D1,  
           output Y);  
  
    assign Y = S ? D1 : D0;  
endmodule
```

- 1) Sketch a design using AND, OR, and NOT gates.



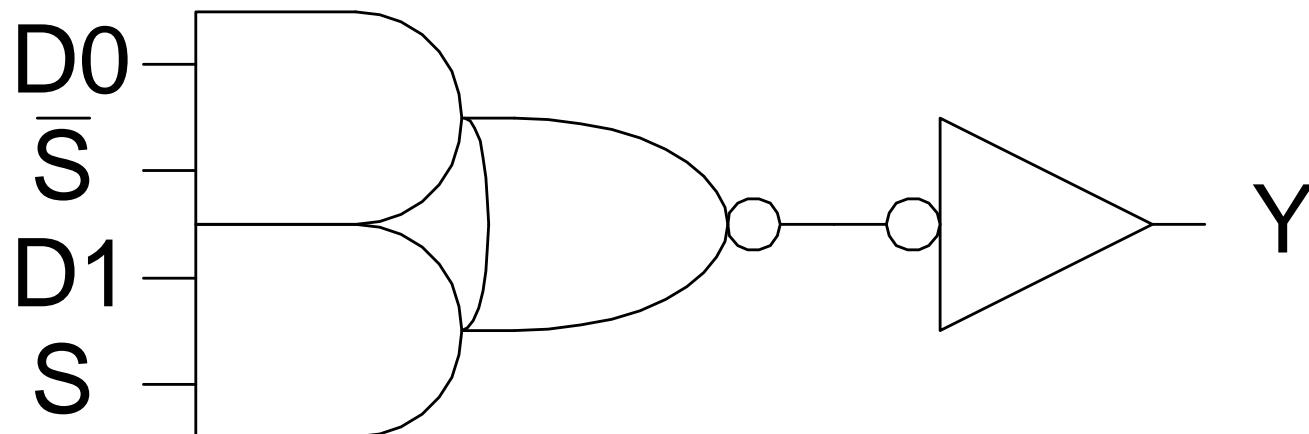
Example 2

- 2) Sketch a design using NAND, NOR, and NOT gates.
Assume $\sim S$ is available.



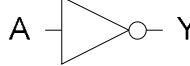
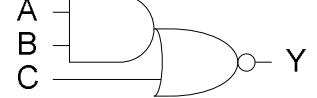
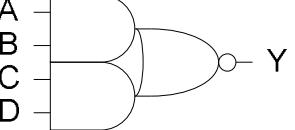
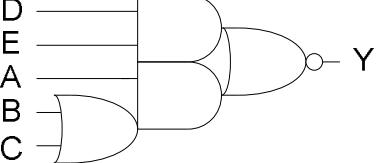
Example 3

- 3) Sketch a design using one compound gate and one NOT gate. Assume $\sim S$ is available.



Compound Gates

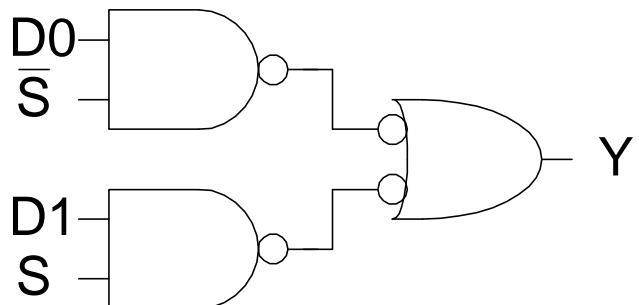
□ Logical Effort of compound gates

unit inverter	AOI21	AOI22	Complex AOI
$Y = \overline{A}$	$Y = \overline{A \square B + C}$	$Y = \overline{A \square B + C \square D}$	$Y = \overline{A \square (B + C) + D \square E}$
			
$g_A = 3/3$ $p = 3/3$	$g_A = 6/3$ $g_B = 6/3$ $g_C = 5/3$ $p = 7/3$	$g_A = 6/3$ $g_B = 6/3$ $g_C = 6/3$ $g_D = 6/3$ $p = 12/3$	$g_A = 5/3$ $g_B = 8/3$ $g_C = 8/3$ $g_D = 8/3$ $g_E = 8/3$ $p = 16/3$

Example 4

- The multiplexer has a maximum input capacitance of 16 units on each input. It must drive a load of 160 units. Estimate the delay of the two designs.

$$H = 160 / 16 = 10 \quad B = 1 \quad N = 2$$



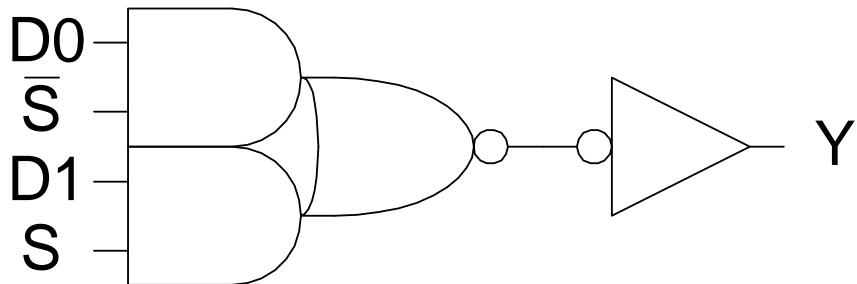
$$P = 2 + 2 = 4$$

$$G = (4/3) \square (4/3) = 16/9$$

$$F = GBH = 160/9$$

$$\hat{f} = \sqrt[N]{F} = 4.2$$

$$D = N\hat{f} + P = 12.4\tau$$



$$P = 4 + 1 = 5$$

$$G = (6/3) \square (1) = 2$$

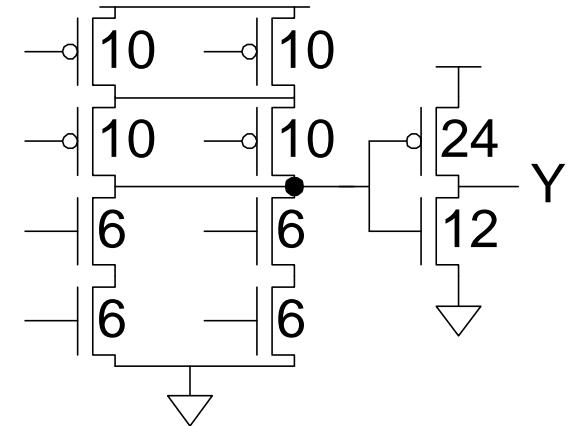
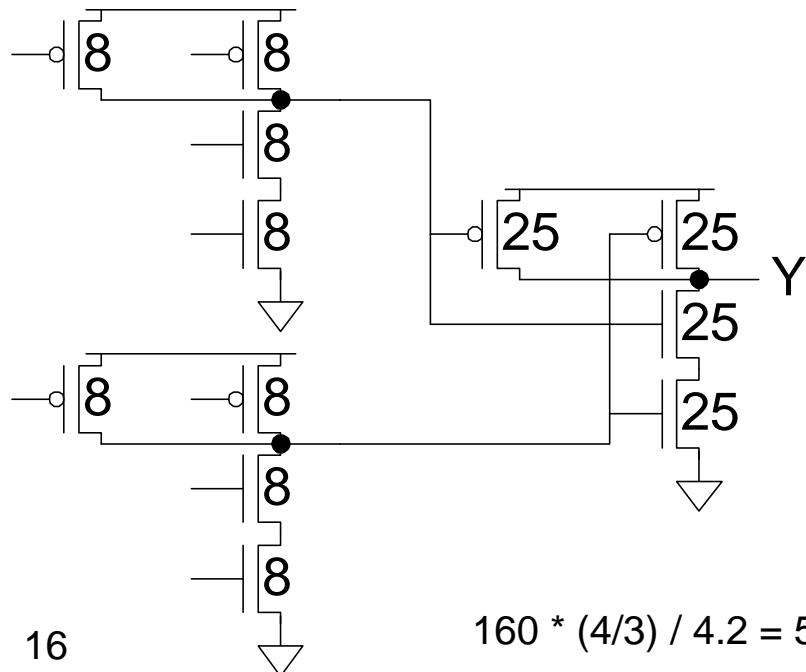
$$F = GBH = 20$$

$$\hat{f} = \sqrt[N]{F} = 4.5$$

$$D = N\hat{f} + P = 14\tau$$

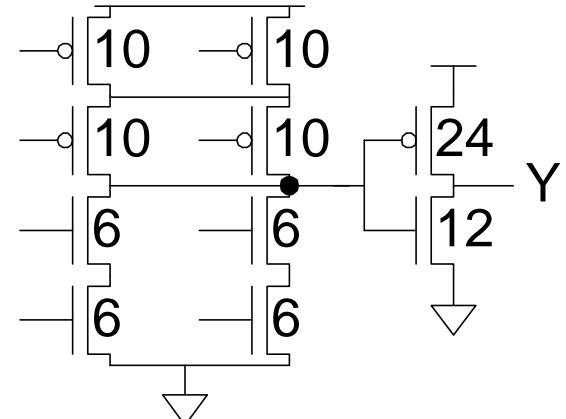
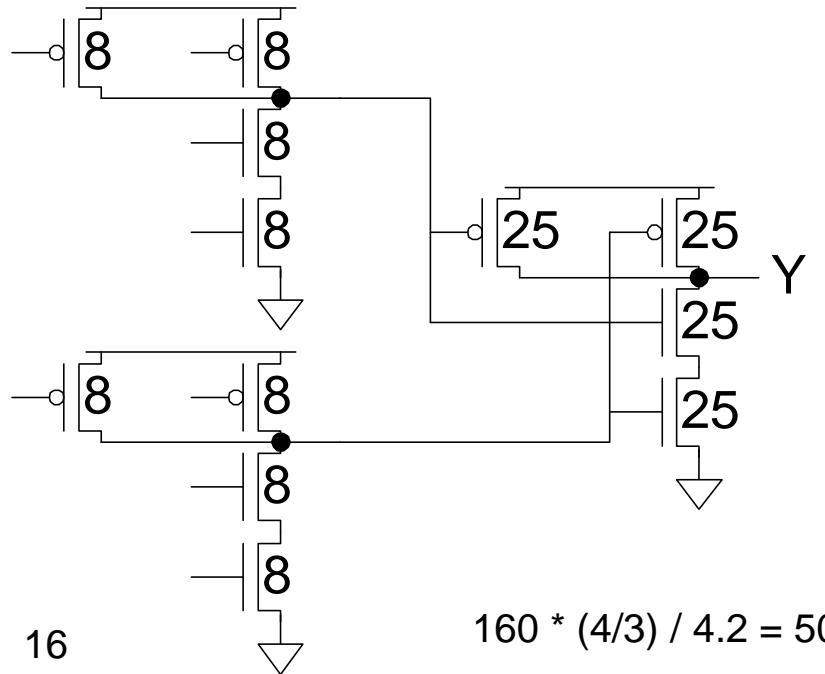
Example 5

- Annotate your designs with transistor sizes that achieve this delay.



Example 5 (Area)

- Let's calculate the total area:

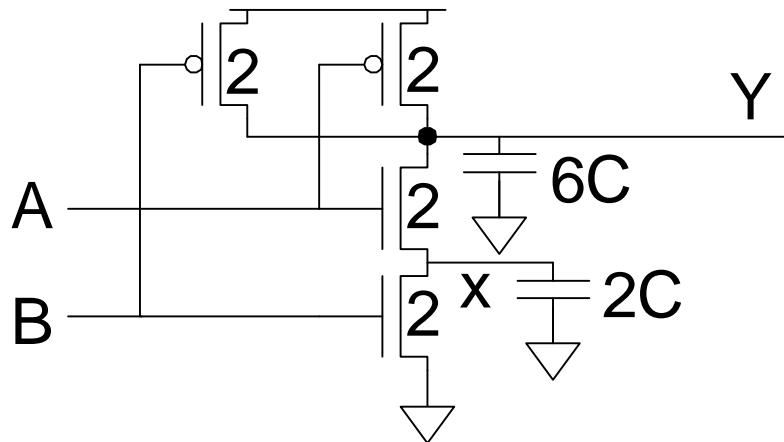


- $8 \times 8 + 4 \times 25 = 164$ $4 \times 6 + 4 \times 10 + 12 + 24 = 100$
- Conclusion: NAND-only 11.5% faster but 64% larger than AOI

Input Order

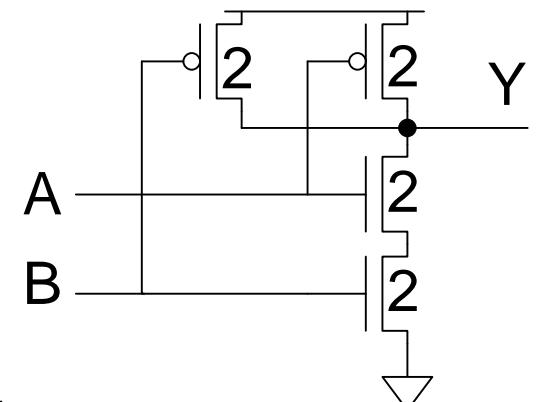
- ❑ Our parasitic delay model was too simple
 - Calculate parasitic delay for Y falling
 - If A arrives latest? 2τ
 - If B arrives latest? 2.33τ

NOTE: This is
based on Elmore
delay!



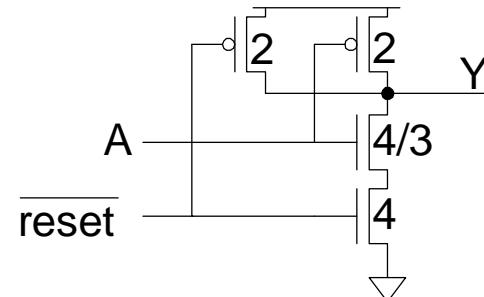
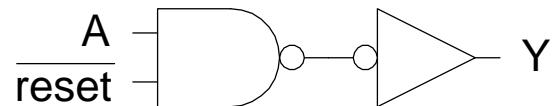
Inner & Outer Inputs

- ❑ *Inner* input is closest to output (A)
- ❑ *Outer* input is closest to rail (B)
- ❑ If input arrival time is known:
 - Connect latest input to inner input



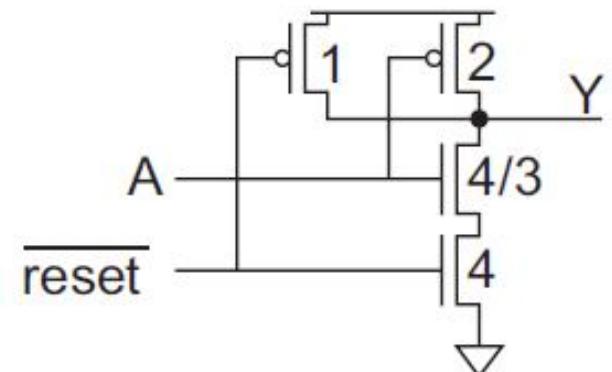
Asymmetric Gates

- ❑ Asymmetric gates favor one input over another
- ❑ Ex: suppose input A of a NAND gate is most critical
 - Use smaller transistor on A (less capacitance)
 - Boost size of noncritical input
 - So total resistance is same
- ❑ $g_A = 10/9$
- ❑ $g_{\text{reset}} = 2$
- ❑ $g_{\text{total}} = g_A + g_{\text{reset}} = 28/9$
- ❑ $g_{\text{average}} = g_{\text{total}}/2 = 14/9$
- ❑ Asymmetric gate approaches $g = 1$ on critical input



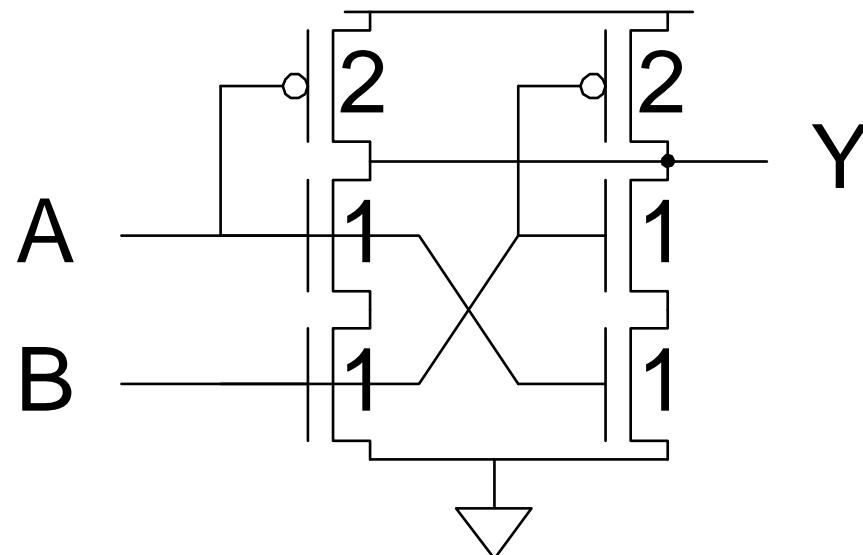
Asymmetric Gates (Cont'd)

- But total logical effort goes up (compare 14/9 with 4/3)
- To remedy:
 - Shrink the pMOS transistor on the reset input
 - Lowers logical effort
 - Reduces parasitic delay
 - Cost: slower response to reset



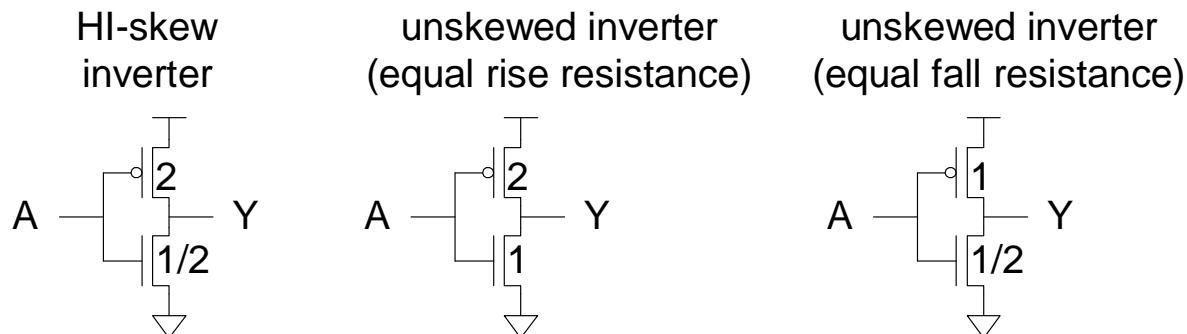
Symmetric Gates

- Inputs can be made perfectly symmetric
- Application example: arbiter circuit



Skewed Gates

- ❑ Skewed gates favor one edge over another
- ❑ Ex: suppose rising output of inverter is most critical
 - Downsize noncritical nMOS transistor



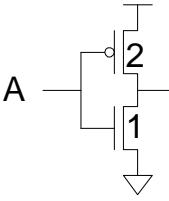
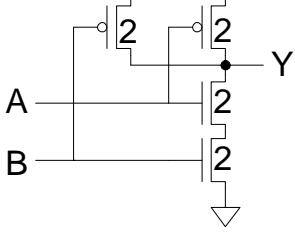
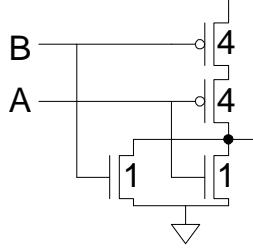
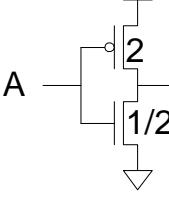
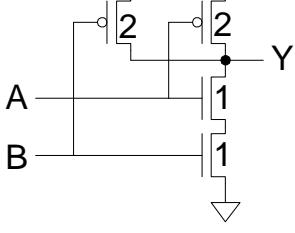
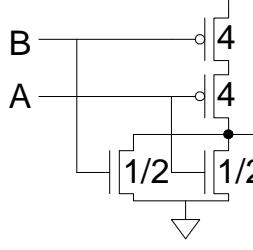
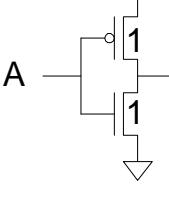
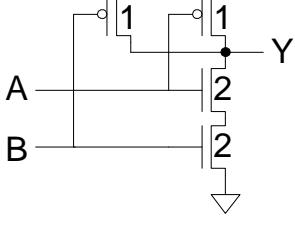
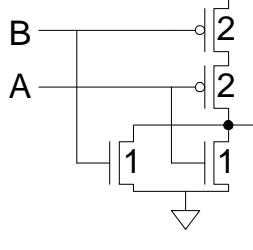
- ❑ Calculate logical effort by comparing to unskewed inverter with same effective resistance on that edge.
 - $g_u = 2.5 / 3 = 5/6 < 1$
 - $g_d = 2.5 / 1.5 = 5/3 > 1$

HI- and LO-Skew

- Def: Logical effort of a skewed gate for a particular transition is the ratio of the input capacitance of that gate to the input capacitance of an unskewed inverter delivering the same output current for the same transition.

 - Skewed gates reduce size of noncritical transistors
 - HI-skew gates favor rising output (small nMOS)
 - LO-skew gates favor falling output (small pMOS)
 - Logical effort is smaller for favored direction
 - But larger for the other direction
-

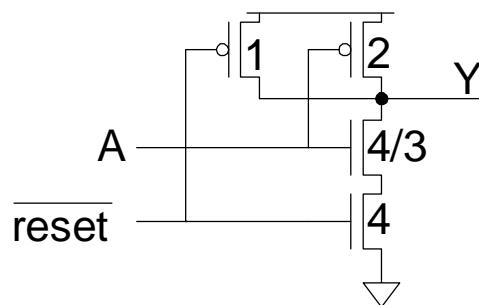
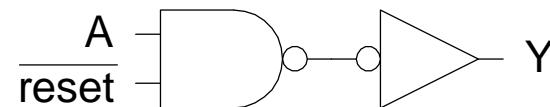
Catalog of Skewed Gates

	Inverter	NAND2	NOR2
unskewed	 <p>A — Y</p> <p>$g_u = 1$ $g_d = 1$ $g_{avg} = 1$</p>	 <p>A — Y</p> <p>$g_u = 4/3$ $g_d = 4/3$ $g_{avg} = 4/3$</p>	 <p>B — Y</p> <p>$g_u = 5/3$ $g_d = 5/3$ $g_{avg} = 5/3$</p>
Hi-skew	 <p>A — Y</p> <p>$g_u = 5/6$ $g_d = 5/3$ $g_{avg} = 5/4$</p>	 <p>A — Y</p> <p>$g_u = 1$ $g_d = 2$ $g_{avg} = 3/2$</p>	 <p>B — Y</p> <p>$g_u = 3/2$ $g_d = 3$ $g_{avg} = 9/4$</p>
LO-skew	 <p>A — Y</p> <p>$g_u = 4/3$ $g_d = 2/3$ $g_{avg} = 1$</p>	 <p>A — Y</p> <p>$g_u = 2$ $g_d = 1$ $g_{avg} = 3/2$</p>	 <p>B — Y</p> <p>$g_u = 2$ $g_d = 1$ $g_{avg} = 3/2$</p>

NOTE: LO-skew NOR2 is better than unskewed gate!

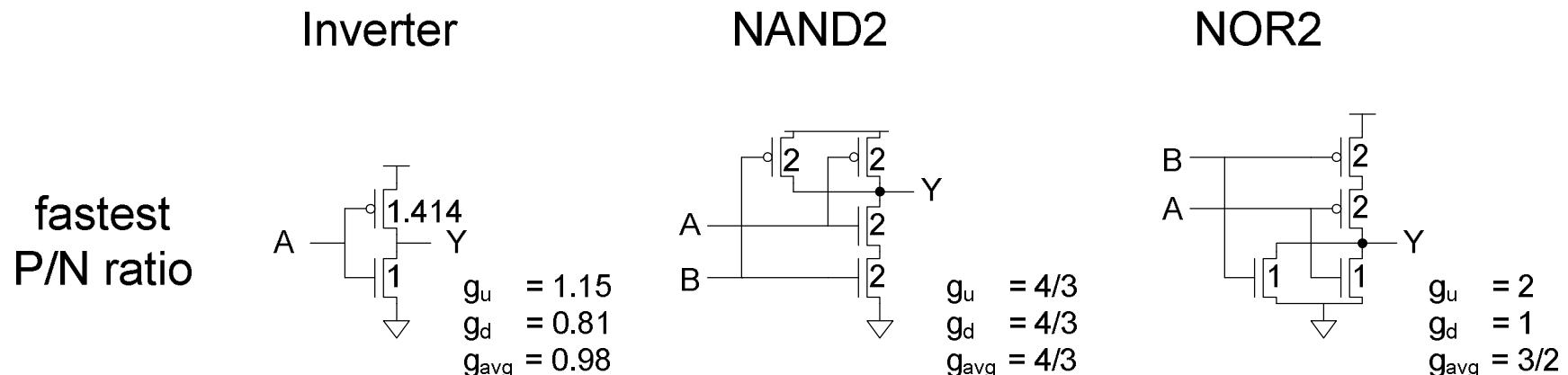
Asymmetric Skew

- Combine asymmetric and skewed gates
 - Downsize noncritical transistor on unimportant input
 - Reduces parasitic delay for critical input



P/N Ratios

- In general, best P/N ratio is sqrt of equal delay ratio.
 - Only improves average delay slightly for inverters
 - But significantly decreases area and power



Homework Assignments

- Chapter 9: 9.11, 9.13, and 9.14
- For Tuesday 1402/10/12