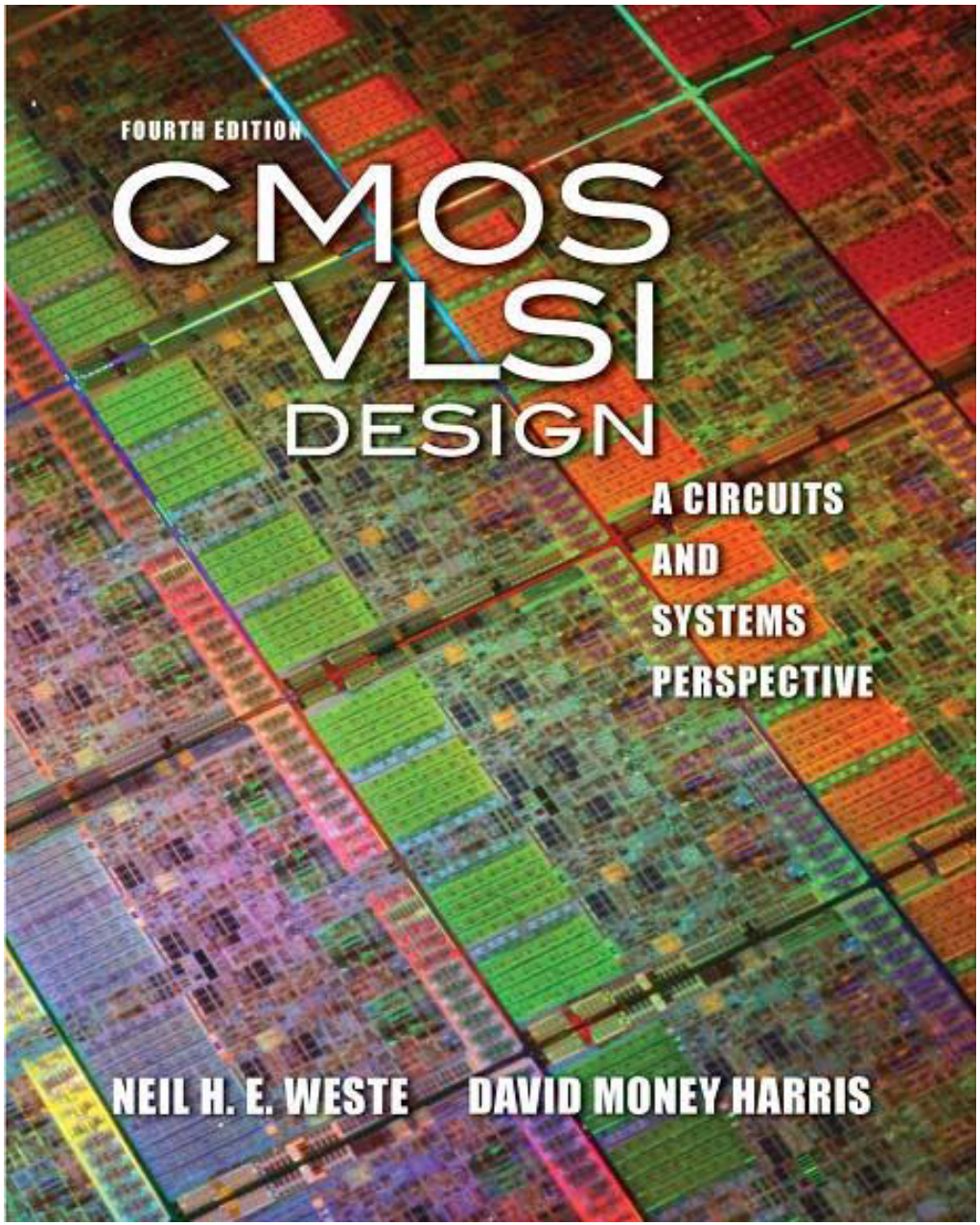



# CMOS Inverter DC Characteristics

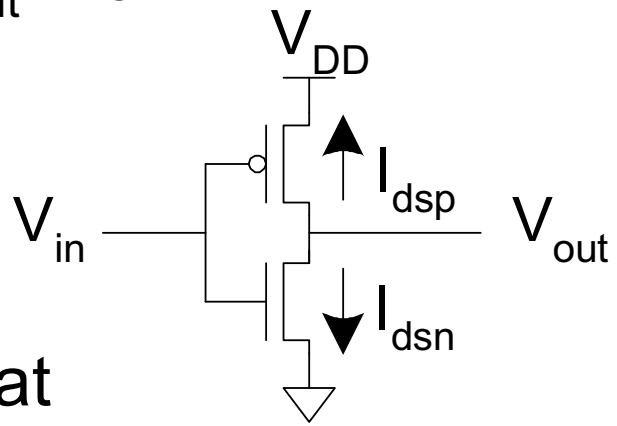
# Outline

- CMOS Inverter DC Response
- Logic Levels and Noise Margins
- Transient Response
- Pass Transistors

# DC Response

- DC Response: $V_{out}$ vs. $V_{in}$ for a gate
- Ex: Inverter
  - When $V_{in} = 0$ -> $V_{out} = V_{DD}$
  - When $V_{in} = V_{DD}$ -> $V_{out} = 0$
  - In between, $V_{out}$ depends on transistor size and current
  - Assuming no load current:
    - By KCL, must settle such that

$$I_{dsn} = |I_{dsp}|$$

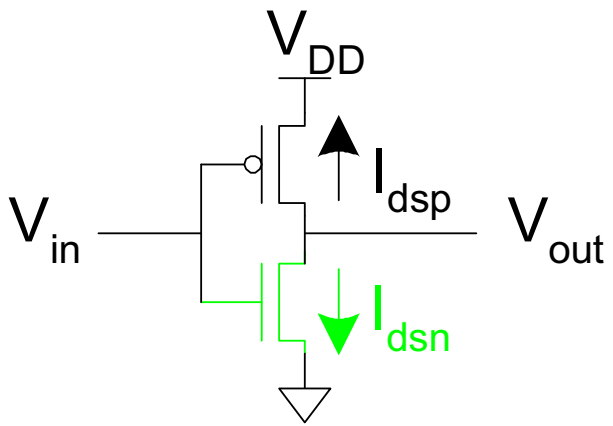


# Transistor Operation

- Current depends on region of transistor behavior
- For what $V_{in}$ and $V_{out}$ are nMOS and pMOS in
  - Cutoff?
  - Linear?
  - Saturation?

# nMOS Operation

| Cutoff | Linear | Saturated |
|---|---|---|
| $V_{gsn}$ < | $V_{gsn}$ > | $V_{gsn}$ > |
| | $V_{dsn}$ < | $V_{dsn}$ > |



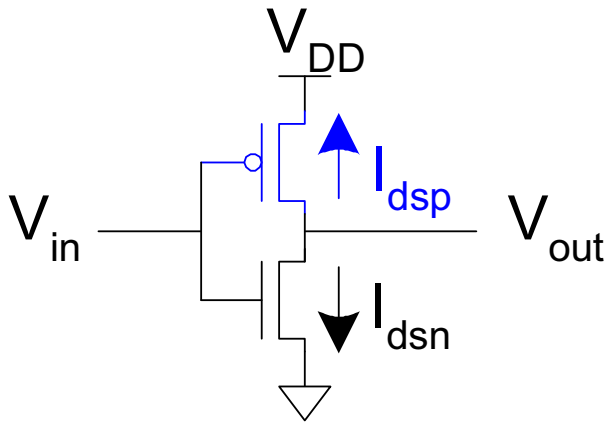
# pMOS Operation

| Cutoff | Linear | Saturated |
|---|---|---|
| $V_{gsp} > V_{tp}$<br>$V_{in} > V_{DD} + V_{tp}$ | $V_{gsp} < V_{tp}$<br>$V_{in} < V_{DD} + V_{tp}$<br>$V_{dsp} > V_{gsp} - V_{tp}$<br>$V_{out} > V_{in} - V_{tp}$ | $V_{gsp} < V_{tp}$<br>$V_{in} < V_{DD} + V_{tp}$<br>$V_{dsp} < V_{gsp} - V_{tp}$<br>$V_{out} < V_{in} - V_{tp}$ |

$V_{gsp} = V_{in} - V_{DD}$

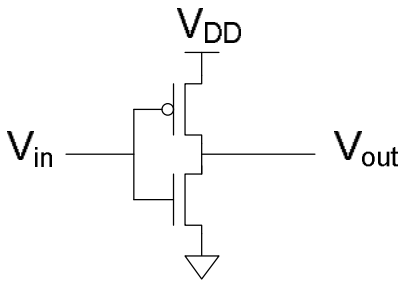
$V_{dsp} = V_{out} - V_{DD}$

$V_{tp} < 0$

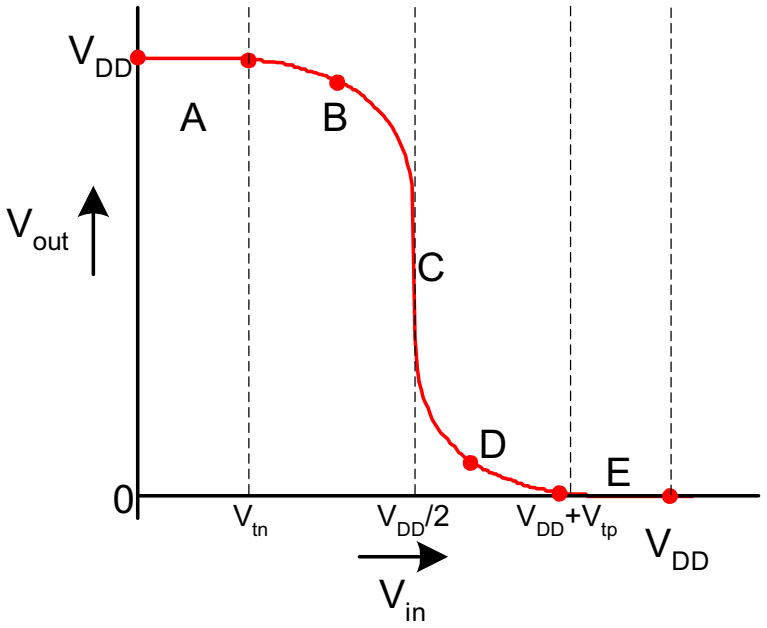


# Voltage Transfer Characteristics

- Five operating regions for two transistors

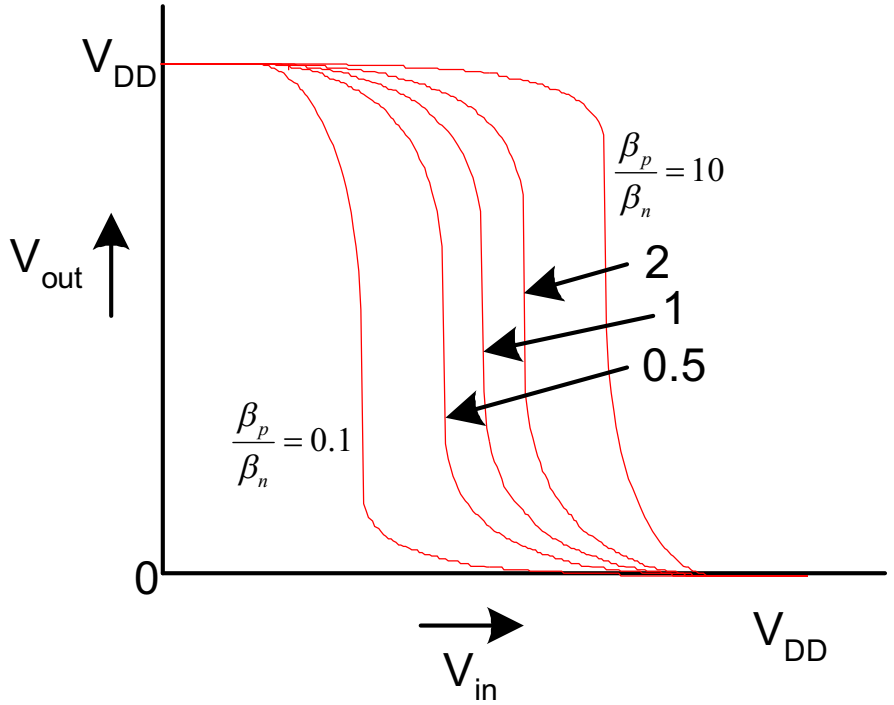



| Region | nMOS | pMOS |
|---|---|---|
| A | | |
| B | | |
| C | | |
| D | | |
| E | | |



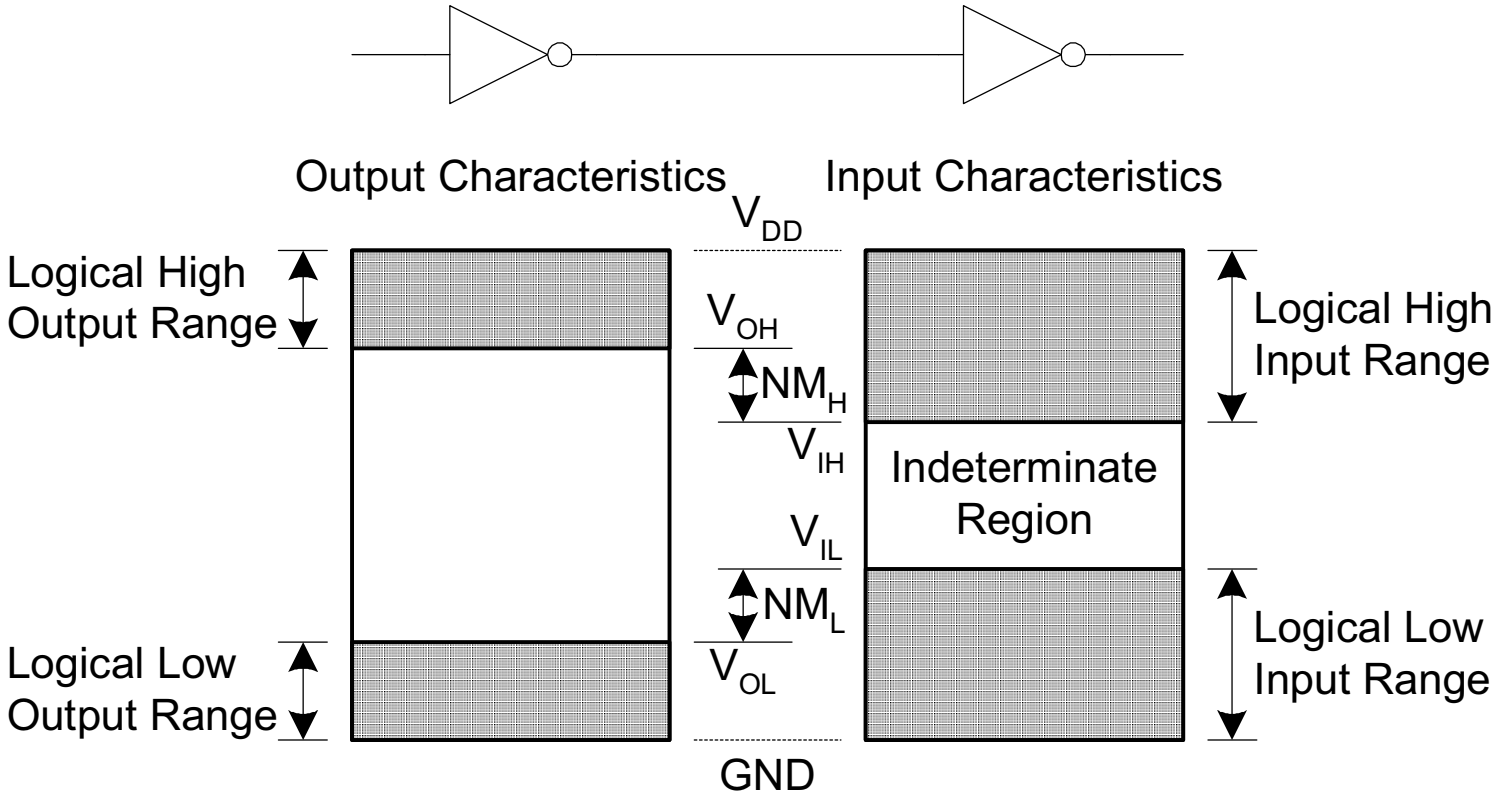
# Beta Ratio

- If $\beta_p / \beta_n \neq 1$, switching point will move from $V_{DD}/2$
- Called *skewed* gate
- Other gates: collapse into equivalent inverter



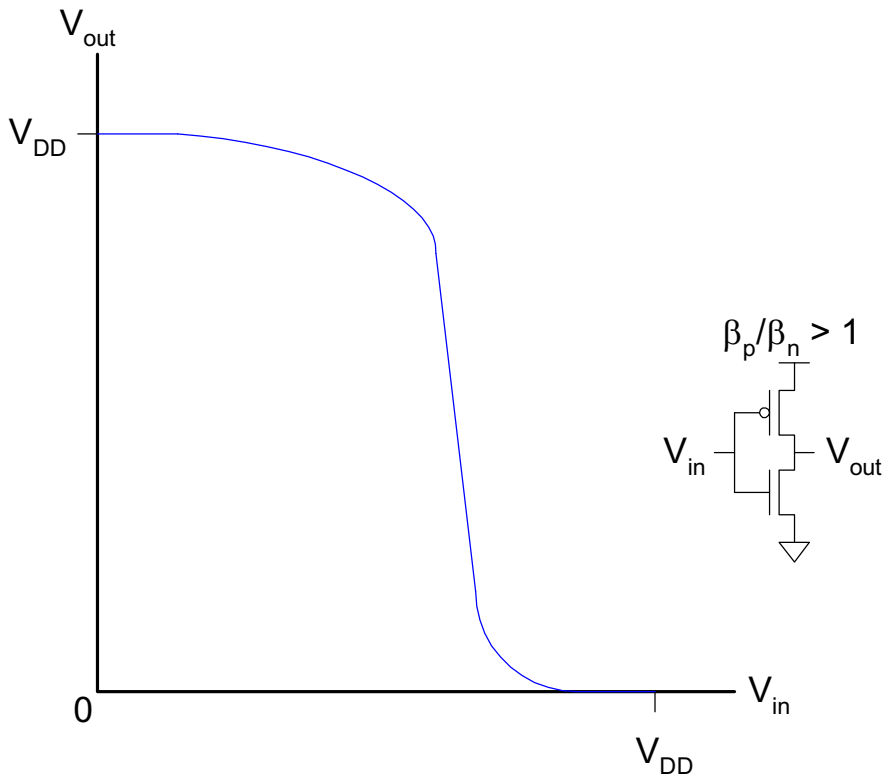
# Noise Margins

- How much noise can a gate input see before it does not recognize the input?



# Logic Levels

- Define critical voltages at:
  - unity gain point of DC transfer characteristic

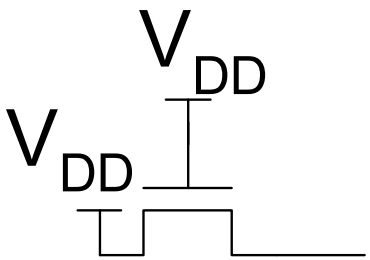


# Transient Response

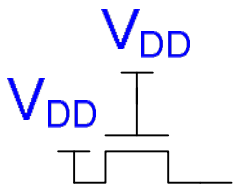
- *DC analysis* tells us $V_{out}$ if $V_{in}$ is constant
- *Transient analysis* tells us $V_{out}(t)$ if $V_{in}(t)$ changes
  - Requires solving differential equations
- Input is usually considered to be a step or ramp
  - From 0 to $V_{DD}$ or vice versa

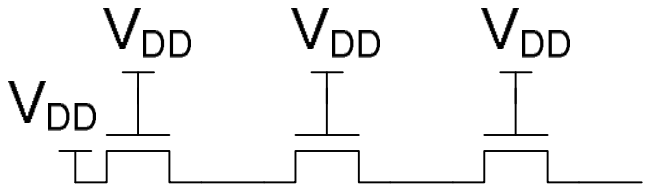
# Pass Transistors

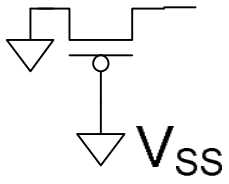
- We have assumed source is grounded
- What if source > 0?
  - e.g. pass transistor passing $V_{DD}$
- $V_g = V_{DD}$
  - If $V_s > V_{DD}-V_t$, $V_{gs} < V_t$
  - Hence transistor would turn itself off
- nMOS pass transistors pull no higher than $V_{DD}-V_{tn}$
  - Called a degraded "1"
  - Approach degraded value slowly (low $I_{ds}$)
- pMOS pass transistors pull no lower than $V_{tp}$
- Transmission gates are needed to pass both 0 and 1

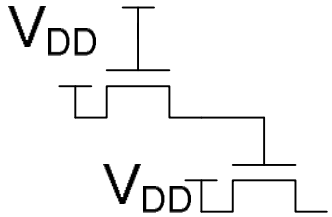


# Pass Transistor Ckts



# Homeworks

- Chapter 2 exercises: 2.16, 2.17, 2.20
- Due date: 1402/8/30