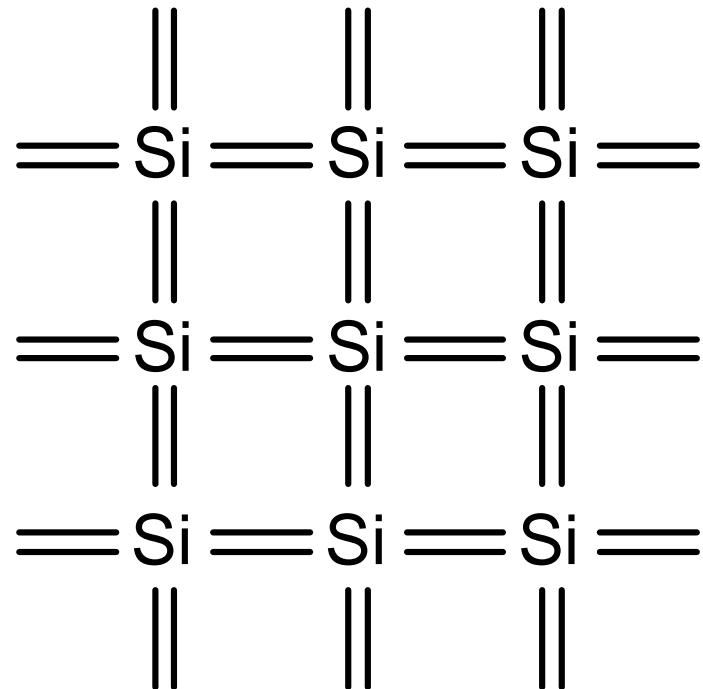


# MOSFET Transistors

# Silicon Lattice

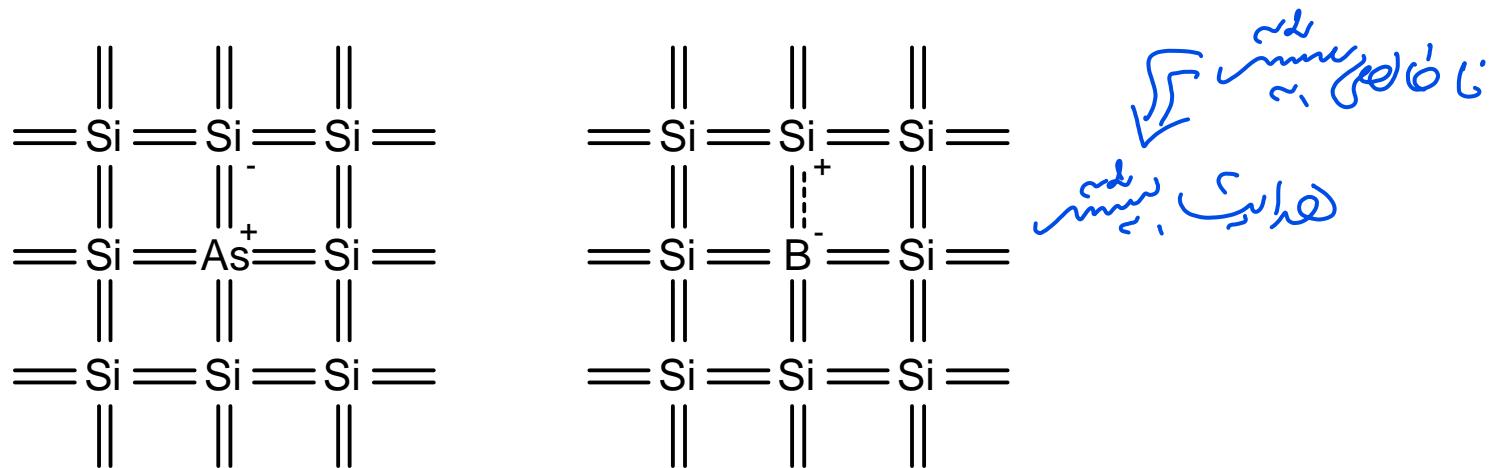
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- Transistors are built on a silicon substrate
- Silicon is a Group IV material
- Forms crystal lattice with bonds to four neighbors



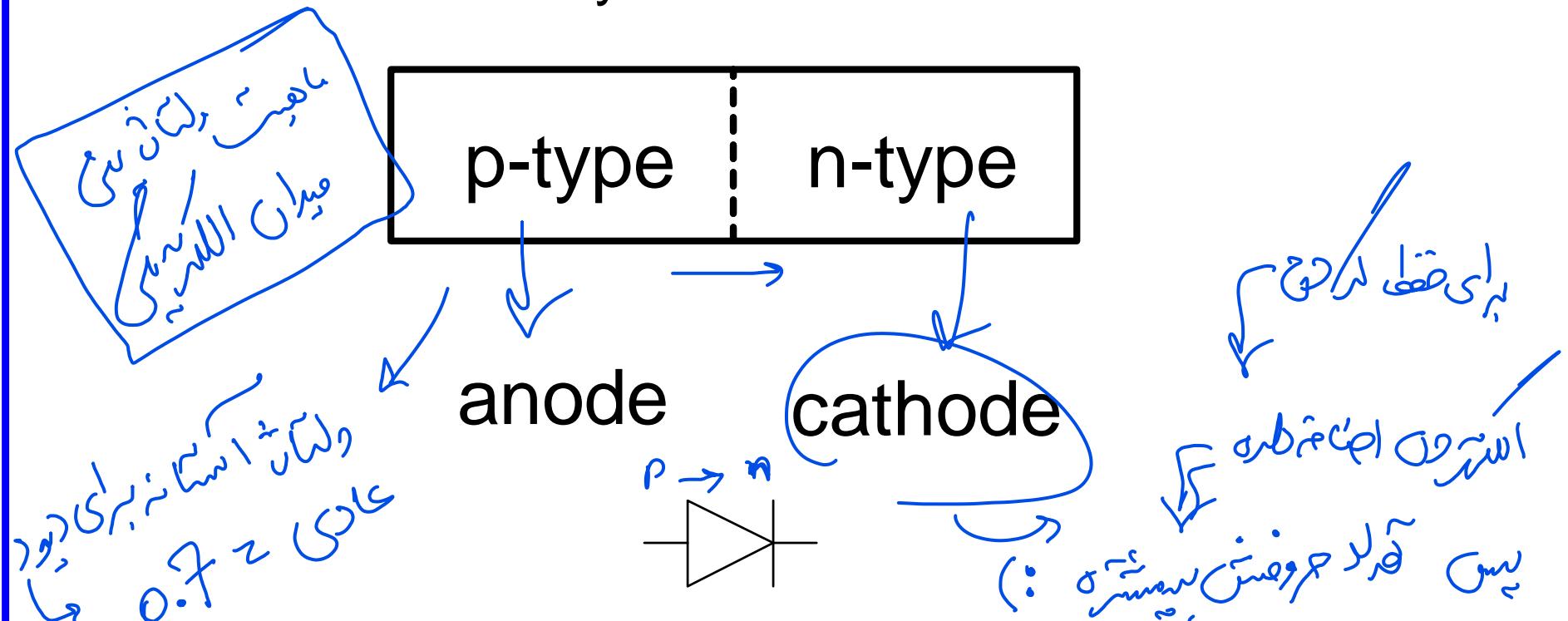
# Dopants

- Silicon is a semiconductor
- Pure silicon has no free carriers and conducts poorly
- Adding dopants increases the conductivity
- Group V: extra electron (n-type)
- Group III: missing electron, called hole (p-type)



# p-n Junctions

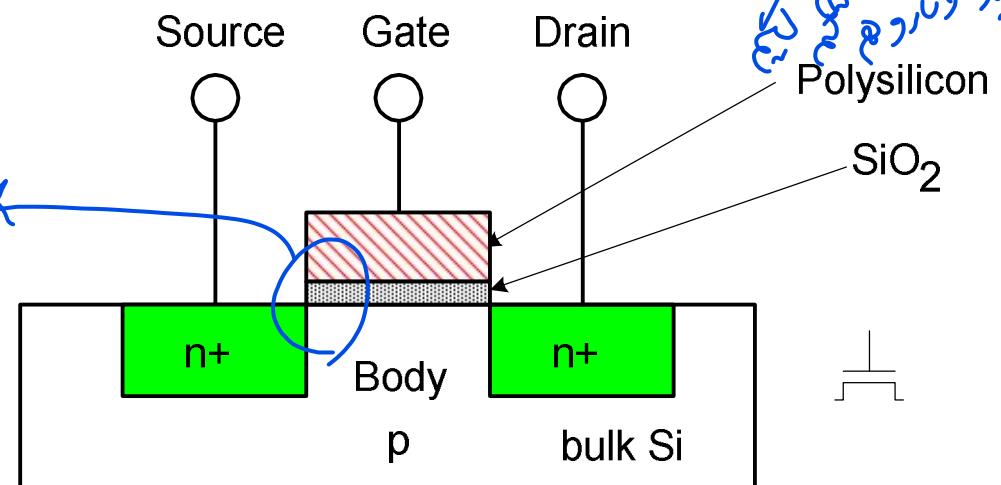
- A junction between p-type and n-type semiconductor forms a diode.
- Current flows only in one direction



$$Q = CV \quad \left\{ \quad I = C \frac{dV}{dt} \rightarrow \text{current} \right.$$

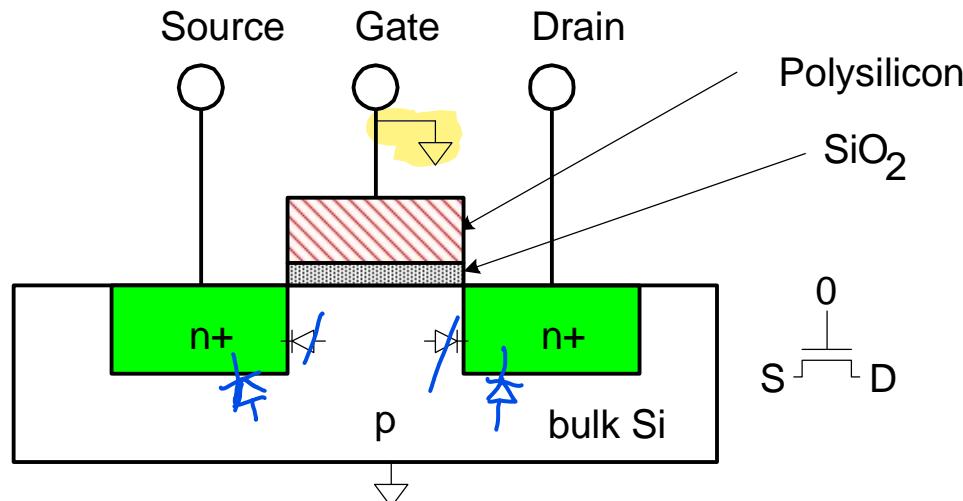
# nMOS Transistor

- Four terminals: gate, source, drain, body
- Gate – oxide – body stack looks like a capacitor
  - Gate and body are conductors
  - $\text{SiO}_2$  (oxide) is a very good insulator
  - Called metal – oxide – semiconductor (MOS) capacitor



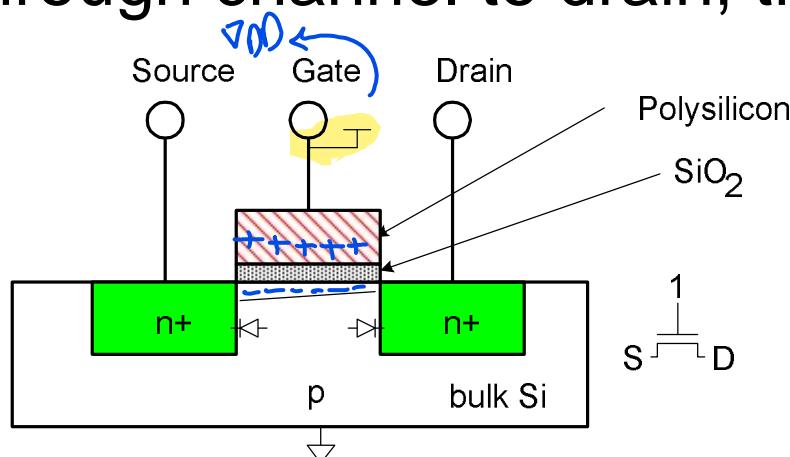
# nMOS Operation

- Body is usually tied to ground (0 V)
- When the gate is at a low voltage:
  - P-type body is at low voltage
  - Source-body and drain-body diodes are OFF
  - No current flows, transistor is OFF



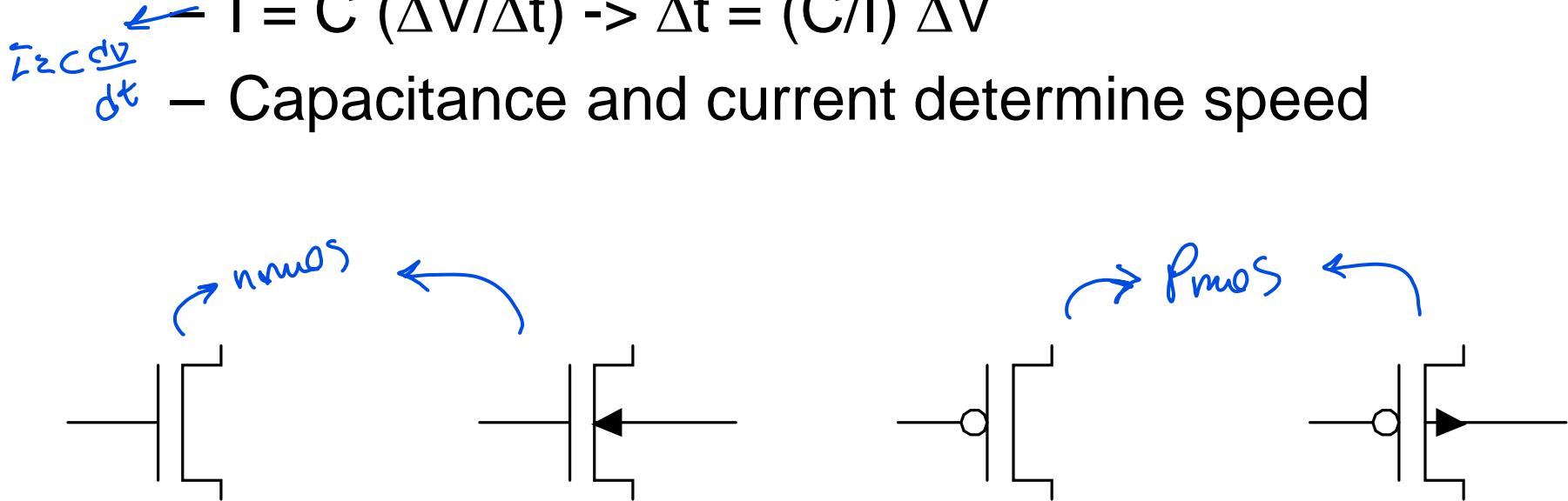
# nMOS Operation Cont.

- When the gate is at a high voltage:
  - Positive charge on gate of MOS capacitor
  - Negative charge attracted towards gate
  - Inverts a channel under gate to n-type
  - Now current can flow through n-type silicon from source through channel to drain, transistor is ON



# Large Picture

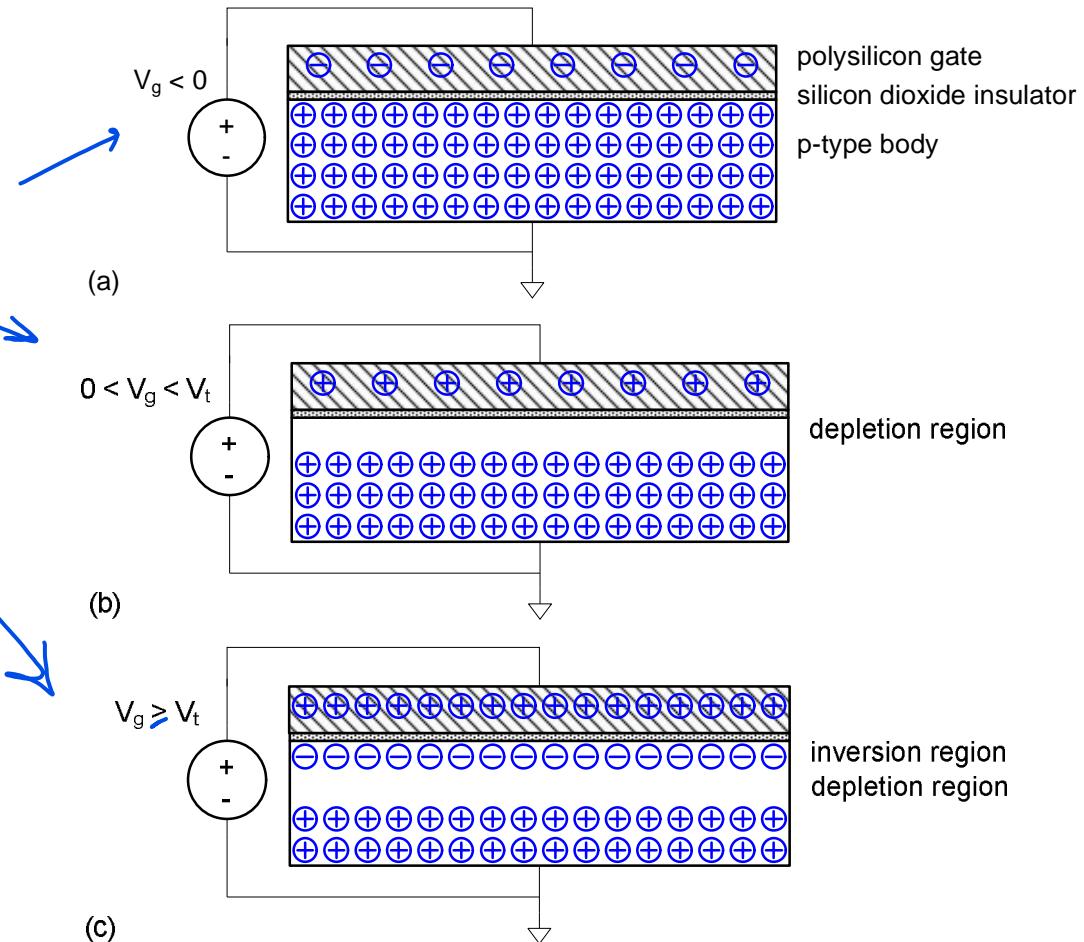
- An ON transistor passes a finite amount of current
  - Depends on terminal voltages
  - Derive current-voltage (I-V) relationships
- Transistor gate, source, drain all have capacitance
  - $I = C (\Delta V / \Delta t) \rightarrow \Delta t = (C/I) \Delta V$
  - Capacitance and current determine speed



# MOS Capacitor

- Gate and body form MOS capacitor

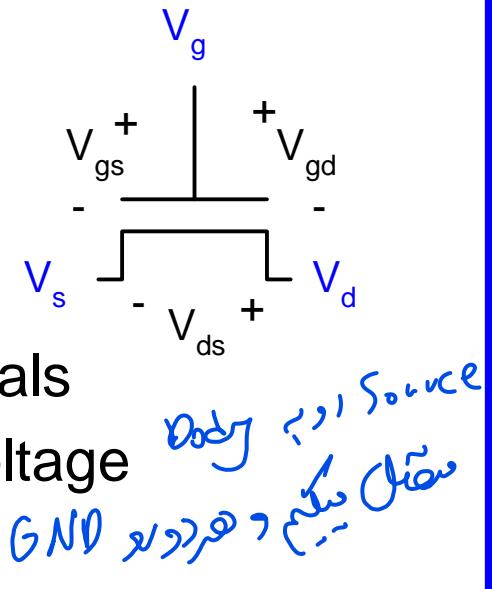
- Operating modes
  - Accumulation
  - Depletion
  - Inversion



# Terminal Voltages

- Mode of operation depends on  $V_g$ ,  $V_d$ ,  $V_s$

- $V_{gs} = V_g - V_s$
- $V_{gd} = V_g - V_d$
- $V_{ds} = V_d - V_s = V_{gs} - V_{gd}$



- Source and drain are symmetric diffusion terminals

- By convention, source is terminal at lower voltage
- Hence  $V_{ds} \geq 0$

- nMOS body is grounded. First assume source is 0 too.

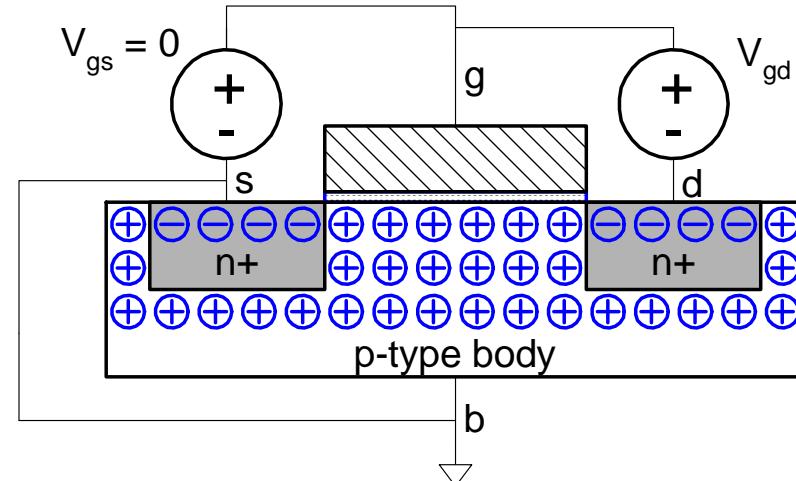
- Three regions of operation

- Cutoff*
- Linear*
- Saturation*

# nMOS Cutoff

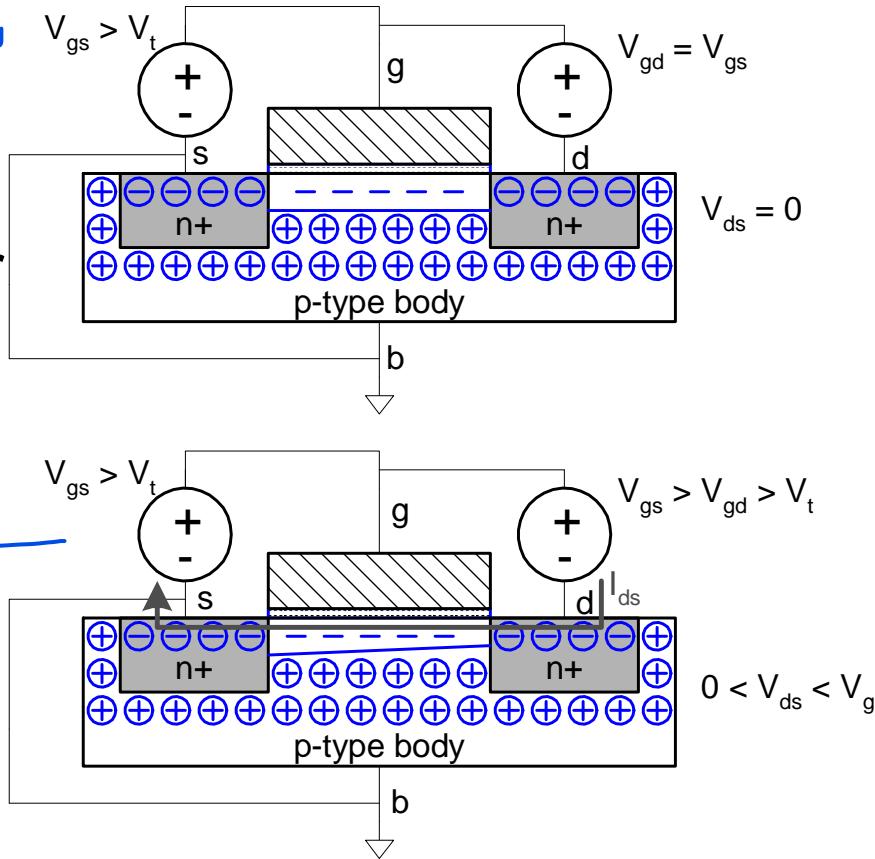
- ❑ No channel
- ❑  $I_{ds} \approx 0$

مکانیزم قطع (Cut-off mechanism)



# nMOS Linear

- Channel forms
- Current flows from d to s
  - $e^-$  from s to d بسیسری
- $I_{ds}$  increases with  $V_{ds}$
- Similar to linear resistor



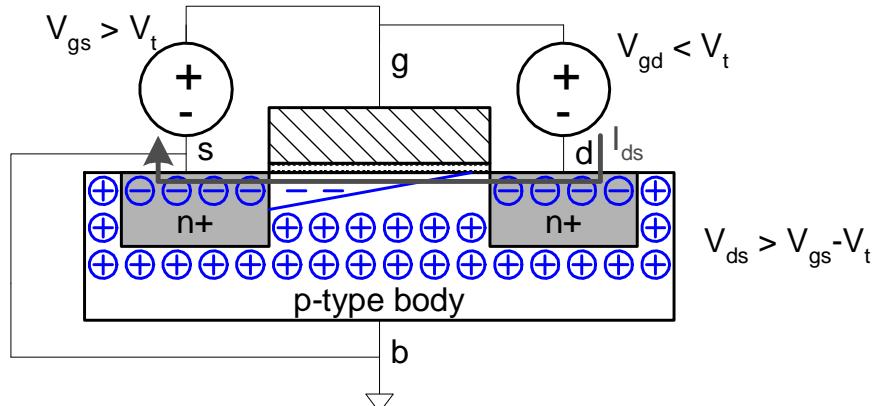
بری میں عواید مادہ میں ایسے  
امم ہستے ہیں جنکے پس میں فنیوں  
وکی بکی میں افکر کا ہے اس از کے خاصی  
ہستے کا ریاضی پس میں ضعیف ترہ نہیں  
وکی اس کا دو زیاد تر راستہ ترکیب میں کہ فوکی اس کی  
وکی

# nMOS Saturation

- Channel pinches off
- $I_{ds}$  independent of  $V_{ds}$
- We say current *saturates*
- Similar to current source

مُرْجِعَةٌ لِلْمُنْتَهِيَّاتِ  
أَنْتَ بَلْ تَسْرِي

لِلْمُنْتَهِيَّاتِ  
أَنْتَ بَلْ تَسْرِي



# I-V Characteristics

---

- ❑ In Linear region,  $I_{ds}$  depends on
  - How much charge is in the channel?
  - How fast is the charge moving?

$$I = \frac{Q}{t}$$

اگر میزان بورڈ میٹنگ میں رہنمایی کی مکملیت کا دلیل ہے تو اسے دوسرے میں میریم

# Channel Charge

18  

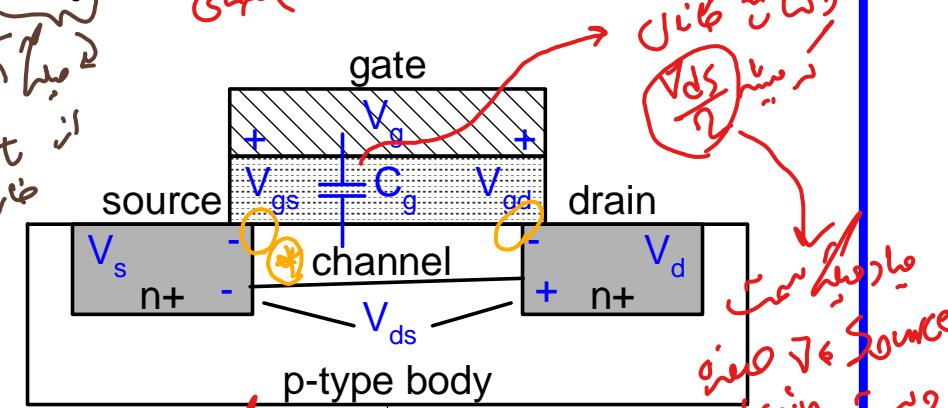
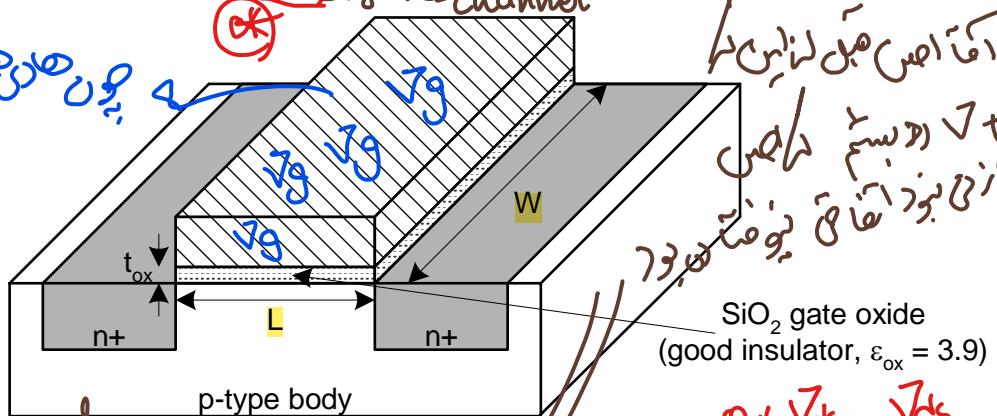
- MOS structure looks like parallel plate capacitor while operating in inversions
    - Gate – oxide – channel

$$\square \quad Q_{\text{channel}} = CV \xrightarrow{\substack{\text{Voltage} \\ \text{thickness}}}$$

◻  $C = C_g = \epsilon_{ox} WL / t_{ox} = \underline{C_{ox} WL}$  *law*

◻  $V = V_{gs} - V_t = (V_{gs} - V_{ds}/2) - V_t$

$$C_{ox} = \epsilon_{ox} / t_{ox}$$



برگایابه زمان

# Carrier velocity

برگایابه زمان

برگایابه زمان



- Charge is carried by e-
- Electrons are propelled by the lateral electric field between source and drain

$$\hookrightarrow E = V_{ds}/L \quad \leftarrow E = \frac{V}{d}$$

- Carrier velocity  $v$  proportional to lateral E-field

$$\hookrightarrow v = \mu E$$

$\mu$  called mobility

- Time for carrier to cross channel:

$$\hookrightarrow t = L / v$$

$$\hookrightarrow t = \frac{L}{v} = \frac{L}{\mu E} \Rightarrow t = \frac{L}{\mu} \frac{1}{E}$$

carrier

برگایابه زمان

# nMOS Linear I-V

- Now we know
    - How much charge  $Q_{\text{channel}}$  is in the channel
    - How much time  $t$  each carrier takes to cross

$$I_{ds} = \frac{Q_{\text{channel}}}{t}$$

بات دارای اسلامهای مول بفرمول عالی پیش میر

همچنین مقطع شیر و شیوه ساده تر میتواند

پس از هر دو بیشتری برای این

نامی میشود

را بخوبی میتوان

آنکه کسر مم

اگر این ایجاد شود

نامی میشود

عدهی (بیرون فارم)

که

$$= \mu C_{\text{ox}} \frac{W}{L} \left( V_{gs} - V_t - \frac{V_{ds}}{2} \right) V_{ds}$$

$$= \beta \left( V_{gs} - V_t - \frac{V_{ds}}{2} \right) V_{ds}$$

نامی میشود

که

$$\beta = \mu C_{\text{ox}} \frac{W}{L}$$

# nMOS Saturation I-V

- If  $V_{gd} < V_t$ , channel pinches off near drain
    - When  $V_{ds} > V_{dsat} = V_{qs} - V_t$

- Now drain voltage no longer increases current

$$I_{ds} = \beta \left( V_{gs} - V_t - \frac{V_{dsat}}{2} \right) V_{dsat}$$

برای این رابطه دو مسیر پیش داده شده اند:

مسیر اول:  $I_{ds} = \beta \left( V_{gs} - V_t - \frac{V_{dsat}}{2} \right) V_{dsat}$

مسیر دوم:  $I_{ds} = \frac{\beta}{2} \left( V_{gs} - V_t \right)^2$

$$V_{ds} = V_{gs} - V_{gd} \quad \text{--- (1)}$$

$$V_{gd} = V_{gs} - V_{ds} \quad \text{--- (2)}$$

$$\underbrace{V_{gs} - V_{ds}}_{V_{gd}} < V_t \Rightarrow V_{ds} > \underbrace{V_{gs} - V_t}_{V_{dsat}}$$

مقدار  $V_{ds}$  کمتر نباشد

long channel

# nMOS I-V Summary

## Shockley 1<sup>st</sup> order transistor models

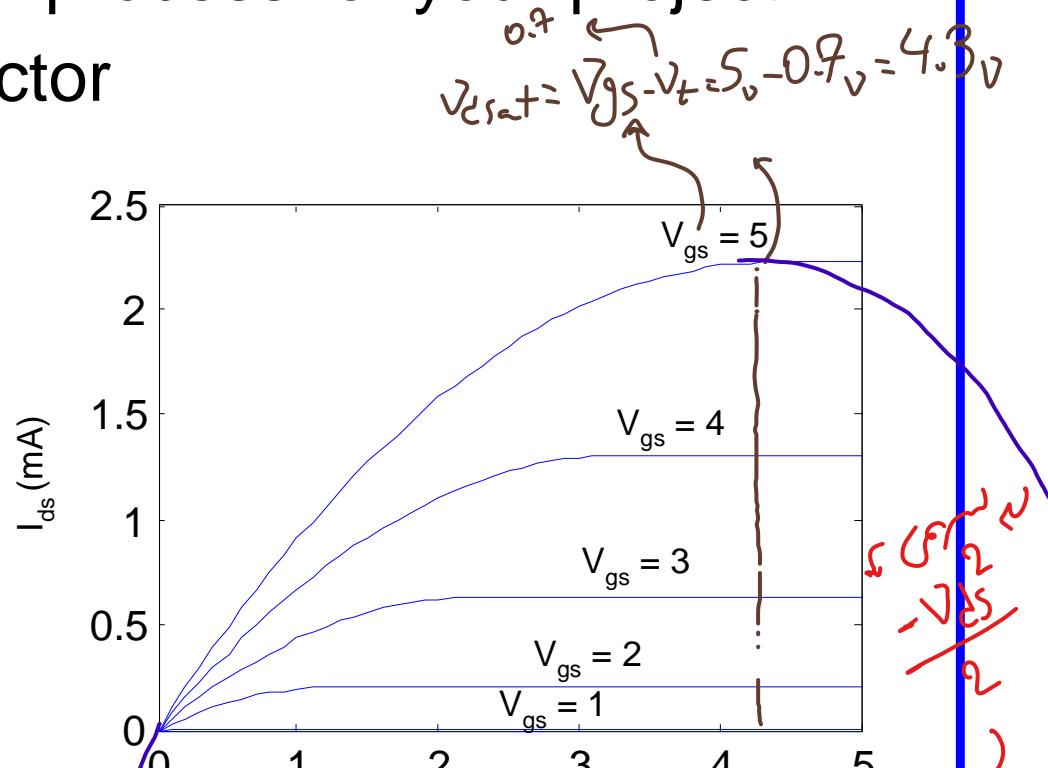
ماقی اسلام ۱۲ لعیم لر چون نامه‌ی بین دو طبقه ایل (DOD) پس می‌یابد  
قوی ای تولید می‌شود و این اتفاق زیاد و تا ۷۰٪ ای از ریکت نیزه دارد با پیشرفت تکنولوژی دیجیت نامه‌ی تولید ریکت  
کاهش خفت و خلی پیشرفت دلیل دیگر ای این اتفاق هم به اندانه کمتر می‌کنست پس این نوابط ساده‌تری (بیکار اوی) صادر شد  
از ماز

$$I_{ds} = \begin{cases} 0 & V_{gs} < V_t \quad \text{cutoff} \\ \beta \left( V_{gs} - V_t - \frac{V_{ds}}{2} \right) V_{ds} & V_{ds} < V_{dsat} \quad \text{linear} \\ \frac{\beta}{2} (V_{gs} - V_t)^2 & V_{ds} > V_{dsat} \quad \text{saturation} \end{cases}$$

# Example

- We will be using a  $0.6 \mu\text{m}$  process for your project
  - From AMI Semiconductor
  - $t_{\text{ox}} = 100 \text{ \AA}$
  - $\mu = 350 \text{ cm}^2/\text{V}\cdot\text{s}$
  - $V_t = 0.7 \text{ V}$
- Plot  $I_{\text{ds}}$  vs.  $V_{\text{ds}}$ 
  - $V_{\text{gs}} = 0, 1, 2, 3, 4, 5$
  - Use  $W/L = 4/2 \lambda$

$$\beta = \mu C_{\text{ox}} \frac{W}{L} = (350) \left( \frac{3.9 \times 8.85 \cdot 10^{-14}}{100 \cdot 10^{-8}} \right) \left( \frac{W}{L} \right) = 120 \frac{W}{L} \mu\text{A/V}^2$$

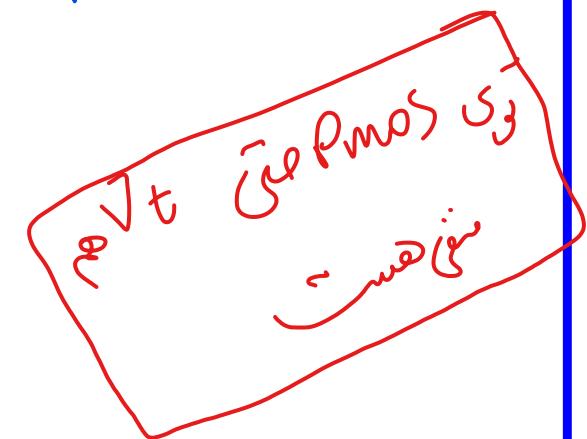
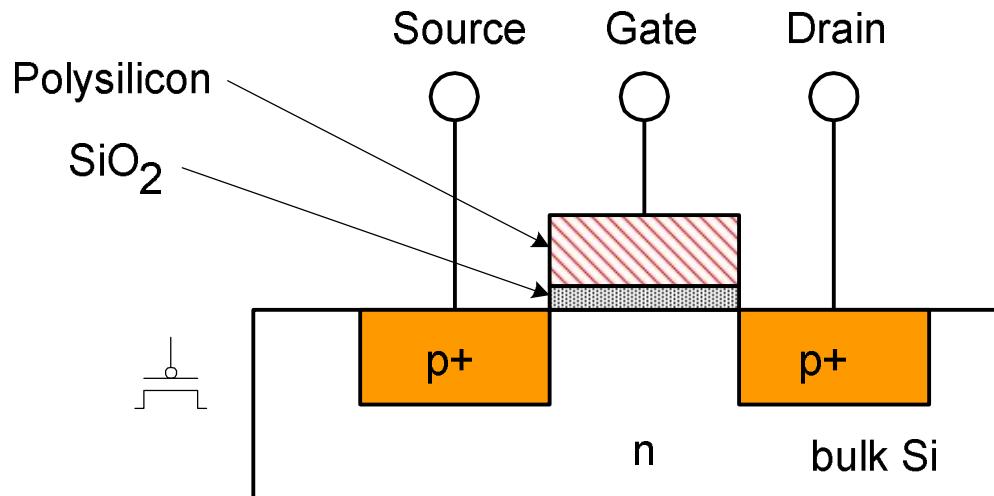


nMOS Gate, Schematic

# pMOS Transistor

- Similar, but doping and voltages reversed

- Body tied to high voltage ( $V_{DD}$ ) → *جسم موصى بالجهد العالى*  
*nmos Gate*
- Gate low: transistor ON
- Gate high: transistor OFF
- Bubble indicates inverted behavior

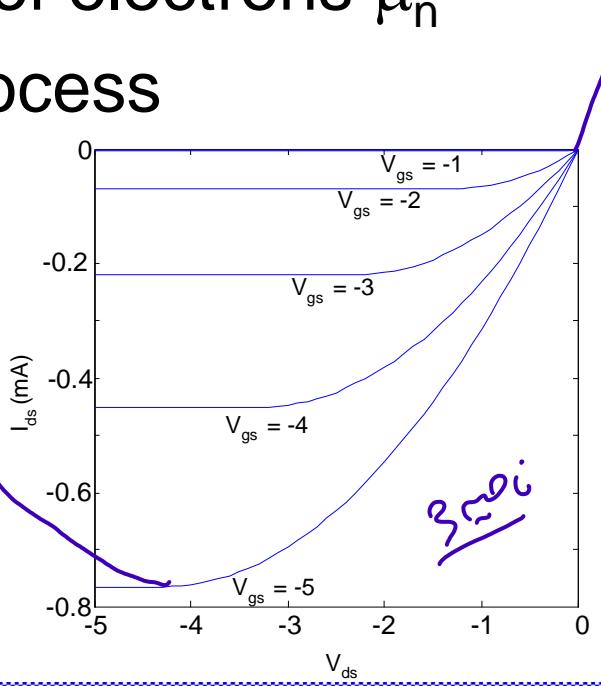


# pMOS I-V

- All dopings and voltages are inverted for pMOS
    - Source is the more positive terminal
  - Mobility  $\mu_p$  is determined by holes
    - Typically 2-3x lower than that of electrons  $\mu_n$
    - $120 \text{ cm}^2/\text{V}\cdot\text{s}$  in AMI 0.6  $\mu\text{m}$  process
  - Thus pMOS must be wider to
    - In this class, assume

$$\mu_n / \mu_p = 2$$

## لیسی فیڈ وارونہ مسٹر



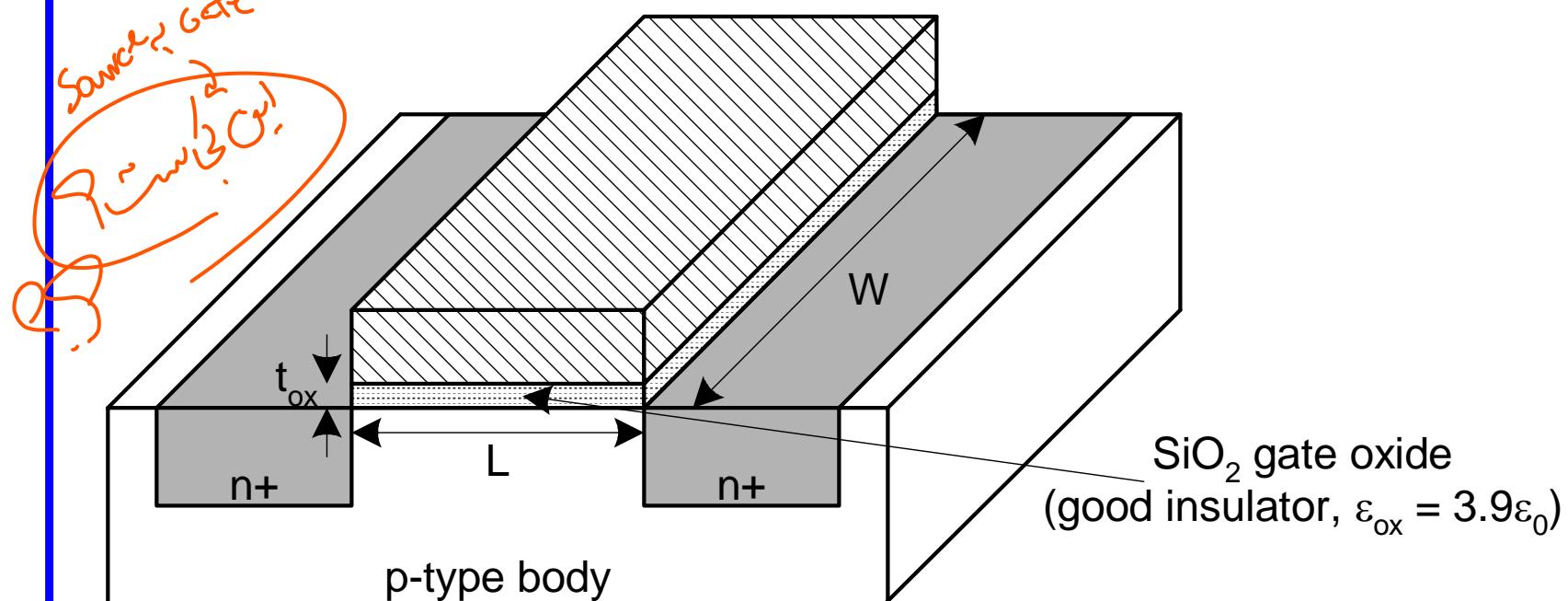
# Capacitance

- Any two conductors separated by an insulator have capacitance خواص چند چیزی که میان دو قطب قرار گیرند
- Gate to channel capacitor is very important ↗  $C_{gc}$ 
  - Creates channel charge necessary for operation
- Source and drain have capacitance to body
  - Across reverse-biased diodes
  - Called **diffusion capacitance** because it is associated with source/drain diffusion

خواص داخل چند چیزی که میان سلیمانی و Body و drain و Body ! Source  
diffusion Capacitance ← چند چیزی که میان (p-N junction) قرار گیرند

# Gate Capacitance

- Approximate channel as connected to source
- $C_{gs} = \epsilon_{ox} WL/t_{ox} = C_{ox} WL = C_{\text{permicron}} W$
- $C_{\text{permicron}}$  is typically about  $2 \text{ fF}/\mu\text{m}$



# Power Supply Voltage

- GND = 0 V
  - In 1980's,  $V_{DD} = 5V$
  - $V_{DD}$  has decreased in modern processes  $\rightarrow$ 
    - High  $V_{DD}$  would damage modern tiny transistors
    - Lower  $V_{DD}$  saves power
  - $V_{DD} = 3.3, 2.5, 1.8, 1.5, 1.2, 1.0, \dots$
- برای اطمینان از میزان مصرف برق،  $\frac{1}{\sqrt{2}}$  از  $V_{DD}$  باید کم باشد، اما معمولاً  $V_{DD}$  برابر باشد با  $\sqrt{2}$  از میزان مصرف برق.
- میزان مصرف برق در حالت دینامیکی:
- $$P_{dynamic} = f_C V_{DD}^2$$