Chapter 8

POWER OPTIMIZATION USING MULTIPLE SUPPLY VOLTAGES

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Multiple supply voltage design is an effective technique for power minimization in CMOS circuits. Clustered Voltage Scaling (CVS) and Extended Clustered Voltage Scaling (ECVS) are the two major methodologies used for assigning the voltage supply to gates in circuits having dual power supplies. This chapter presents current state of the art approaches that combine CVS and ECVS with threshold voltage assignment and gate sizing to enable the maximum reduction in power dissipation. Later we also present a comparison of achievable power savings using CVS and ECVS and point out that ECVS provides appreciably larger power improvements compared to CVS. However, ECVS rests on the availability of well designed asynchronous level converters. We also quantify the impact of the efficiency of level conversion on power savings.

8.1 INTRODUCTION

Dynamic power dissipation in CMOS circuits is proportional to the square of the supply voltage (VDD). A reduction in VDD thus considerably lowers the power dissipation of the circuit. Dual- (or more generally multi-) VDD design is an important scheme that exploits this concept to reduce power consumption in integrated circuits (ICs) [5][30]. Since a reduction in VDD degrades circuit performance, in order to maintain performance in dual-VDD designs, cells along critical paths are assigned to the higher VDD (VDDH) while cells along non-critical paths are assigned to a lower VDD (VDDL). Thus the timing slack available on non-critical paths is efficiently converted to energy savings by use of a second supply voltage. However, level conversion (from VDDL to VDDH) becomes essential at boundaries where a VDDL driven cell feeds into a VDDH driven cell to eliminate the

undesirable static current that otherwise flows. This current flows since the logic "high" signal of the VDDL driven cell cannot completely turn off the PMOS pull-up network of the subsequent VDDH cell.

The use of level converters is largely determined by the algorithm used in assigning VDD to gates. The two major existing algorithms used for VDD assignment are (1) Clustered Voltage Scaling (CVS) [30], and (2) Extended Clustered Voltage Scaling (ECVS) [10]. In CVS, the cells driven by each power supply are grouped ("clustered") together and level conversion is needed only at sequential element outputs (referred to as "*synchronous level conversion*"). In ECVS, the cell assignment is more flexible, allowing level conversion anywhere (i.e., not just at the sequential element outputs) in the circuit. This is referred to as "*asynchronous level conversion*". Since ECVS allows more freedom in VDD assignment, it has been suggested that it potentially provides greater power reductions than CVS [33].

Both CVS and ECVS assign the appropriate power supply to the gates by traversing the circuit from the primary outputs to the primary inputs in reverse topological level order. CVS is based on a topological constraint that only allows a single transition from a VDDH driven cell to a VDDL driven cell along any path from input to output (i.e., a VDDL driven cell may not feed into a VDDH driven cell). Depending on the design, this may greatly reduce the fraction of VDDL assigned gates and degrade the achievable power savings. Alternatively, ECVS relaxes this topological constraint by allowing a VDDL driven cell to feed a VDDH driven cell along with the insertion of a dedicated asynchronous level converter (ALC). However, since ECVS performs this assignment simply by visiting gates one at a time in reverse topological level order, it still assigns supply voltages in a fundamentally constrained manner. Noting these drawbacks, an algorithm that removes the "levelization" approach will be discussed in Section 8.3. Since level converters consume power and timing slack, it is important to consider their effect on the power savings.

Techniques such as gate sizing and dual threshold voltage (Vth) assignment can be combined with dual-VDD assignment in order to realize a more optimized design. Many different approaches have been proposed that use the variables of VDD/Vth/sizing for power optimization. In [34] the authors address the problem of power optimization using simultaneous VDD and Vth assignment. They propose two different approaches depending on whether a system is dynamic or leakage power dominated. The approach for dynamic power dominated systems fails to consider that assigning a gate to high Vth negatively impacts the extent to which other gates in the circuit can be assigned to VDDL and thus fails to consider the optimization of total power. The approach for leakage dominated systems assigns gates to high Vth in the order of their level from the outputs. Since Vth assignment does not impose any topological constraints as in the case of VDD assignment, this approach unnecessarily limits the achievable power savings. Recently, [21] proposed a