Amirkabir University of Technology

(Tehran Polytechnic)

Memory Technologies Course By

Dr. Hammed Farbeh

Homework 1

CE5431 | Spring 2024

Teaching Assistants

Morteza Adelkhani (Madelkhani@aut.ac.ir)

Sarah Zamani (sara.zamani73@aut.ac.ir)

Description:

In this series of homework assignments on memory technology, we aim to assess the academic knowledge you have acquired from this course and prepare you for the final exam. Therefore, please read the questions carefully, analyze them, and if necessary, conduct research on the internet or consult the course slides to provide detailed answers.

Note: If you refer to a source and base your answers on this information, you must cite the reference.

This homework consists of six types of questions designed to assess various aspects of your understanding. Please follow the instructions for each type of question carefully. The questions are organized as follows:

Question Type 1 True or False Questions

Instruction:

-1 Indicate whether each of the following statements is true or false.

-2 explain your reasoning.

Questions:

1) Phase Change Memory (PCM) is more technology-scalable than DRAM.

   1. True 2. False

2) PCM read/write operations are more energy efficient than DRAM read/write operations.

   1. True 2. False

3) PCM provides shorter access latency but has lower endurance compared to NAND flash memory.

   1. True 2. False

4) NVM has lower endurance than DRAM because writes to NVM take much longer.

   1. True 2. False

Question Type 2 **Multiple Choice Questions**

Instruction:

-1 For each statement, choose the answer that best fits.

-2 provide a detailed explanation for your choice.

Questions:

1) One drawback of employing NAND flash memory as a file system is as follows:

   a) Data stored in it deteriorates over time, necessitating regular refreshing.

   b) Its read speeds exhibit unpredictability, posing challenges for I/O scheduling.

   c) The seek times are notably longer compared to traditional disks.

   d) It imposes restrictions on the number of writes per block due to its limited support.

Question Type 3 **Fill-in-the-Blank Questions**

Instruction:

-1 Read each statement carefully.

-2 fill in the blank(s) with the most appropriate word, phrase, sign or number that completes the sentence.

Questions:

1) Complete the table below detailing various types of memory utilized in digital circuits. For "Composition," elucidate how the memory is constructed, such as through latches, capacitors, etc., and for "Noise Resilience," classify as Low, Medium, or High:

	Registers	SRAM	DRAM	Hard Disk	Flash
Approx. Access Time (ns or s)					
Density (Mb/area)					
Volatility					
Approx. Cost/Bit ($)					
Power Usage (W)					

Question Type 4 **Definitional Questions**

Instruction:

-1 Read each question carefully.

-2 Provide a clear and concise definition for the term or concept being asked.

-3 Ensure that your definition is complete and includes all necessary components to accurately describe the term.

-4 Use your own words to explain the concept, unless a direct quote is specifically requested.

Questions:

1) Consider a conventional 6-T SRAM cell optimized for stability under standard operating conditions and integrated within a pre-charged bit-line array; we aim to lower its supply voltage and explore assist techniques for this purpose. Let's delve into the impact of peripheral signals on the cell's operation. Please provide concise one-sentence responses to the following questions:
    a) What is the effect of increased word-line voltage on the read stability of the cell?
    b) How does increased word-line voltage influence the read access time of the cell?
    c) What impact does increase word-line voltage have on the writeability of the cell?
    d) How does a shortened wordline pulse affect the read stability of the cell?
    e) What is the effect of a lengthened wordline pulse on the writeability of the cell?
    f) How does an elevated cell supply voltage (without altering other signal levels) affect the writeability of the cell?

2) Magnetoresistive Random Access Memory (MRAM) and Phase-change memory (PRAM or PCRAM) represent two types of non-volatile memory with potential applications in future consumer devices and embedded systems. Compare and

contrast these technologies by elucidating their operational principles, primary advantages as substitutes for DRAM and/or SRAM, benefits for embedded system designers, limitations, and areas where they may not be well-suited.

3) Analyze the role of SSD technology in the shift away from hard-disk drives (HDD) toward solid-state storage, particularly in the realms of consumer electronics and enterprise infrastructure.

4) Elaborate on the NVMe interface protocol and its superiority over conventional HDD-related interfaces like SATA, emphasizing performance metrics such as transfer rates.

5) Differentiate between a floating-gate transistor and a standard planar MOSFET in terms of their structural composition. Explain the significance of the floating gate's absence of a direct connection to external terminals.

Question Type 5 **Scenario Based Question**

Instruction:

-1 Carefully read the provided scenario to understand the context and details.

-2 Identify the key issues or problems presented in the scenario.

-3 Answer the questions that follow, applying the relevant concepts or theories.

-4 Your responses should be based on the information given in the scenario and your understanding of the subject matter.

-5 Provide detailed explanations and justifications for your answers.

Questions:

1) **Develop a Computer System for Deep Space Mission**

You are assigned the development of a computer system for an extensive deep space mission aimed at exploring a remote exoplanet. This mission will involve the acquisition and analysis of substantial scientific data over an extended period, with restricted bandwidth for data transmission back to Earth. The spacecraft will be outfitted with a variety of sensors, cameras, and scientific apparatuses to collect information on the exoplanet's atmospheric conditions, geological features, and possible indications of life.

Challenge 1: System Architecture Design

Devise an architecture for the computer system that employs a structured memory hierarchy, incorporating various non-volatile memory types, to manage

the data obtained throughout the deep space mission. Select the optimal memory unit for each tier of the hierarchy, taking into account the following factors:

a) The necessity for dependable, space-hardened non-volatile memories that can endure the extreme space environment.

b) Approaches to reduce power usage and enhance storage capacity, given the spacecraft's power and size constraints.

c) Techniques to preserve data integrity and reduce the chances of data loss or corruption over the mission's duration.

d) The integration of fault-tolerant features to address potential hardware malfunctions or errors caused by radiation.

e) Methods for effective data access and processing, considering the spacecraft's limited computational capabilities.

f) The harmonization of non-volatile memory systems with other computer system elements, such as CPUs, communication interfaces, and power control units.

Challenge 2: Memory Hierarchy Selection

For each segment of the memory hierarchy (e.g., cache, primary memory, secondary storage), identify the most suitable non-volatile memory type (e.g., NAND flash, NOR flash, phase-change memory, resistive random-access memory), based on its properties and the mission's unique demands. Support your selections by explaining how each memory type meets the aforementioned

critical aspects.

Challenge 3: Backup and Redundancy Plan

Suggest a contingency and duplication strategy for the non-volatile memory subsystem to guarantee the safeguarding of essential data in case of a severe malfunction or unforeseen irregularity during the mission. Determine the most fitting redundancy method (e.g., duplication, parity, RAID) and backup protocol (e.g., regular data duplication to a backup storage unit, error-correcting codes) for each memory hierarchy level. Describe how your strategy will minimize risks and contribute to the mission's success.

2) SRAM Memory Block Design

Imagine you're tasked with designing an SRAM memory block intended to hold 1024 words, each comprising 32 bits.

Challenge: Achieving Balanced Delay in SRAM Memory Block Design

Incorporate the specificities of a 6T cell design where the word line connects to the gate of both access transistors and each bit line connects to the source/drain node of one access transistor. Assume that the capacitance of an access transistor gate is equivalent to the source/drain capacitance.

How many address bits are needed for the row decoder, and how many for the column decoder to achieve a balanced delay between the word line and bit line?

Question Type 6 **Design-Based Questions**

Instruction:

-1 read each question thoroughly to understand the design problem presented.

-2 Consider all the requirements and constraints specified in the question.

-3 Develop a solution that addresses the problem, keeping in mind practicality and feasibility.

-4 Sketch your design clearly, detailing how it meets the criteria given.

Questions:

1) Your objective in this task is to create the circuitry for a dual-ported ROM that is 4-bit wide and 4-word deep. This ROM features two separate ports, each equipped with a 2-bit address bus and a 4-bit data bus, allowing simultaneous access to any of the four stored data words. Initiate the design process by adapting the basic single-ported ROM cells provided. Subsequently, sketch a circuit schematic for the entire dual-ported ROM, encompassing all essential circuits. The contents of the ROM are detailed below.

address	Value
00	0101
01	1010
10	0101
11	1010