In the name of God

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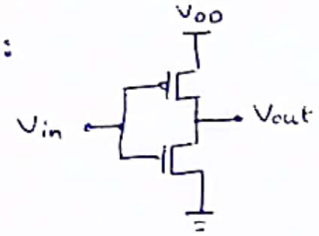
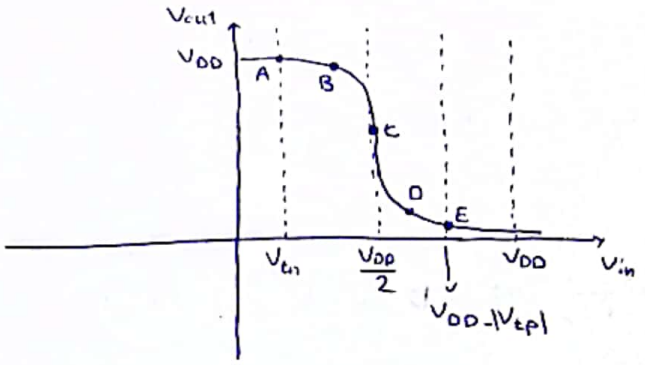
HW02

2.16 :





I should equalize the current of the transistors in the B region.

In B regin
- nMOS in saturation $\Rightarrow \frac{K'_n W}{L}\left(V_{gs}-V_{th,n}\right)^2 = I_{ds(n)}$
- pMOS in linear $\Rightarrow \frac{K'_p W}{L}\left[V_{gs}-V_{th,p}-\frac{V_{ds}}{2}\right]V_{ds} = I_{ds(p)}$

$$\Rightarrow I_{ds(n)} = I_{ds(p)} \;:\; \left(V_{gs}-V_{th,n}\right)^2 = \left(V_{gs}-V_{th,p}-\frac{V_{ds}}{2}\right)V_{ds} \xrightarrow{V_{th,n}=V_{th,p}=V_{th}}$$

$$\Rightarrow \left(V_{in}-V_{th}\right)^2 = \left(V_{in}-V_{out}+V_{th}-\frac{1}{2}\left(V_{out}-V_{DD}\right)\right)\left(V_{out}-V_{DD}\right)$$

$$\Rightarrow V_{in}^2+V_{th}^2-2V_{in}V_{th} = V_{out}V_{in}-V_{out}^2+V_{out}V_{th}-\frac{1}{2}V_{out}^2+\frac{1}{2}V_{out}V_{DD}-V_{in}V_{DD}+V_{out}V_{DD}$$
$$-V_{th}V_{DD}+\frac{1}{2}V_{out}V_{DD}-\frac{1}{2}V_{DD}^2$$

$$\Rightarrow V_{in}^2+V_{th}^2+V_{in}V_{DD}-2V_{in}V_{th}+V_{DD}V_{th}+\frac{1}{2}V_{DD}^2 = V_{out}\left[V_{in}-V_{out}+V_{th}-\frac{1}{2}V_{out}+\frac{1}{2}V_{DD}+V_{DD}+\frac{1}{2}V_{DD}\right]$$

$$\Rightarrow V_{out} = \left(V_{in}+V_{th}\right)+\left[\left(V_{in}+V_{th}\right)^2-\left(V_{in}-V_{th}\right)^2+V_{DD}\left(V_{DD}-2V_{in}-2V_{th}\right)\right]^{\frac{1}{2}}$$

Repeat this calculation for D regin →
- PMOS in saturation
- nMOS in Linear

$$\Rightarrow \cancel{K'_n}\cancel{\frac{W}{L}}\left[V_{gs}-V_{th,n}-\frac{V_{ds}}{2}\right]V_{ds} = \cancel{K'_p}\cancel{\frac{W}{L}}\left(V_{gs}-V_{th,p}\right)^2 \xrightarrow{V_{thp}=V_{thn}}$$

$$\Rightarrow \left(V_{in}-V_{th}-\frac{1}{2}V_{out}\right)V_{out} = \left(V_{in}-V_{DD}+V_{th}\right)^2 \Rightarrow V_{out} = \left(V_{in}-V_{th}\right) - \sqrt{(V_{in}-V_{th})^2-(V_{DD}-V_{in}-V_{th})^2}$$

2.17 : noise margin for Inverter operating at 1^V with $V_{tn}=|V_{tp}|=0.35^V$, $\beta_p=\beta_n$

we must calculate $\frac{dV_{out}}{dV_{in}}$ at D and B point.

I) for point B : $V_{out} = (V_{in}+V_t) + \left[(V_{in}+V_t)^2-(V_{in}-V_t)^2+V_{DD}(V_{DD}-2V_{in}-2V_t)\right]^{\frac{1}{2}}$

$\xrightarrow[V_t=0.35^V]{V_{DD}=1^V}$ $V_{out} = (V_{in}+0.35) + \sqrt{(V_{in}+0.35)^2-(V_{in}-0.35)+1(1-2V_{in}-2(0.35))}$

$\begin{cases} V_{in} \geq 1.89^V \longrightarrow V_{out} \text{ is complex} \longrightarrow \text{unacceptable} \\ V_{in} \leq 0.408^V \longrightarrow V_{out} = 0.781^V \checkmark \longrightarrow \begin{cases} V_{IL} = 0.408^V \\ V_{OH} = 0.781^V \end{cases} \end{cases}$

II) for point D : $V_{out} = (V_{in}-V_t) - \sqrt{(V_{in}-V_t)^2-(V_{DD}-V_{in}-V_t)^2} \xrightarrow[V_t=0.35]{V_{DD}=1}$

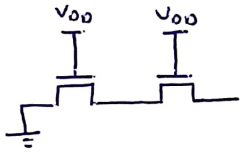
$V_{out} = (V_{in}-0.35) - \sqrt{(V_{in}-0.35)^2-(1-V_{in}-0.35)^2}$

$\Rightarrow \begin{cases} V_{in} \geq 0.5^V \longrightarrow V_{out} = 0.15^V \end{cases} \Rightarrow \begin{cases} V_{IH} = 0.5^V \\ V_{OL} = 0.15^V \end{cases}$

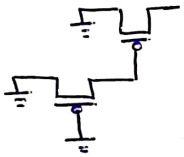
$$NM_H = V_{OH}-V_{IH} = 0.781-0.5 = \boxed{0.281^V}$$

$$NM_L = V_{IL}-V_{OL} = 0.408-0.15 = \boxed{0.258^V}$$

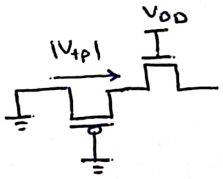
2.20 :

a) 

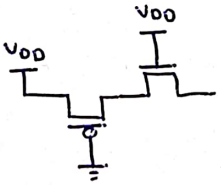
: Pass transistor Pass 0 because nMOS transistor Pass strong 0

b) 

: Pass transistor Pass $|V_{tp}|$ because pMOS transistor Pass strong 1 and degraded 0

c) 

: PMOS transistor pass $|V_{tp}|$ and nMOS Transistor pass the same $|V_{tp}|$

d) 

: PMOS transistor pass 1 and nMOS transistor pass $V_{DD} - V_{tn}$ because degraded 1