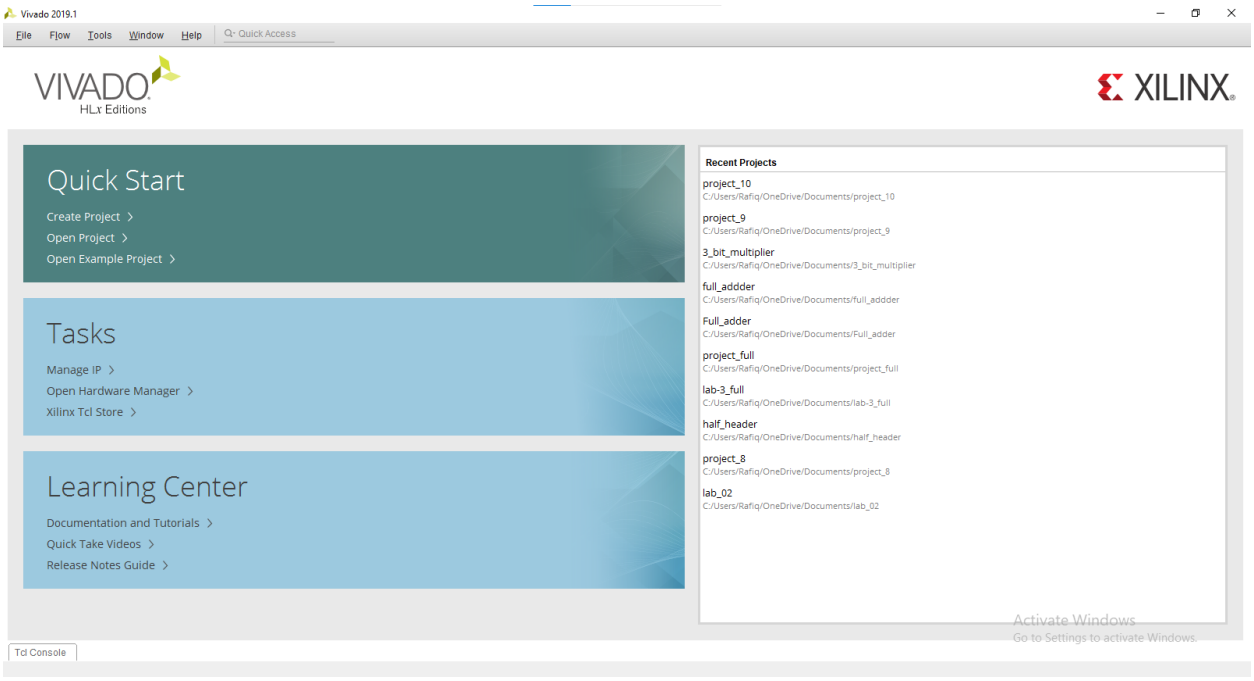
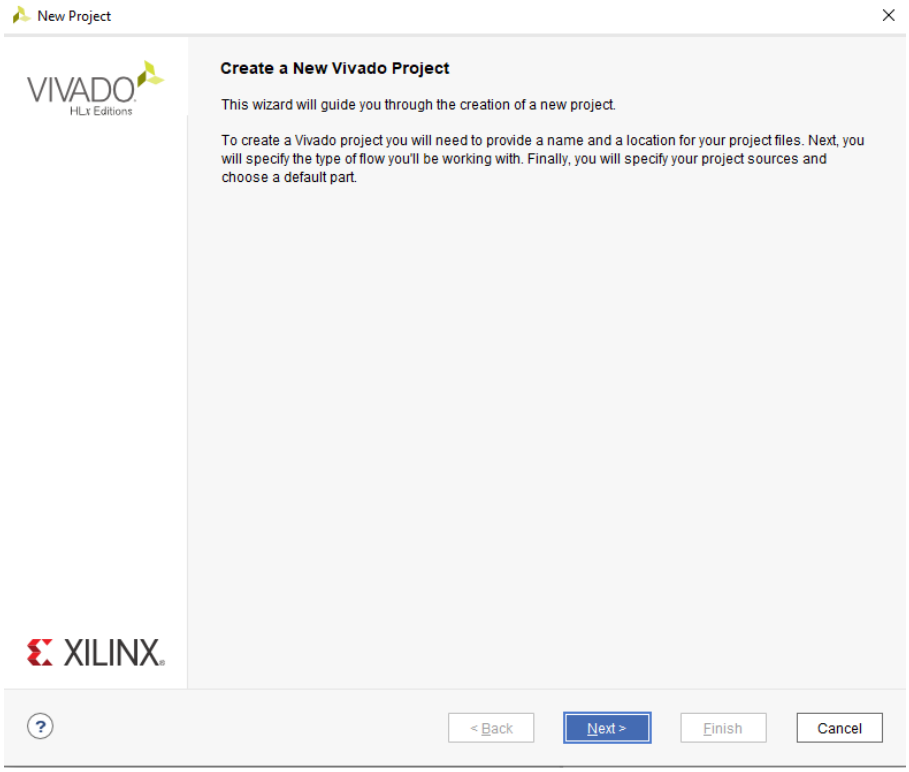
How to create your First Project in VIVADO?

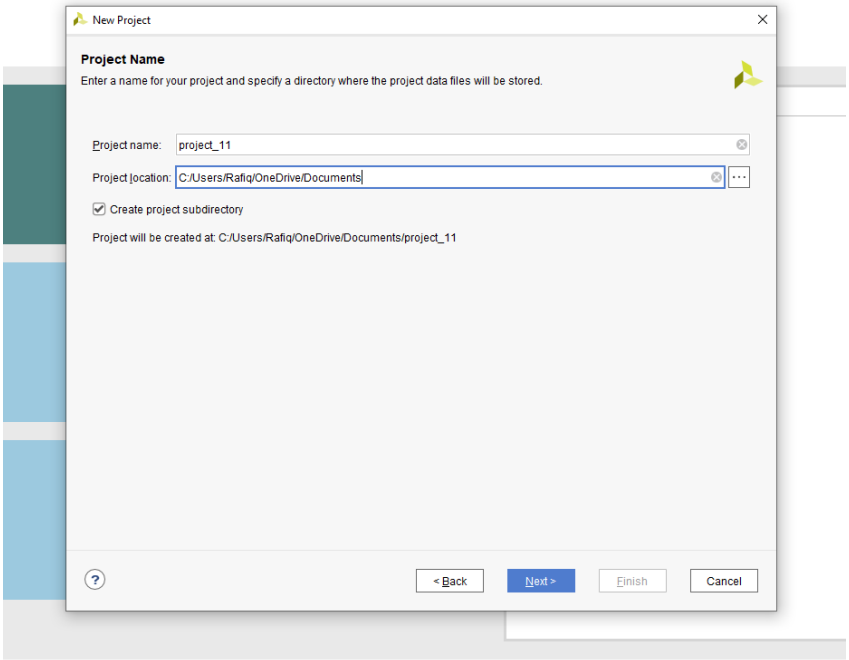
1. Create a new project **OR** open a project



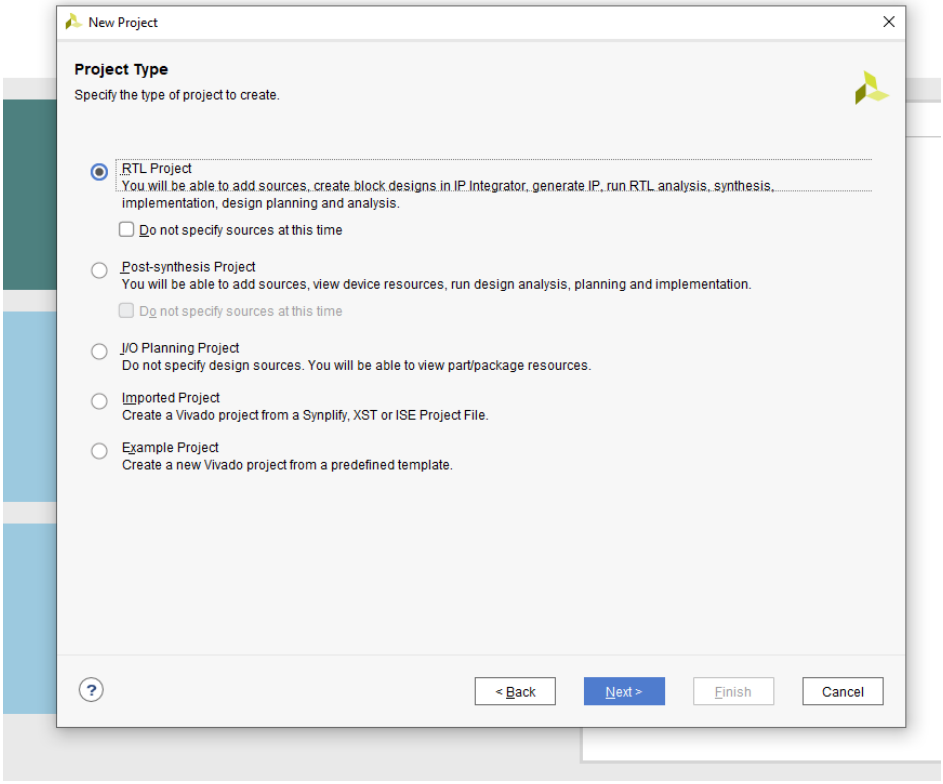
2. Click next



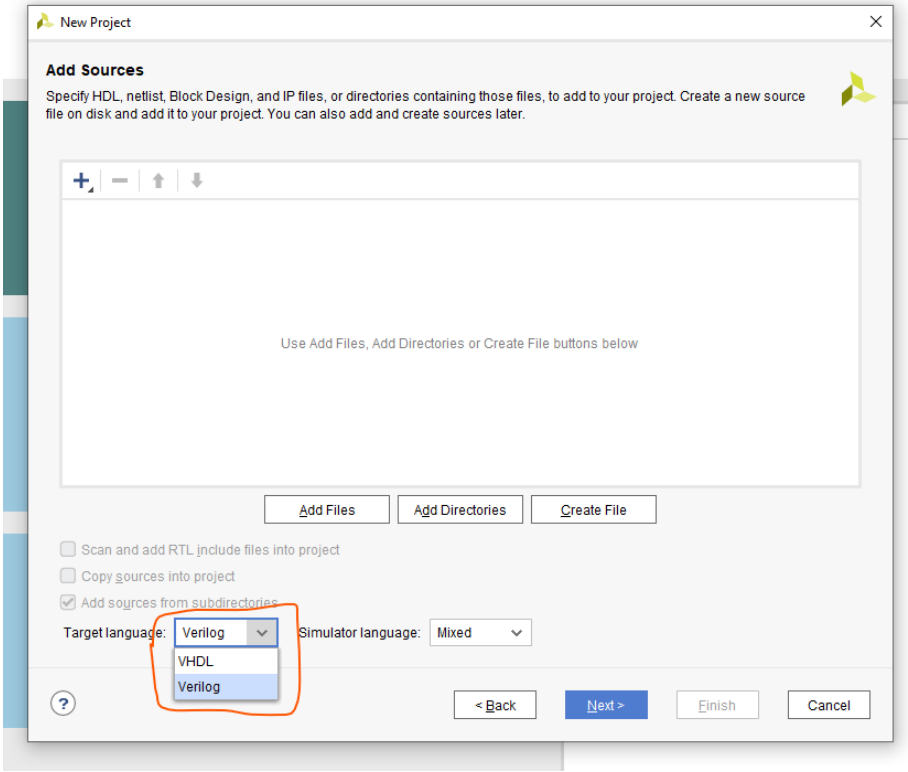
3. Enter project name and location



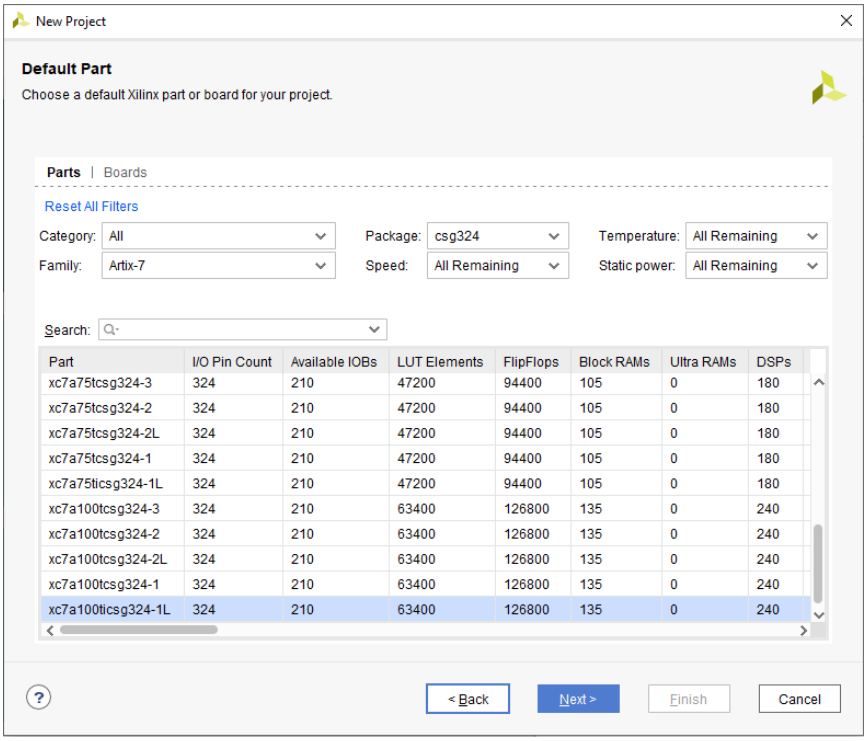
4. Choose RTL Project



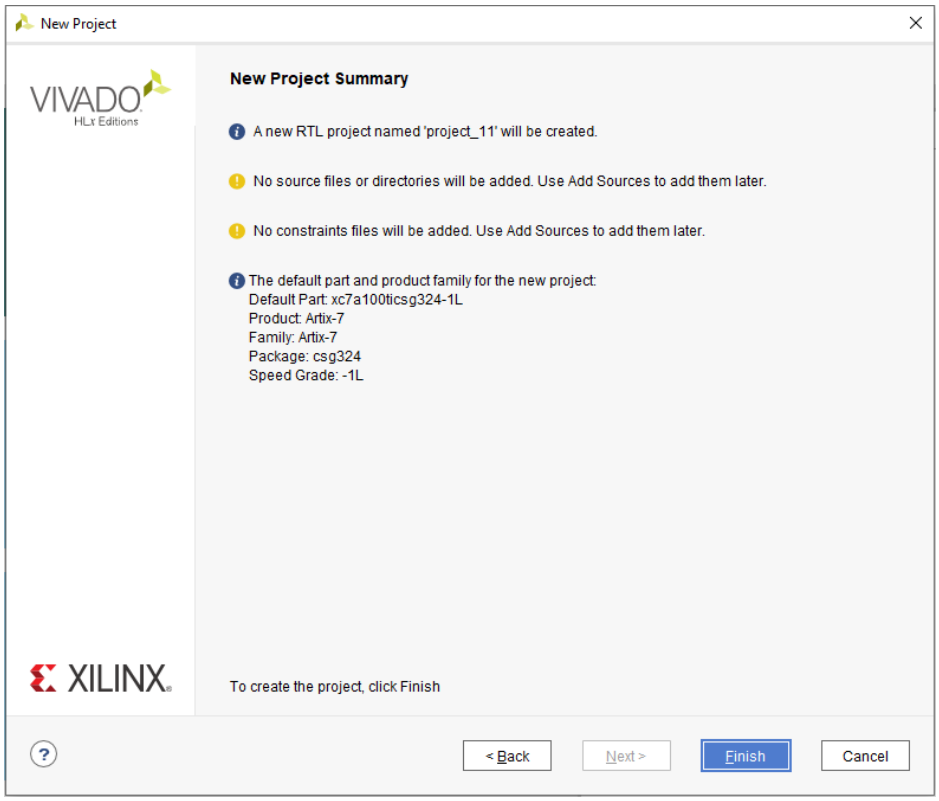
5. Choose target language Verilog



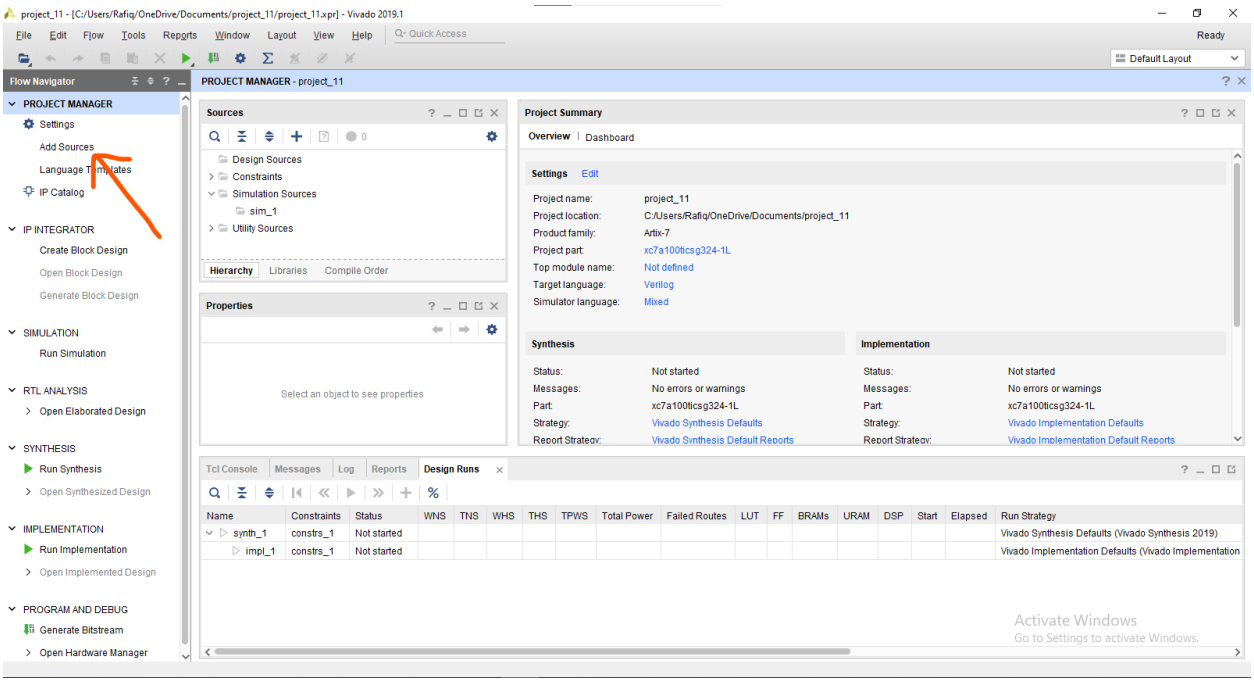
6. Choose Board family, package and part according to FPGA that you have. So, I my case I choose Artix-7 , csg324 and XC7A100T-1CSG324C respectively.



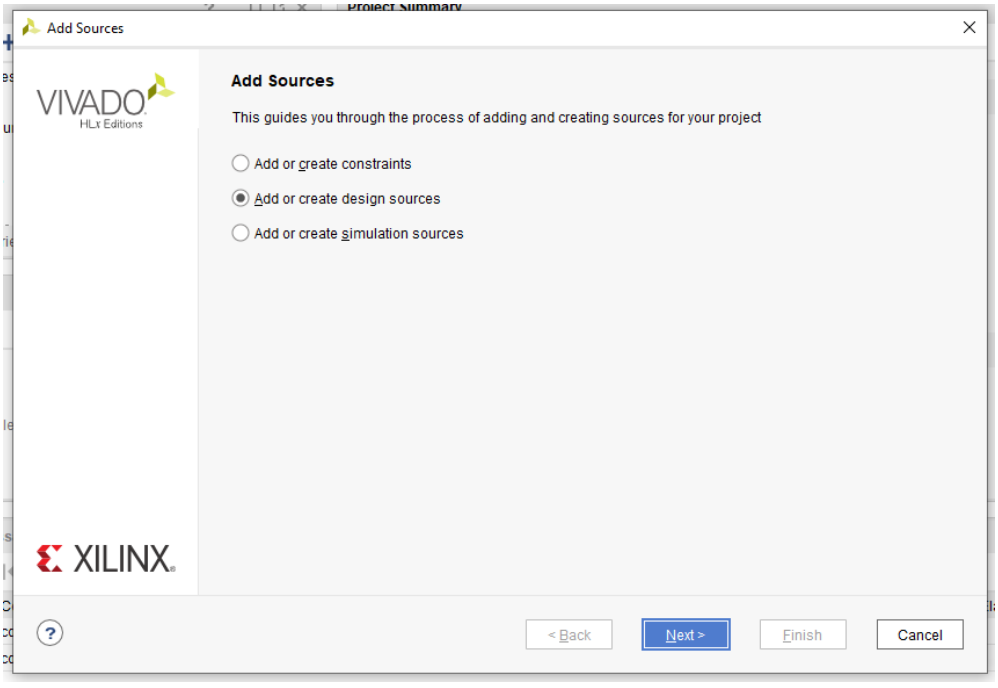
7. And finish project



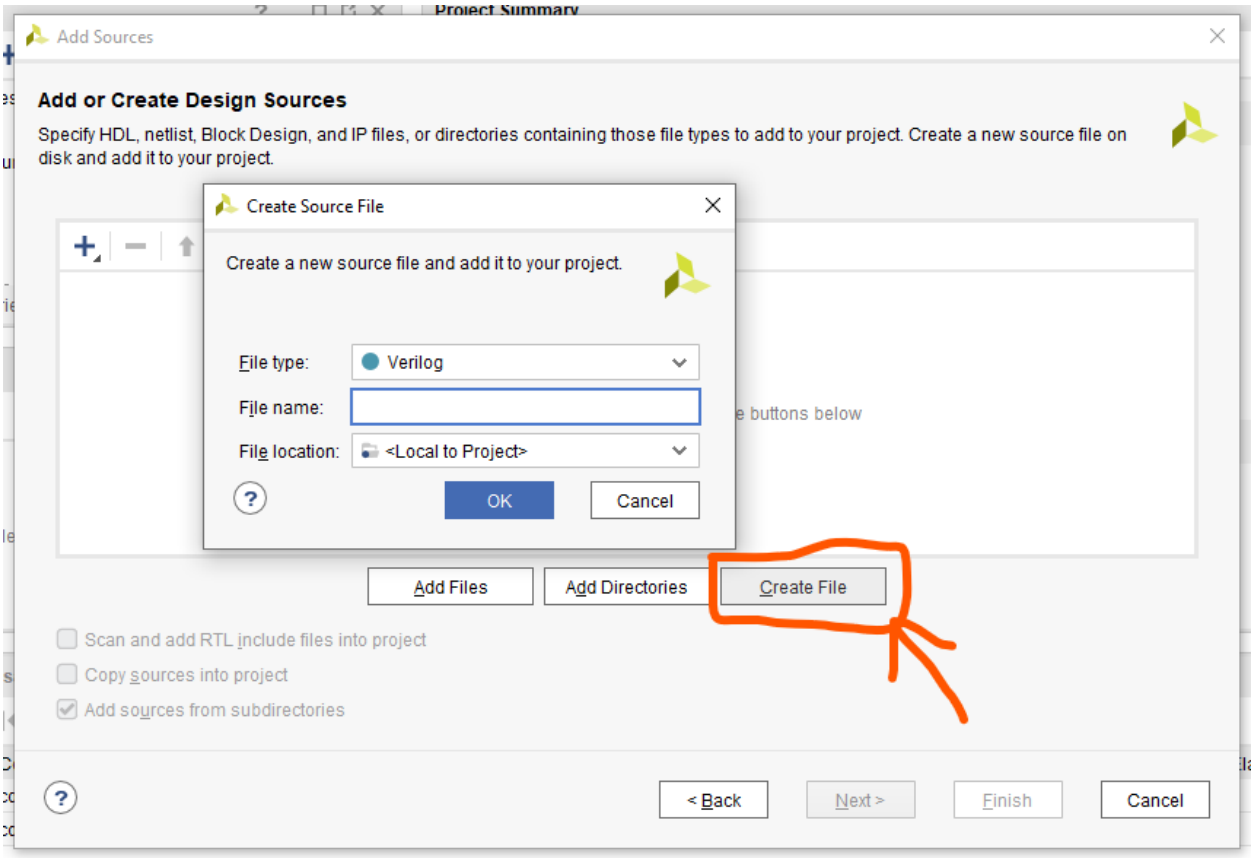
8. Add source file in your project



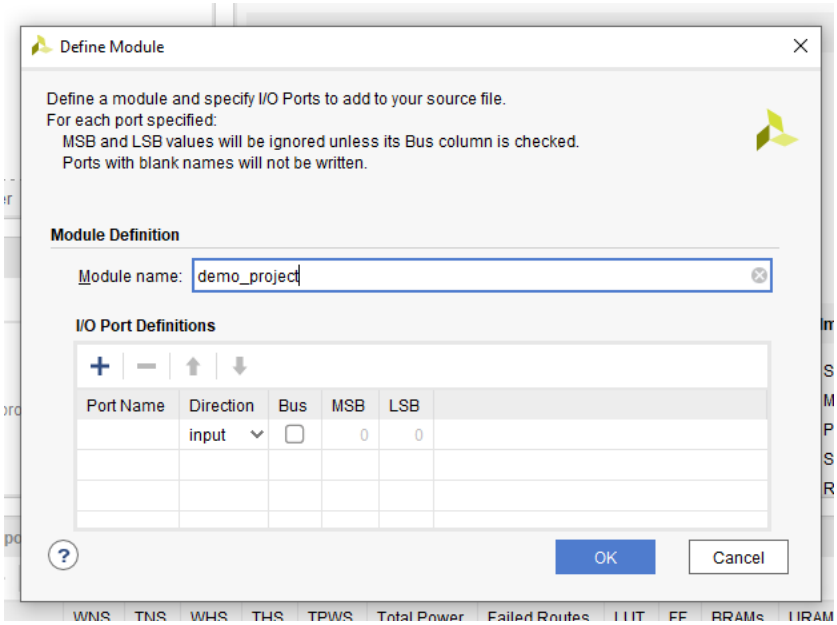
9. Choose add or create design source option



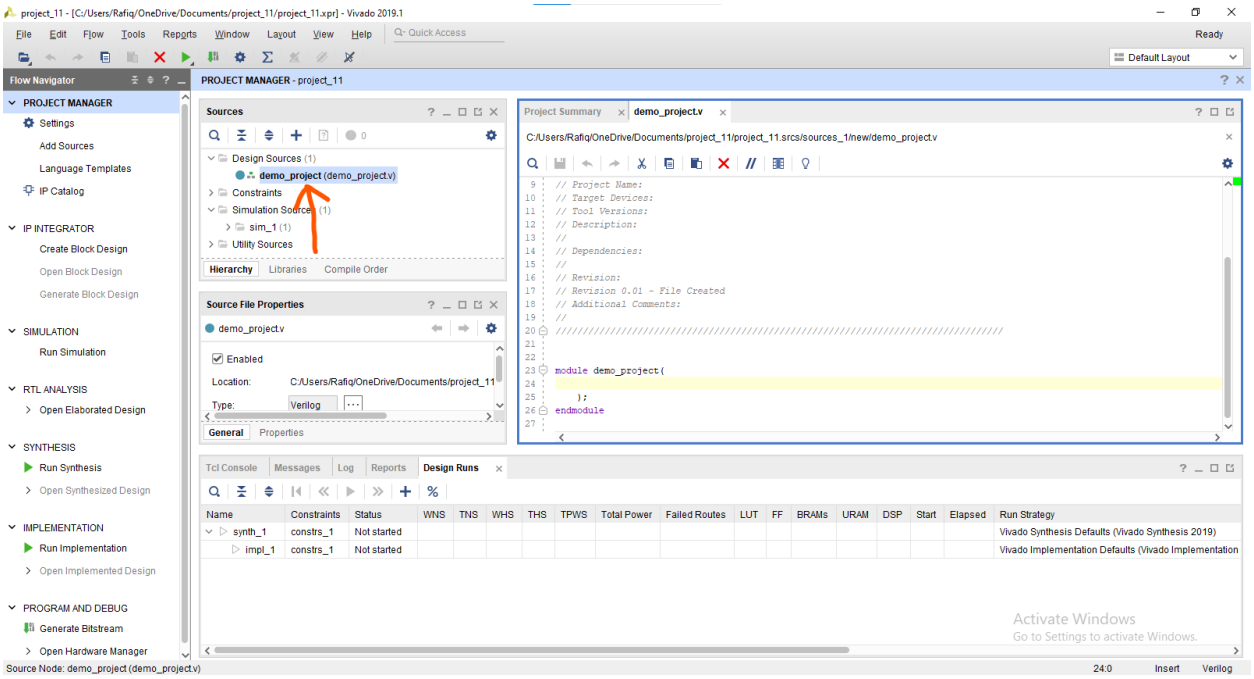
10. Click on create file and enter file name after that click on OK.



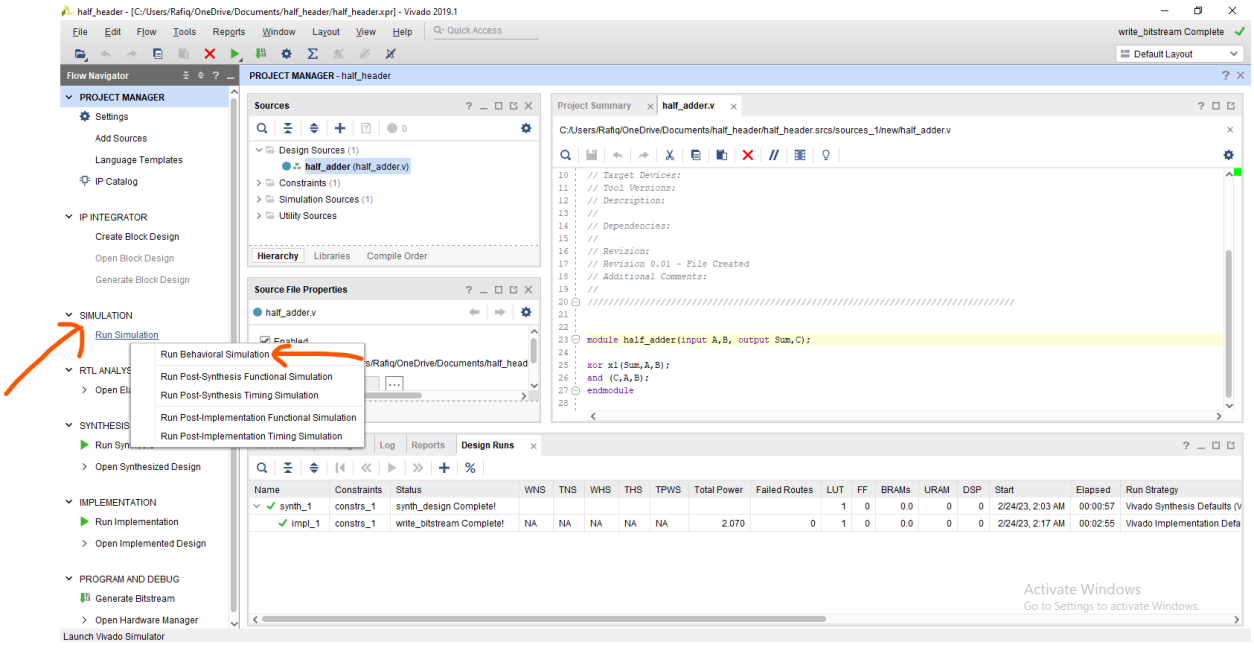
11. If you want to create I/O ports before code then enter the port name otherwise simple click ok



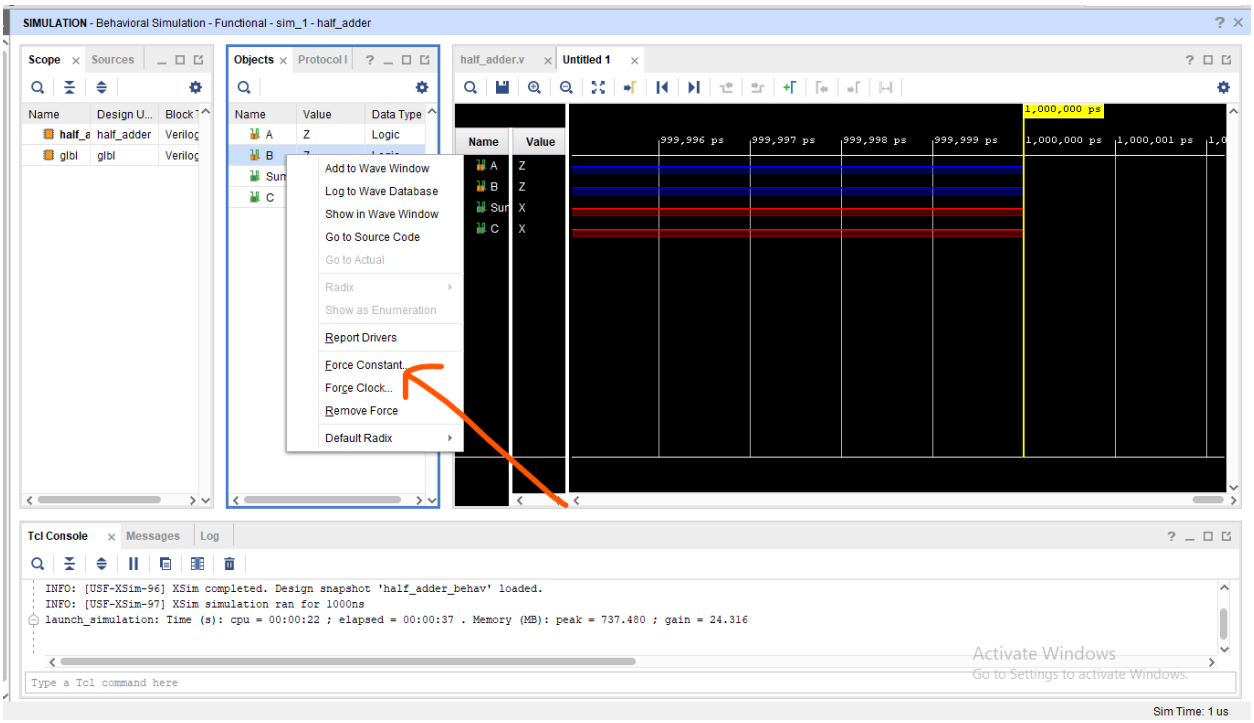
12. A Verilog file is shown under the design source in SOURCES tab.



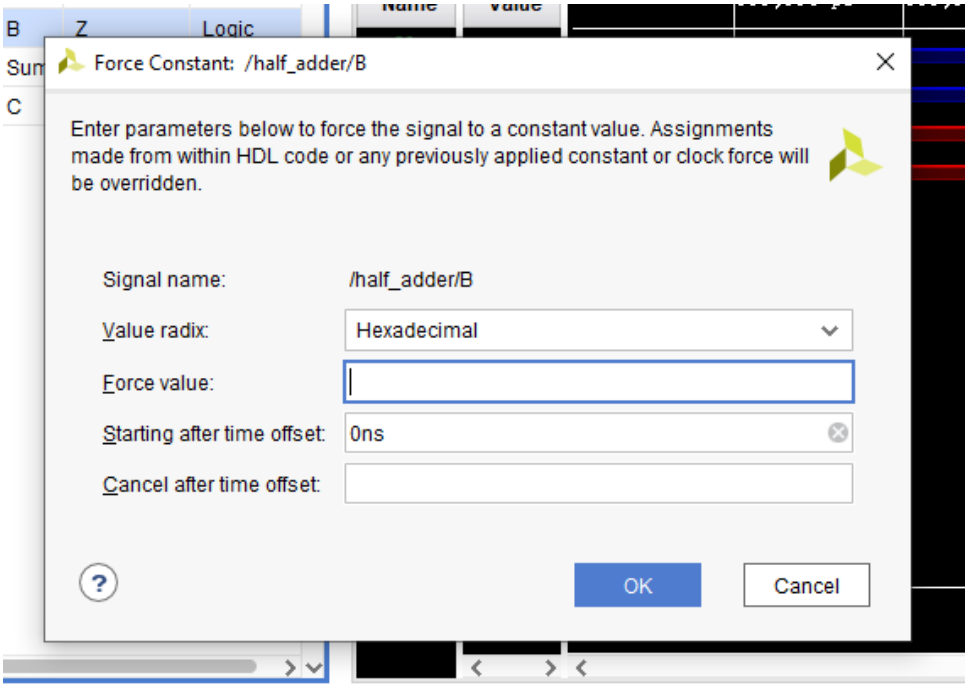
13. After writing code in Verilog click on Run simulation



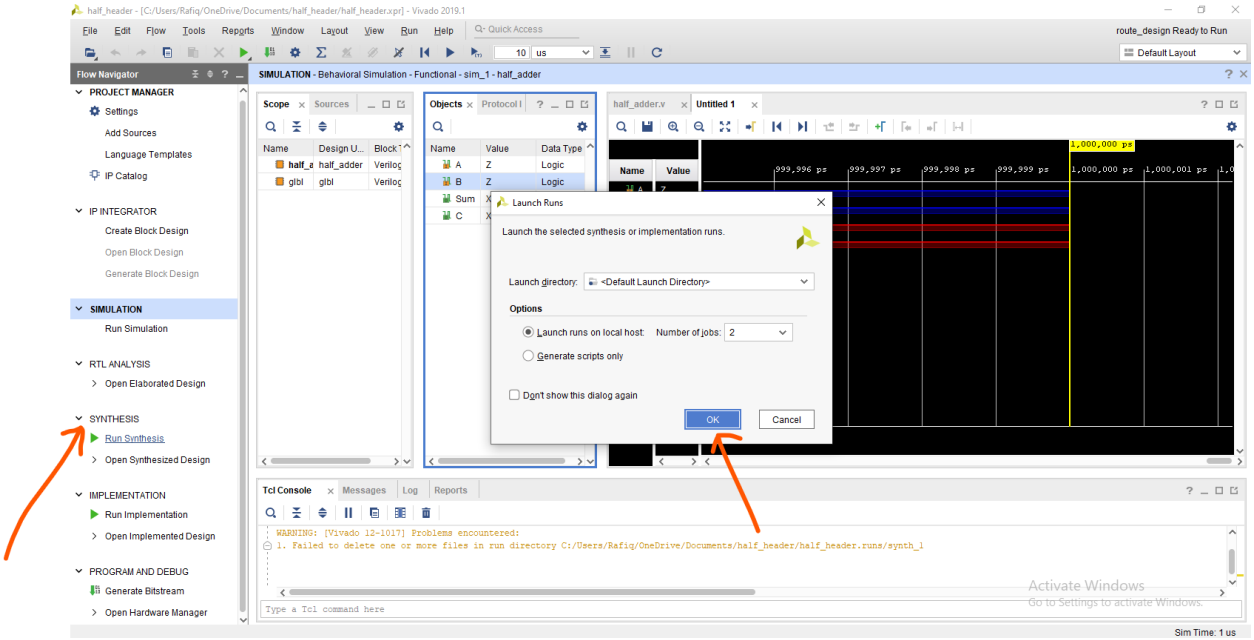
14. After runs the simulation Give force constraint to input to check weather your code is running successfully or not.



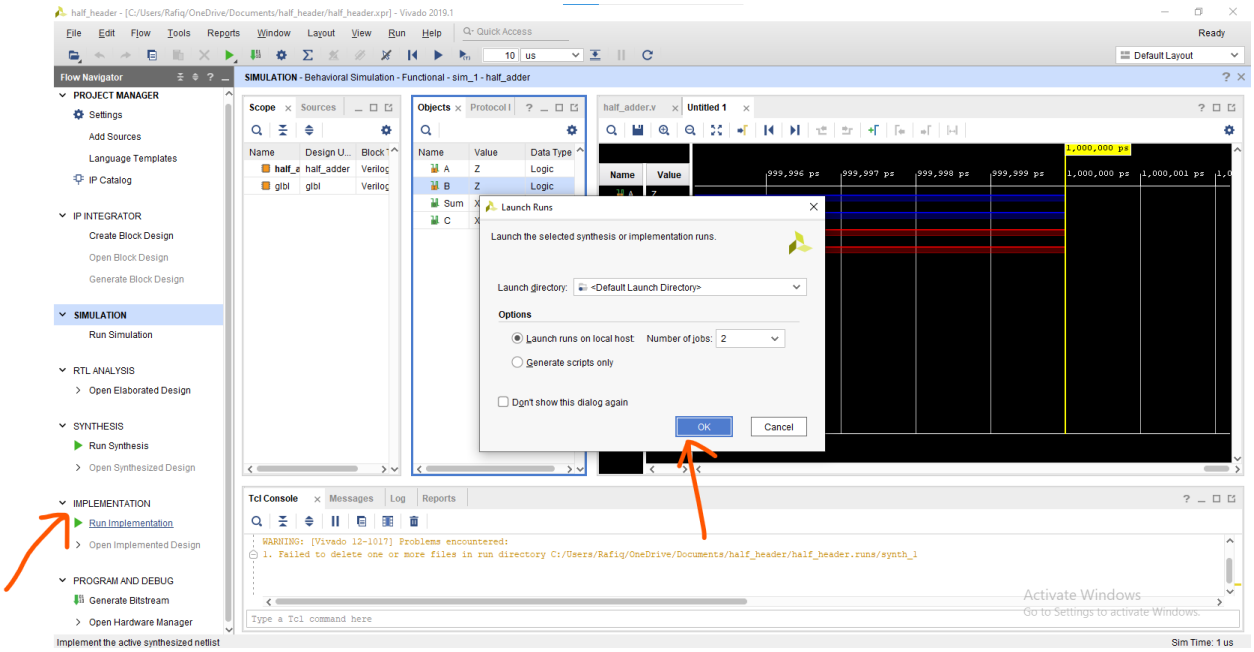
15. Give force constraint value 1 or 0 according to your need.



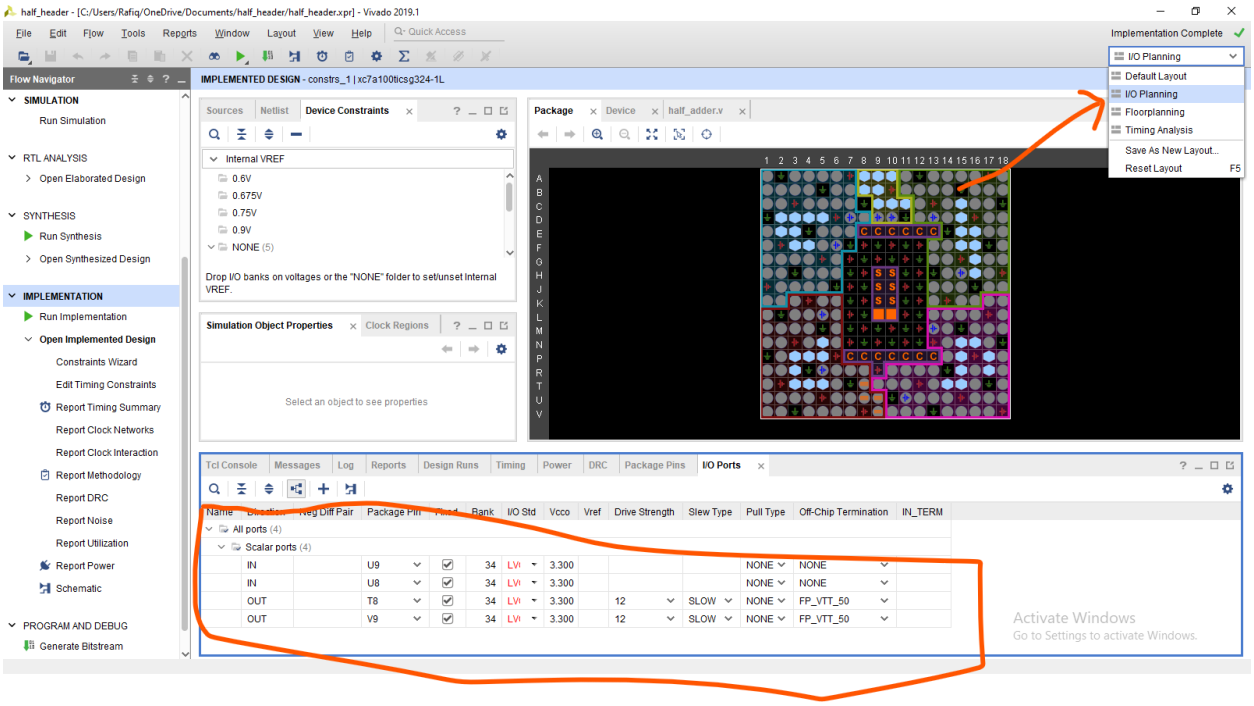
16. Now synthesis your project



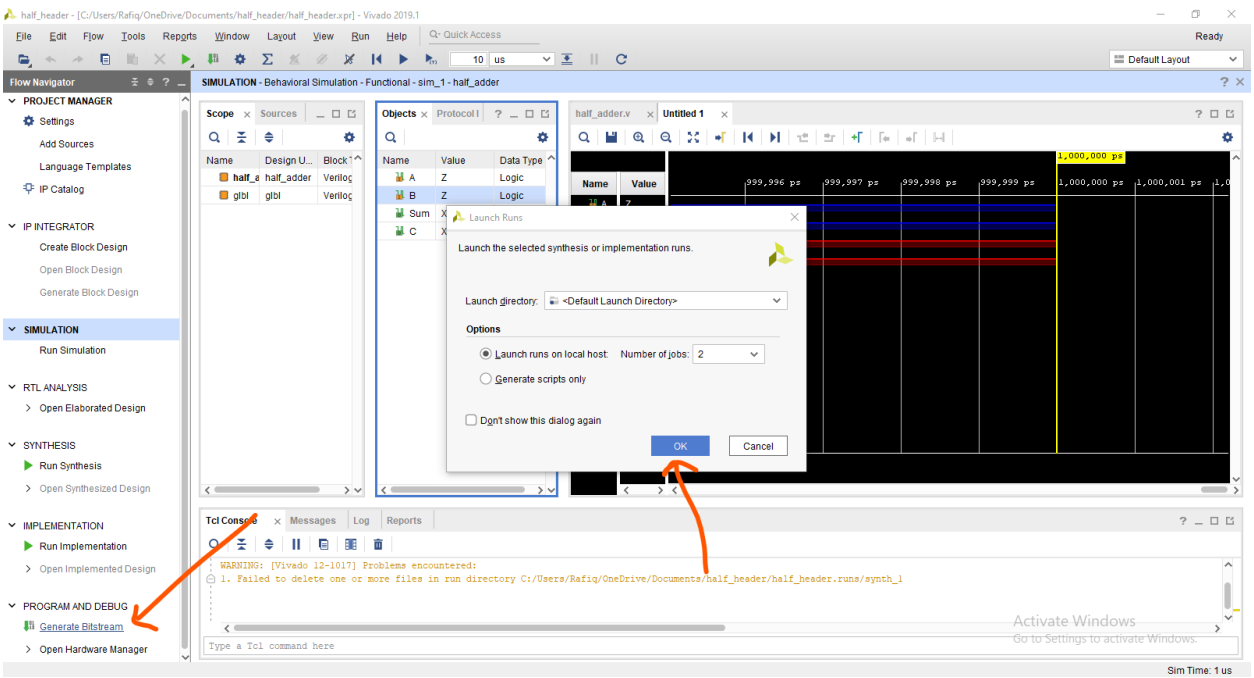
17. After completion of synthesis we run implementation



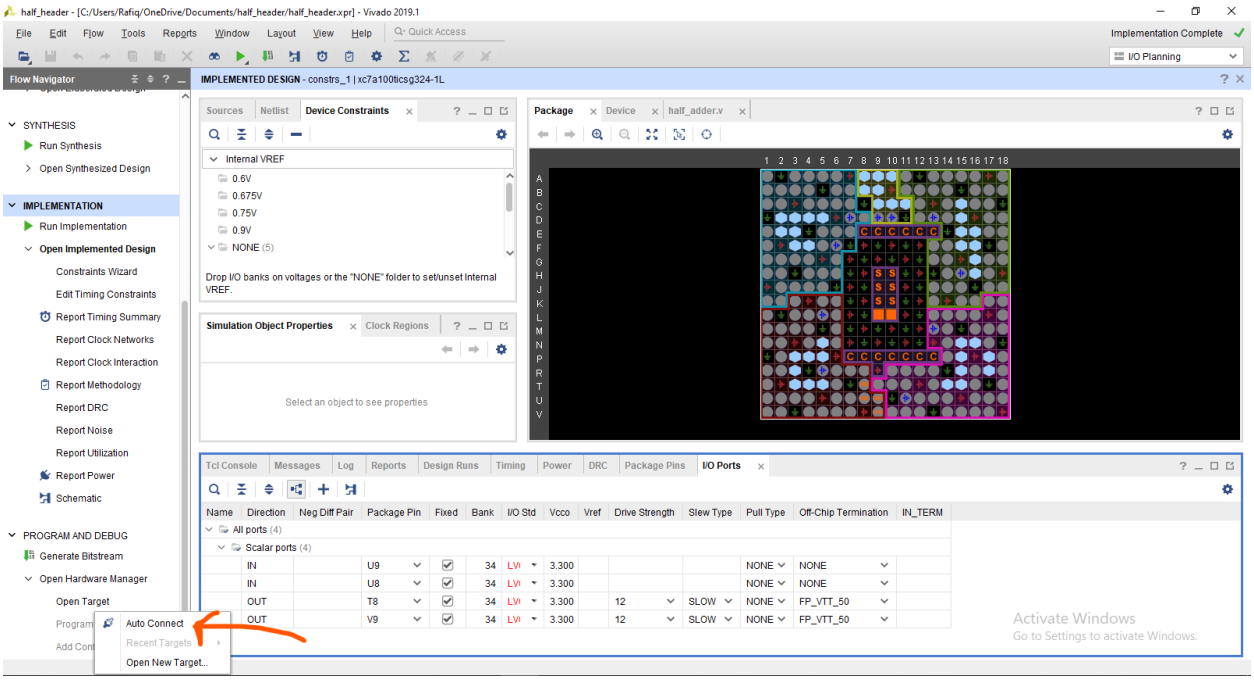
18. Implementation take sometime and after that we select I/O port



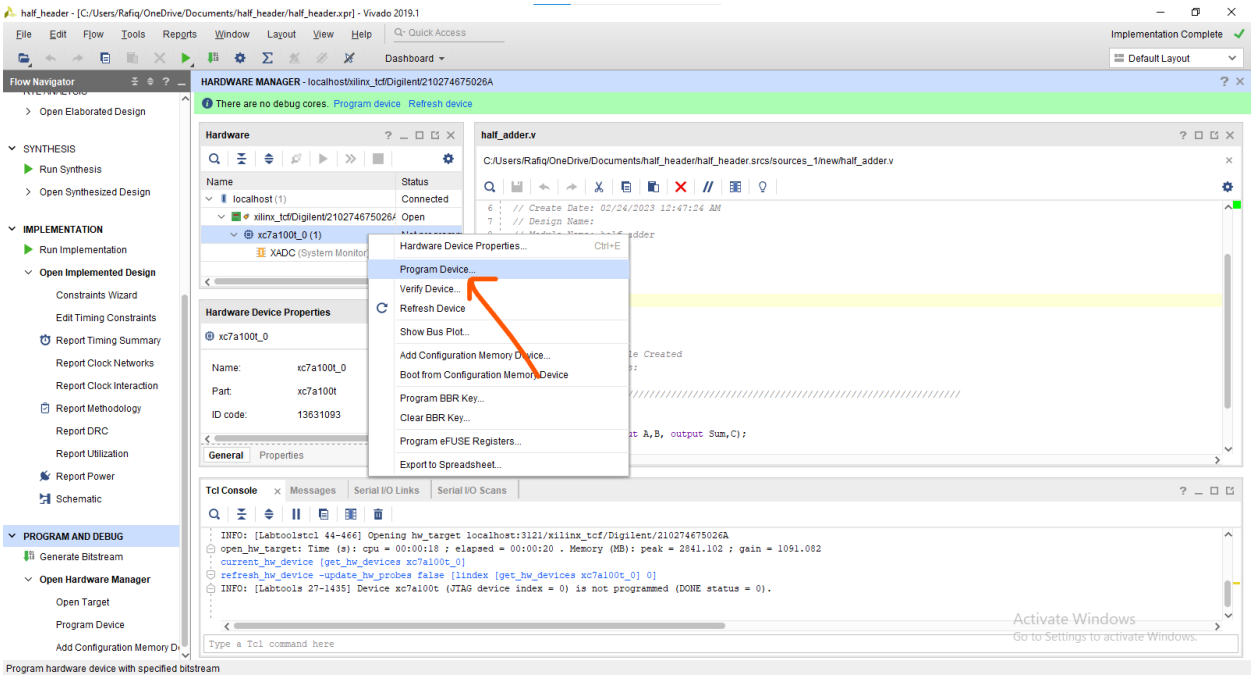
19. Now generate the bitstream of the project



20. Select targeted FPGA under open hardware manager



21. Click on program device



22. Now generate **.bit** file

First you copy the file address where you save your project.

in my case my file address is (**C:\Users\Rafiq\OneDrive\Documents\half_header**)

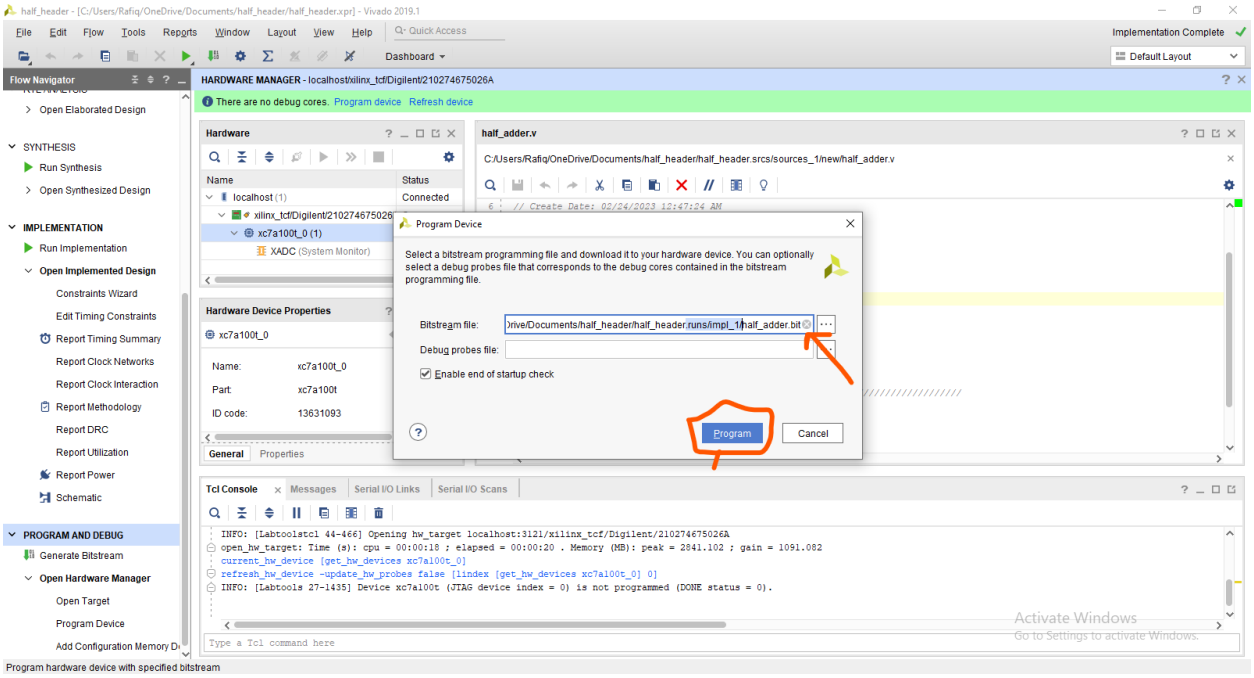
now simply I add project my project name in file address
(**C:\Users\Rafiq\OneDrive\Documents\half_header\half_header**)

now add .runs/impl_1/ in my address

C:\Users\Rafiq\OneDrive\Documents\half_header\half_header\ .runs\impl_1

add **.v** file name in address

C:\Users\Rafiq\OneDrive\Documents\half_header\half_header\ .runs\impl_1\half_adder.bit



After that click on program and your code in implemented your FPGA kit.

Thanks you.