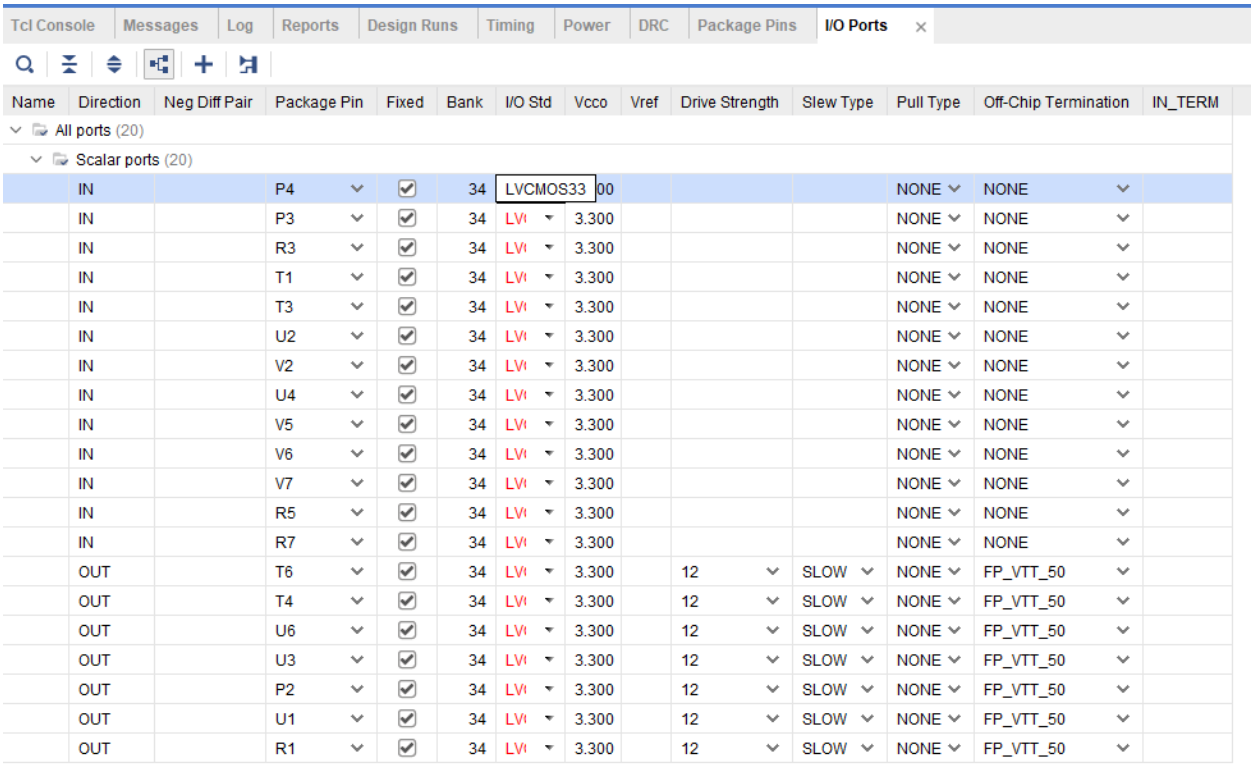
Logic Gates Implementation

```
module lab_02(input a,b,c,e,d,f,g,i,j,k,l,m,n  ,  output x,y,z,w,v,u,t
  );


   assign x= a&b;              //and gate
   assign y= c|d;              // or gate
   assign z= ~e;               // not gate
   assign w= ~(f&g);         //Nand gate
   assign v= ~(i&j);          //nor gate
   assign u= k^l;              //xor gate
   assign t= ~(m^n);         //xnor gate


endmodule
```

Port Assign according in NEXYS-4 ARTIX-7 board



Tcl Console | Messages | Log | Reports | Design Runs | Timing | Power | DRC | Package Pins | I/O Ports

Name	Direction	Neg Diff Pair	Package Pin	Fixed	Bank	I/O Std	Vcco	Vref	Drive Strength	Slew Type	Pull Type	Off-Chip Termination	IN_TERM
All ports (20)													
Scalar ports (20)													
	IN		P4	☑	34	LVCMOS33	00				NONE	NONE	
	IN		P3	☑	34	LVI	3.300				NONE	NONE	
	IN		R3	☑	34	LVI	3.300				NONE	NONE	
	IN		T1	☑	34	LVI	3.300				NONE	NONE	
	IN		T3	☑	34	LVI	3.300				NONE	NONE	
	IN		U2	☑	34	LVI	3.300				NONE	NONE	
	IN		V2	☑	34	LVI	3.300				NONE	NONE	
	IN		U4	☑	34	LVI	3.300				NONE	NONE	
	IN		V5	☑	34	LVI	3.300				NONE	NONE	
	IN		V6	☑	34	LVI	3.300				NONE	NONE	
	IN		V7	☑	34	LVI	3.300				NONE	NONE	
	IN		R5	☑	34	LVI	3.300				NONE	NONE	
	IN		R7	☑	34	LVI	3.300				NONE	NONE	
	OUT		T6	☑	34	LVI	3.300		12	SLOW	NONE	FP_VTT_50	
	OUT		T4	☑	34	LVI	3.300		12	SLOW	NONE	FP_VTT_50	
	OUT		U6	☑	34	LVI	3.300		12	SLOW	NONE	FP_VTT_50	
	OUT		U3	☑	34	LVI	3.300		12	SLOW	NONE	FP_VTT_50	
	OUT		P2	☑	34	LVI	3.300		12	SLOW	NONE	FP_VTT_50	
	OUT		U1	☑	34	LVI	3.300		12	SLOW	NONE	FP_VTT_50	
	OUT		R1	☑	34	LVI	3.300		12	SLOW	NONE	FP_VTT_50	