IQ MODULATOR and INTERPOLATION (HDL design)
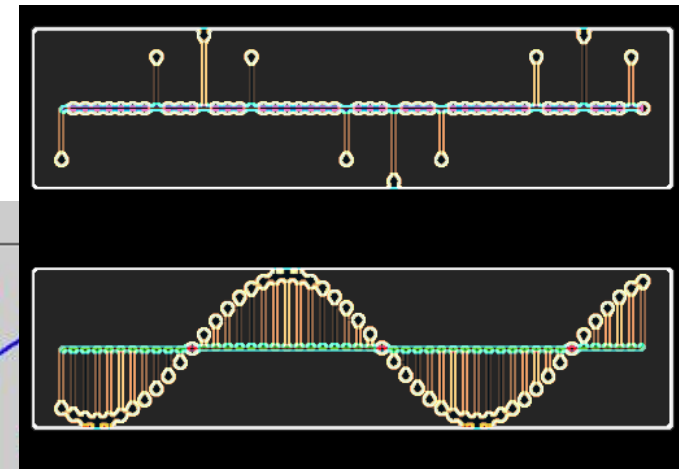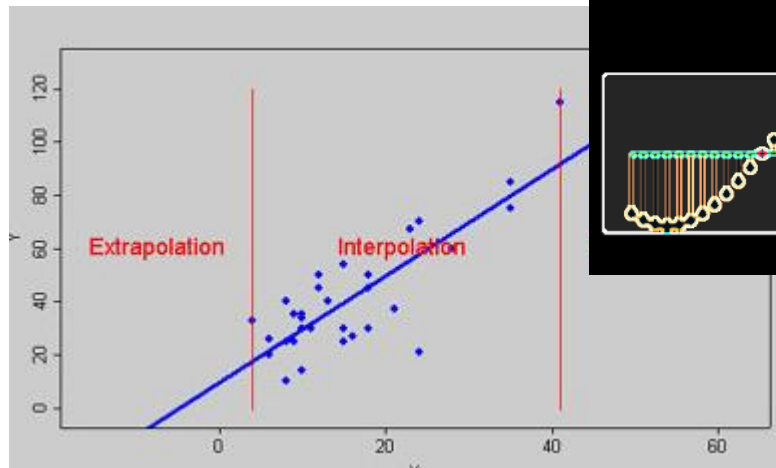
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FPGA/Embedded Linux Developer,
aleksei.rostov@protonmail.com

AGENTA

1. IQ modulator and interpolation filter MATLAB model
2. HDL design and implementation (Verilog) of Interpolation FIR filter and IQ modulator
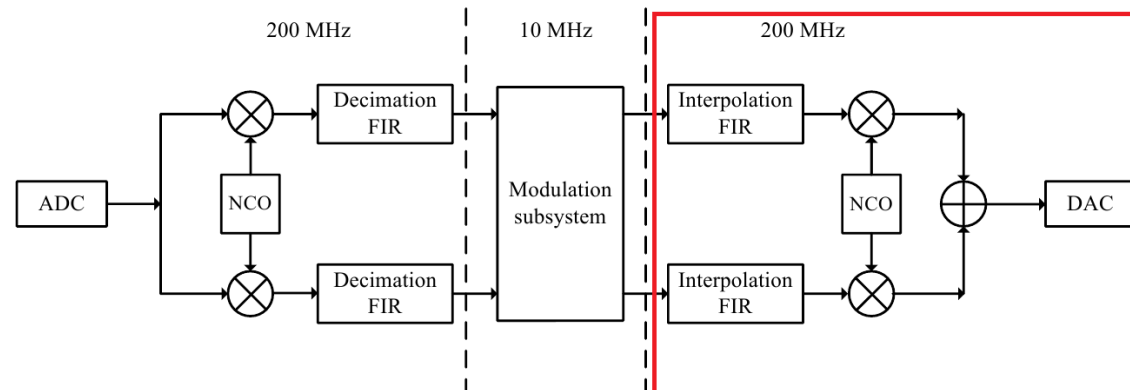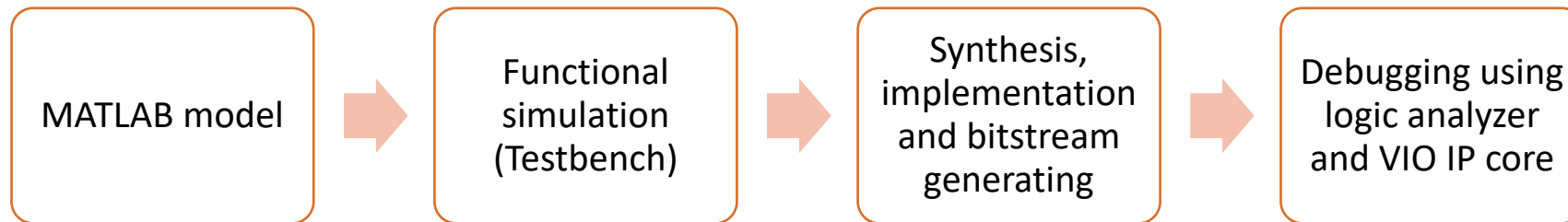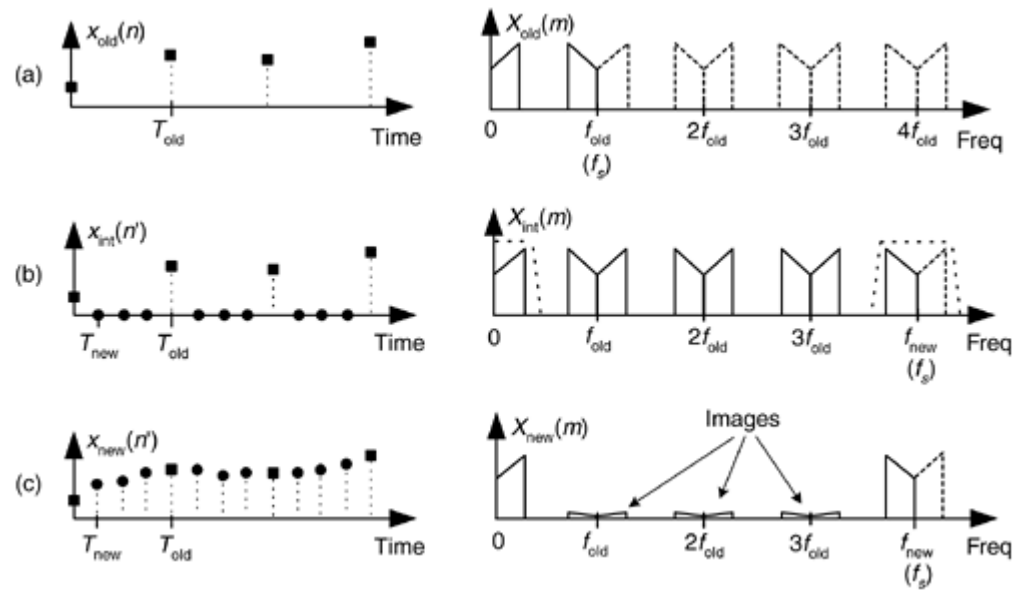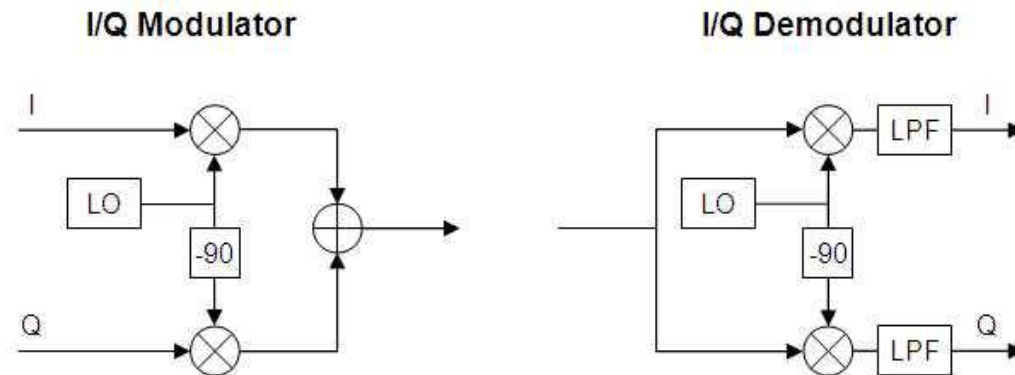
DESIGN FLOW

Рисунок 1 – Система ретрансляции сигнала с подсистемой модуляции

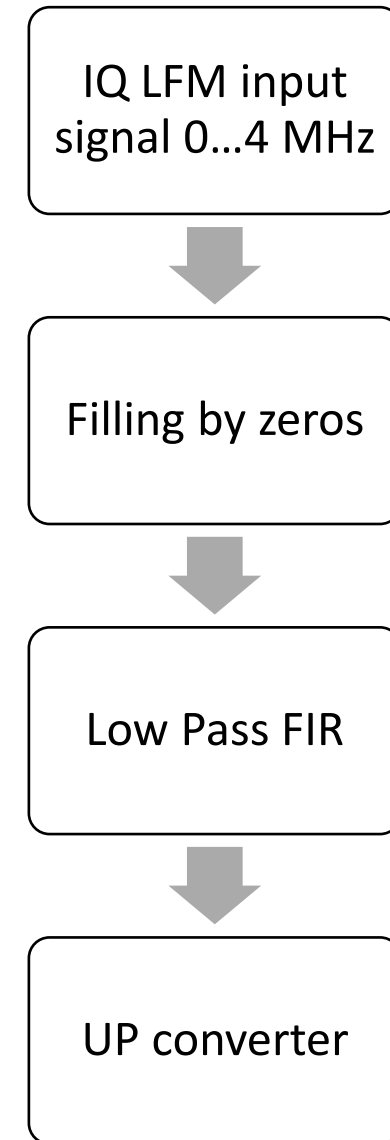aleksei.rostov@protonmail.com

MATLAB model

Interpolation of input signal

IQ modulator and demodulator

Model structure

IQ LFM input signal 0...4 MHz

Filling by zeros

Low Pass FIR

UP converter

Interpolation FIR filter and IQ modulator: hardware design
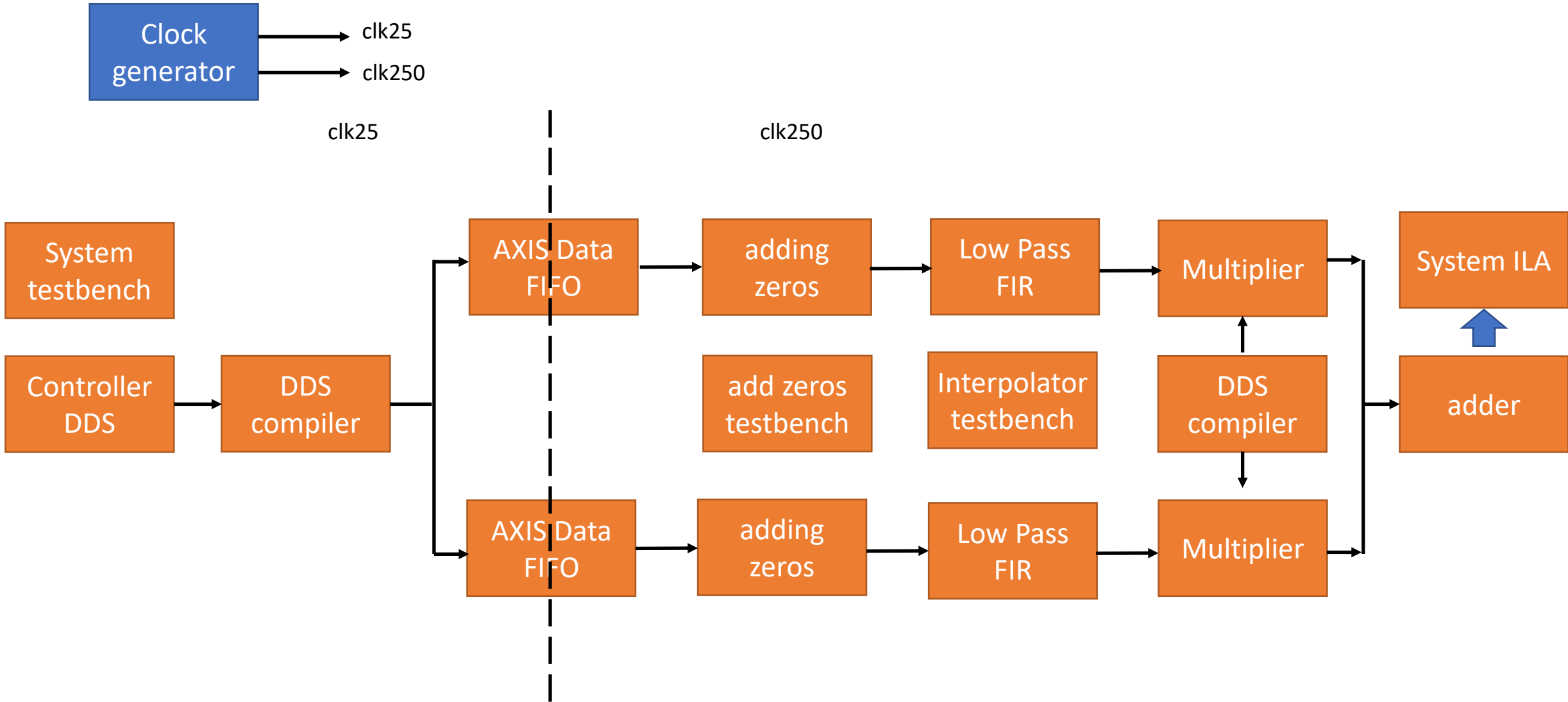
IQ modulator and interpolator by 10

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