IQ DEMODULATOR AND DECIMATION (HDL DESIGN)

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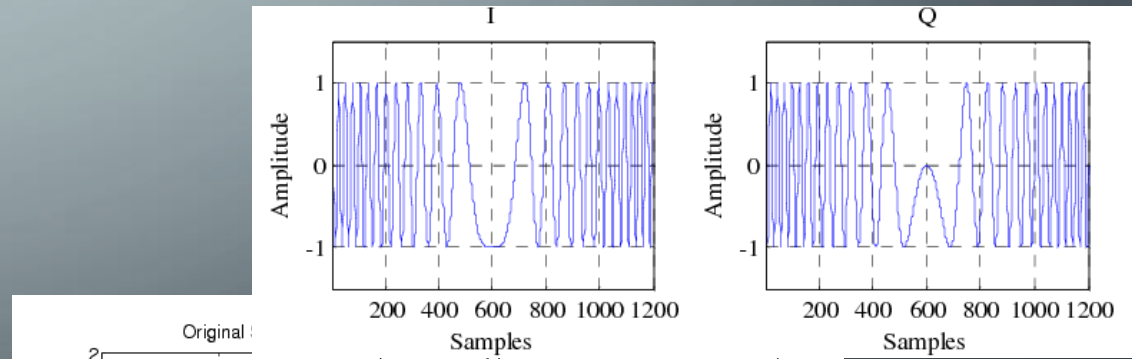

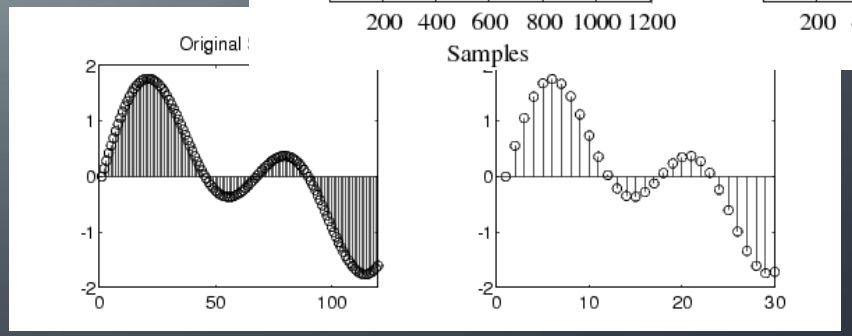

AGENTA

1. IQ demodulator and decimation filter MATLAB model
2. HDL design and implementation (Verilog) of Decimation FIR filter
3. Decimation FIR filter AXIS IP core creation

DESIGN FLOW

MATLAB model → Functional simulation (Testbench) → Synthesis, implementation and bitstream generating → Debugging using logic analyzer and VIO IP core

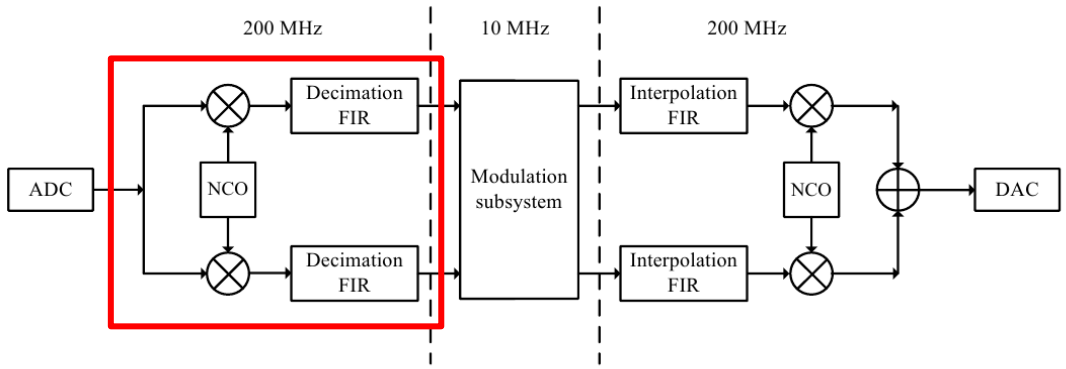

Рисунок 1 – Система ретрансляции сигнала с подсистемой модуляции

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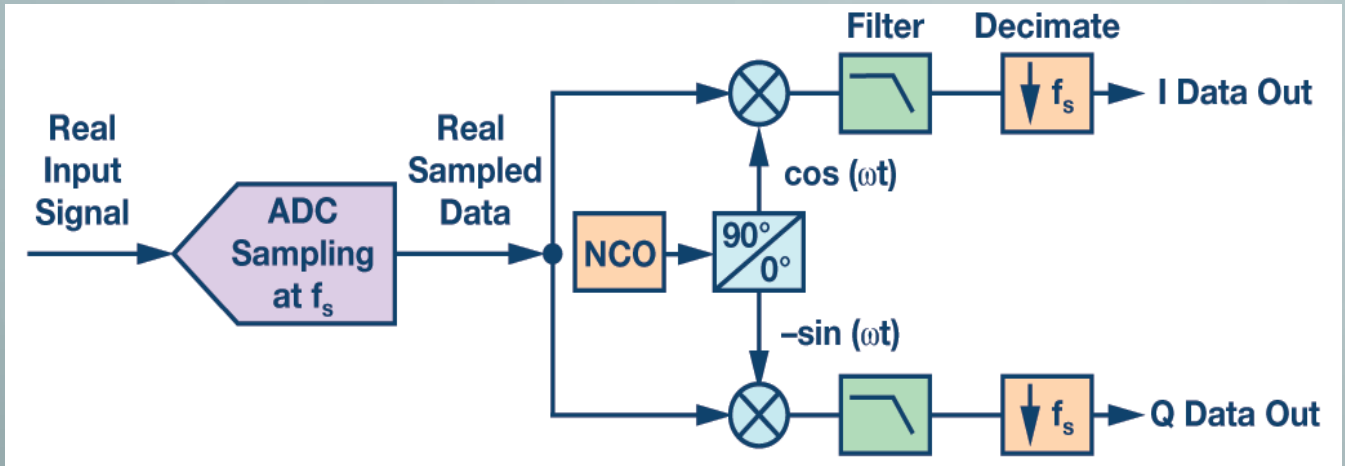
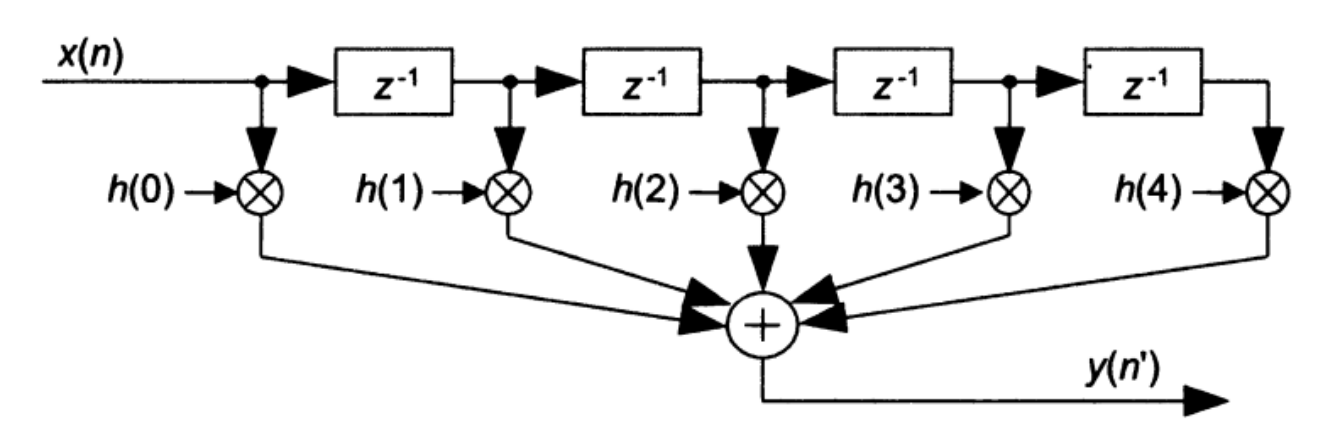
MATLAB model



IQ demodulator with decimation

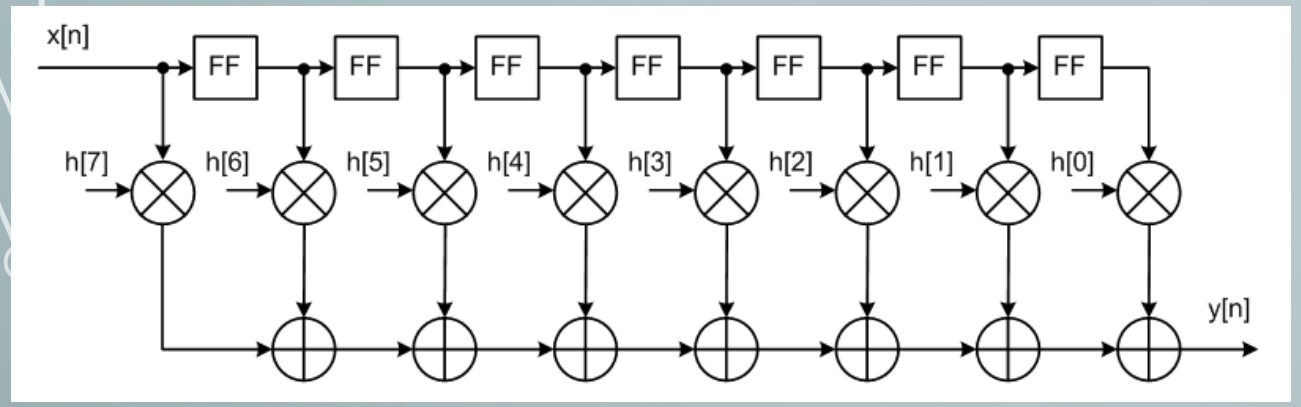


FIR filter with multiplexed output

Model structure

- Real LFM input signal 28…32 MHz
- COS and SIN Multipliers
- Low Pass FIR (anti-aliasing)
- Down sampling

FIR FILTER HARDWARE DESIGN AND IMPLEMENTATION



FIR filter direct form

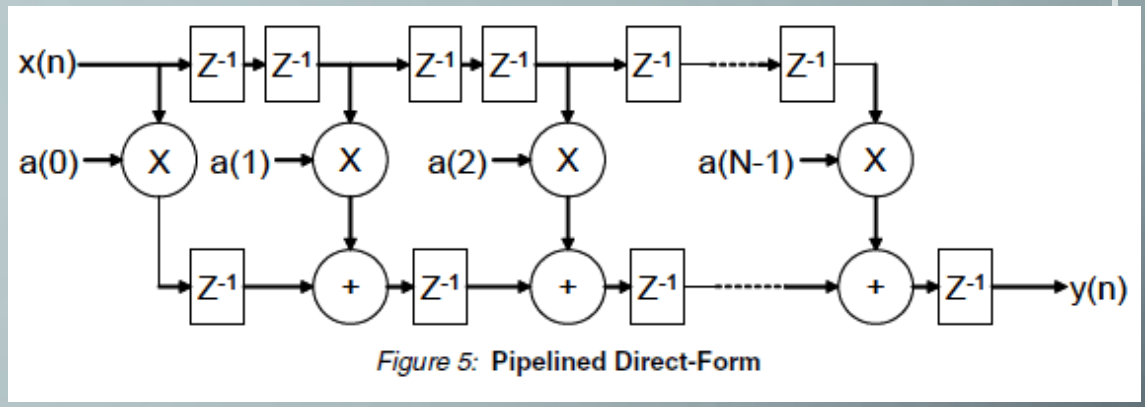
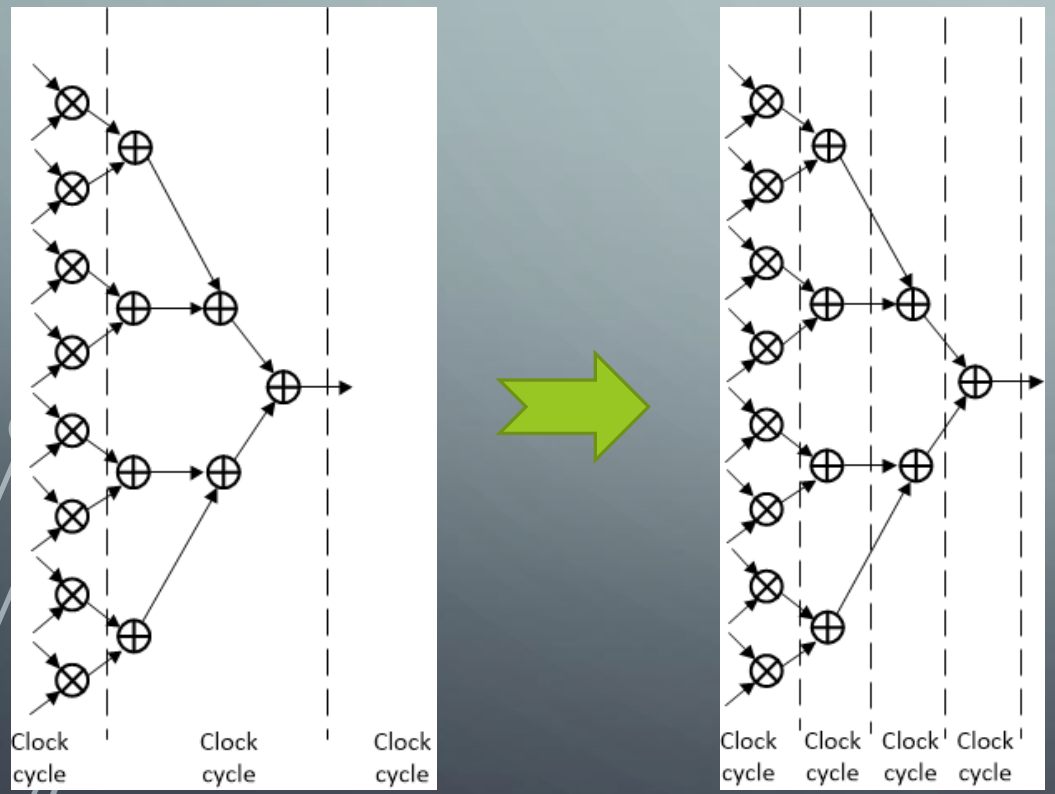
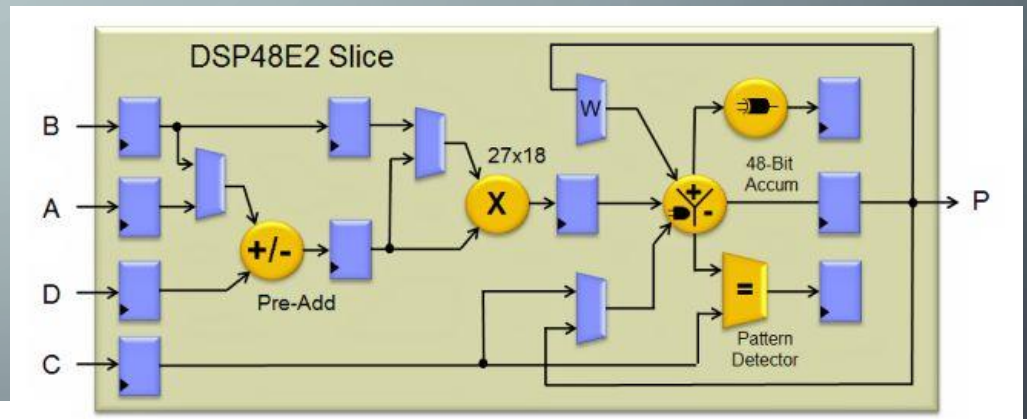


Figure 5: **Pipelined Direct-Form**





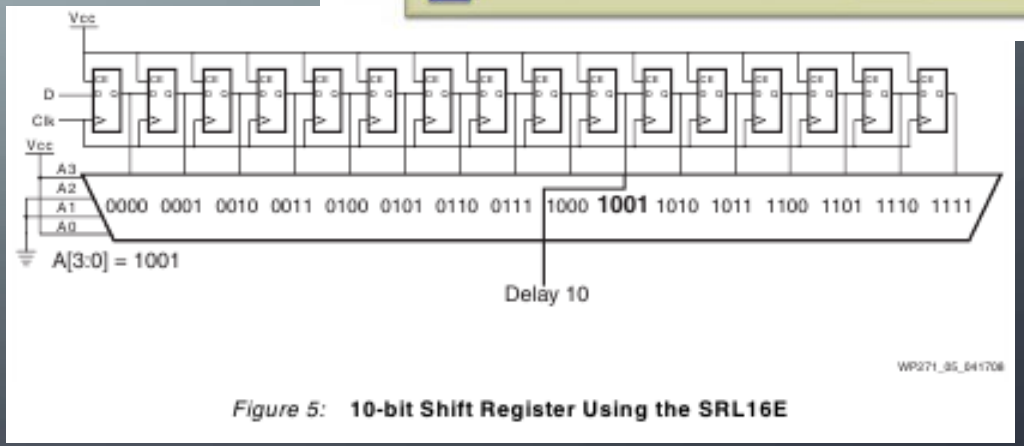
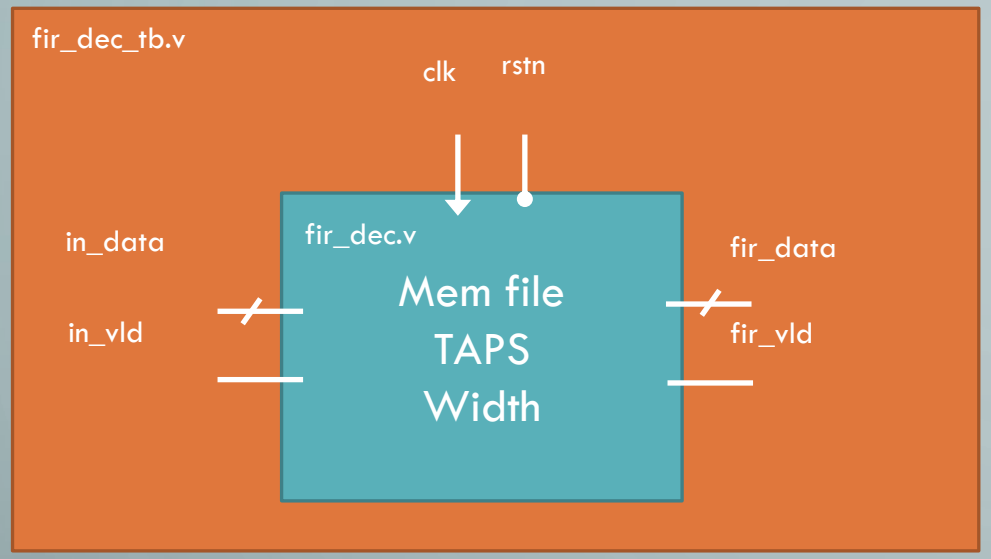
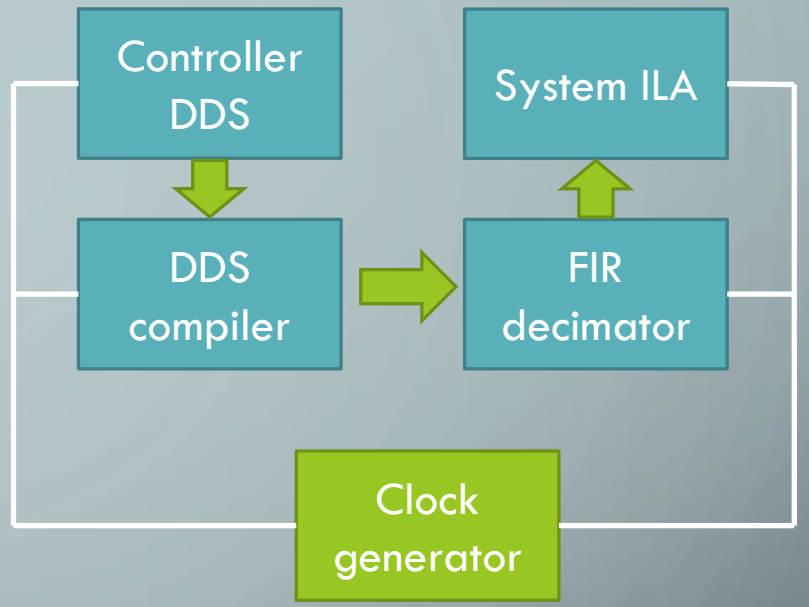


Figure 5: **10-bit Shift Register Using the SRL16E**

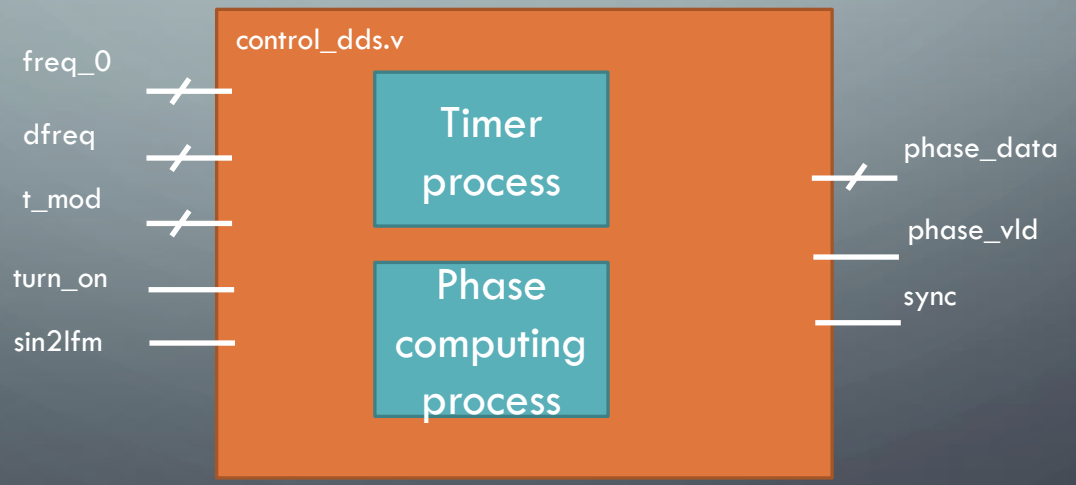
PROJECT MODULES



Modules for functional simulation



Hardware design for FPGA



Controller for DDS

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