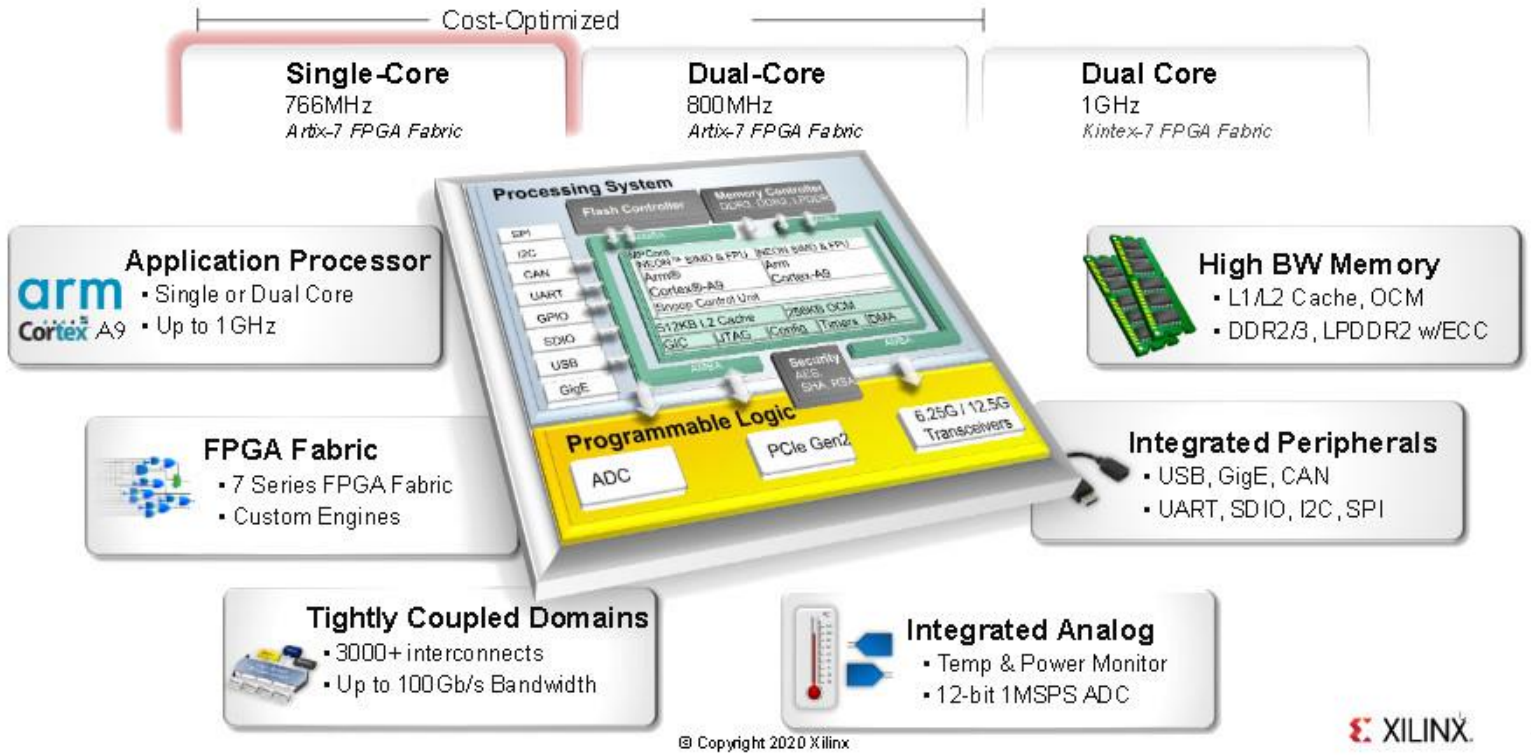
Zynq 7000: Overview, GPIOs, Interrupt Controller



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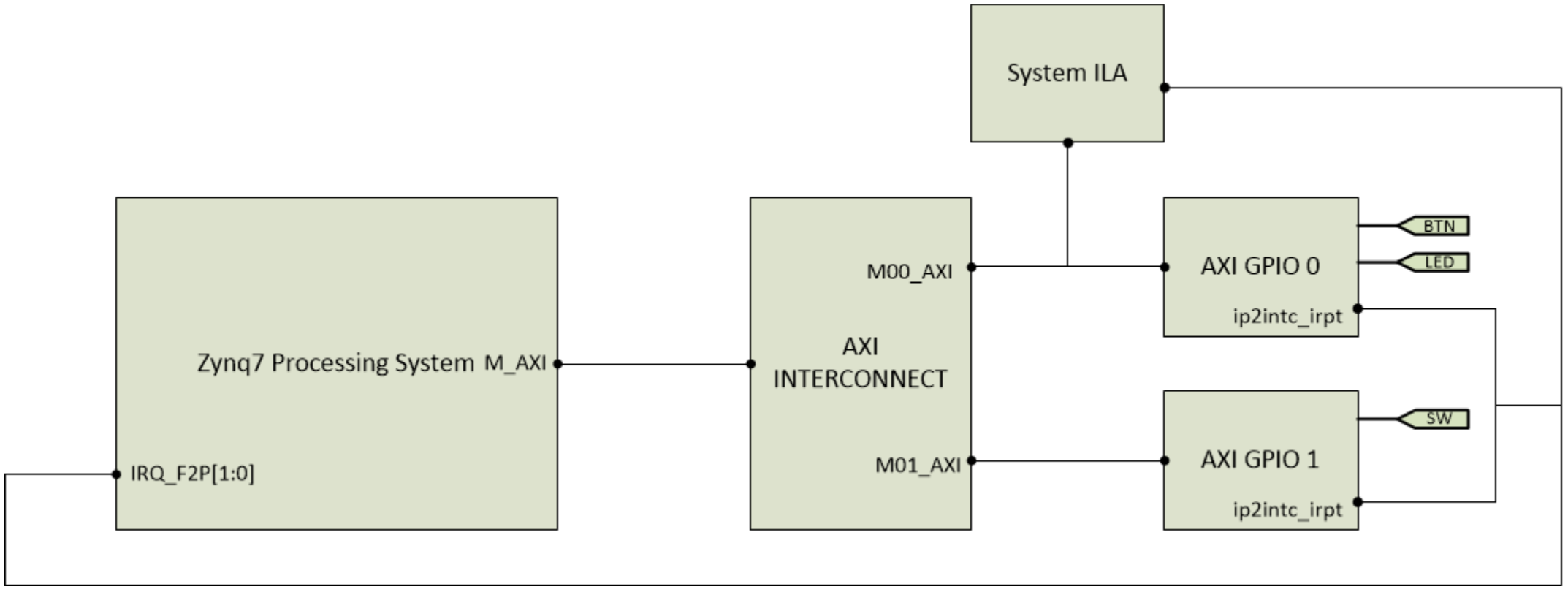
1. Zynq 7000 overview
2. Working with AXI GPIO and Generic Interrupt Controller (GIC)



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AXI GPIO

Table 2-4 shows the AXI GPIO registers and their addresses.

Table 2-4: **Registers**

Address Space Offset[3]	Register Name	Access Type	Default Value	Description
0x0000	GPIO_DATA	R/W	0x0	Channel 1 AXI GPIO Data Register.
0x0004	GPIO_TRI	R/W	0x0	Channel 1 AXI GPIO 3-state Control Register.
0x0008	GPIO2_DATA	R/W	0x0	Channel 2 AXI GPIO Data Register.
0x000C	GPIO2_TRI	R/W	0x0	Channel 2 AXI GPIO 3-state Control.
0x011C	GIER[1]	R/W	0x0	Global Interrupt Enable Register.
0x0128	IP IER[1]	R/W	0x0	IP Interrupt Enable Register (IP IER).
0x0120	IP ISR[1]	R/TOW[2]	0x0	IP Interrupt Status Register.

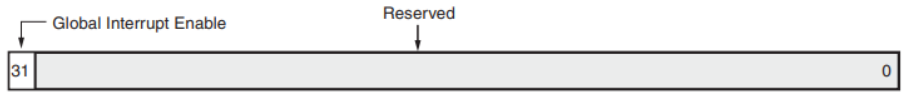
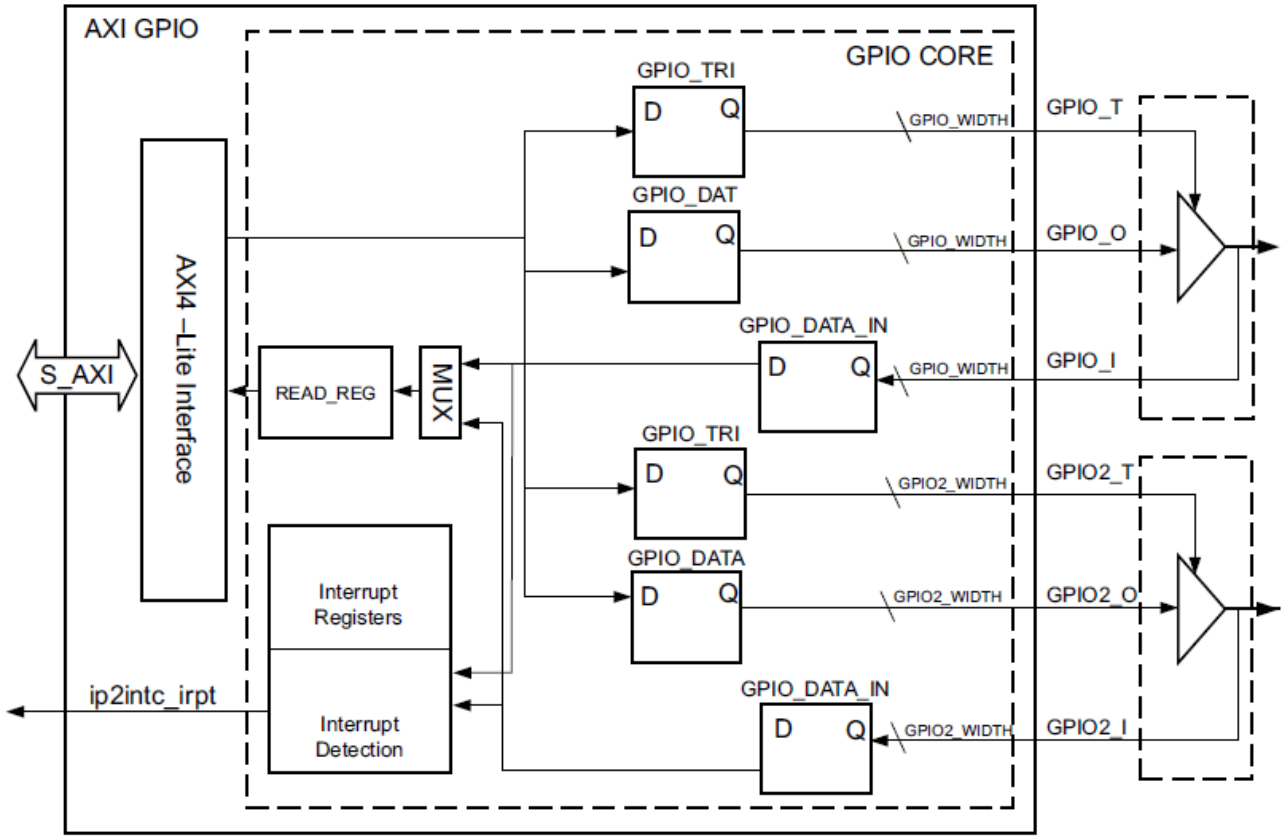


Figure 2-3: **Global Interrupt Enable Register**

Table 2-8: **Global Interrupt Enable Register Description**

Bits	Name	Core Access	Reset Value	Description
31	Global Interrupt Enable	Read/Write	0	Master enable for the device interrupt output to the system interrupt controller: 0 = Disabled 1 = Enabled
30 – 0	Reserved	N/A	0	Reserved. Set to zeros on a read.



AXI GPIO Block Diagram

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AXI GPIO

Figure 2-4: **IP Interrupt Enable and IP Interrupt Status Register**

Table 2-9: **IP Interrupt Enable Register Description**

Bits	Name	Core Access	Reset Value	Description
31–2	Reserved	N/A	0	Reserved. Set to zeros on a read.
1	Channel 2 Interrupt Enable	Read/Write	0	Enable Channel 2 Interrupt. 0 = Disabled (masked) 1 = Enabled
0	Channel 1 Interrupt Enable	Read/Write	0	Enable Channel 1 Interrupt. 0 = Disabled (masked) 1 = Enabled

Table 2-10: **IP Interrupt Status Register Description**

Bits	Name	Core Access	Reset Value	Description
31–2	Reserved	N/A	0	Reserved. Set to zeros on a read.
1	Channel 2 Interrupt Status	Read/TOW(1)	0	Channel 2 Interrupt Status 0 = No Channel 2 input interrupt 1 = Channel 2 input interrupt
0	Channel 1 Interrupt Status	Read/TOW(1)	0	Channel 1 Interrupt Status 0 = No Channel 1 input interrupt 1 = Channel 1 input interrupt

Notes:
1. Toggle-On-Write (TOW) access toggles the status of the bit when a value of 1 is written to the corresponding bit.

Programming Sequence

The following steps are helpful in accessing the AXI GPIO core.

For input ports when the Interrupt is enabled, follow these steps:

1. Configure the port as input by writing the corresponding bit in GPIOx_TRI register with the value of 1.
2. Enable the channel interrupt by setting the corresponding bit in the IP Interrupt Enable Register; also enable the global interrupt, by setting bit 31 of the Global Interrupt Register to 1.
3. When an interrupt is received, read the corresponding bit in the GPIOx_DATA register. Clear the status in the IP Interrupt Status Register by writing the corresponding bit with the value of 1.

For input ports when the Interrupt is not enabled, use the following steps:

1. Configure the port as input by writing the corresponding bit in GPIOx_TRI register with the value of 1.
2. Read the corresponding bit in GPIOx_DATA register.

For output ports, use the following steps:

1. Configure the port as output by writing the corresponding bit in GPIOx_TRI register with a value of 0.
2. Write the corresponding bit in GPIOx_DATA register.

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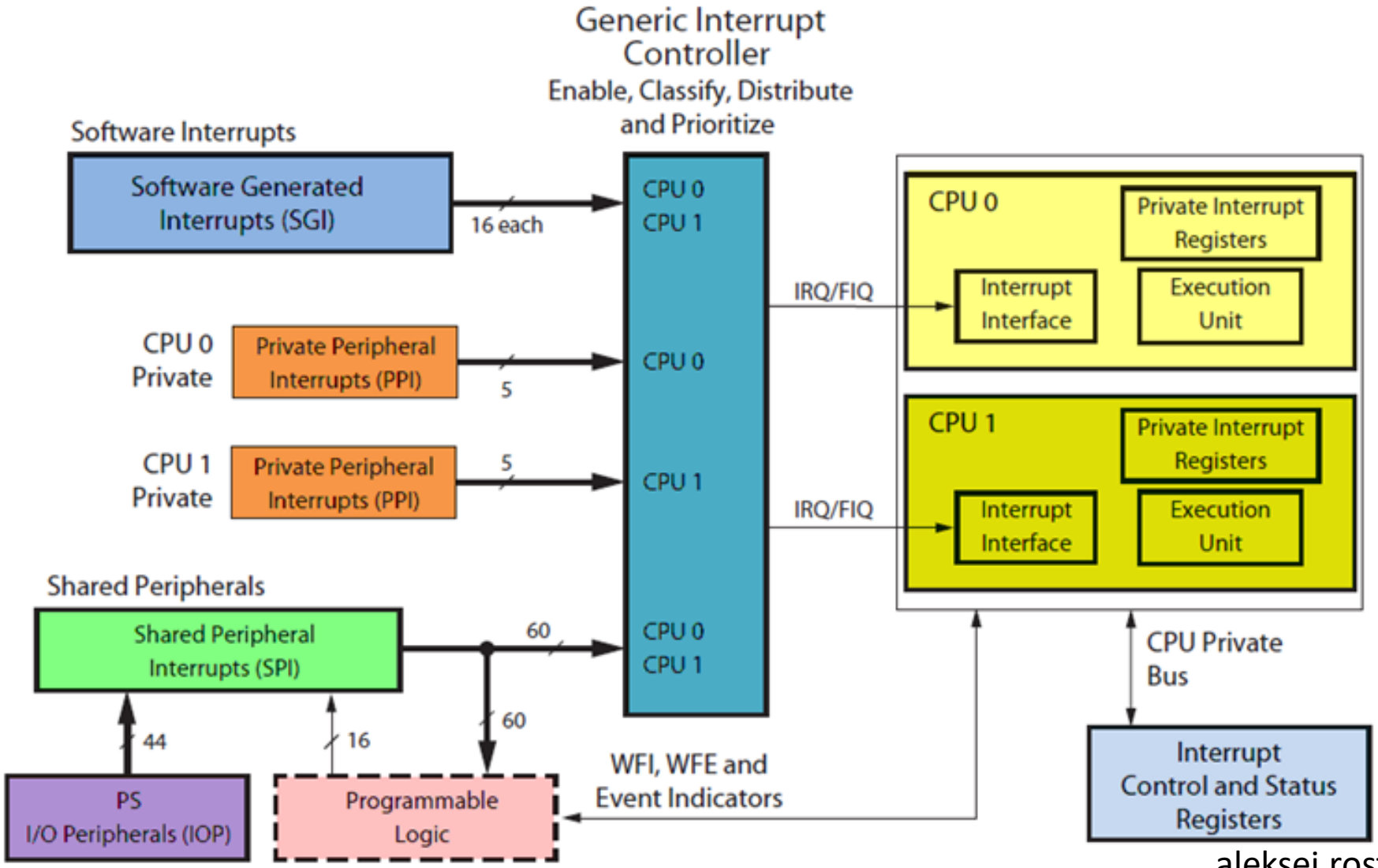
Interrupt Controller



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