

Scheduling Algorithms System

Submitted by:

Mohamed Ahmed Rabea

Mostafa Wael Hussien

Ahmed Sayed Mohamed

Mohamed Yousef Helmy

Ali Abdelmenaim Mohamed

Submitted To:

Dr. Marwa Yousef

Eng. Mohamed Abdelmegid

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Overview

The **Process Scheduler Simulator for Multiprocessor Systems** is a comprehensive tool designed to emulate and evaluate different scheduling policies within a multiprocessor environment. The primary objective of this project is to offer a versatile platform that allows users to simulate, analyze, and compare the performance of distinct scheduling algorithms, including First-Come, First-Served (FCFS), Shortest Job First (SJF), Shortest Time-to-Completion First (STCF), Round Robin (RR), Priority, Multilevel Feedback Queue (MLFQ), and Stride scheduling.

Objectives:

1. **Scheduling Policy Evaluation:** The simulator facilitates the examination and comparison of diverse scheduling policies to comprehend their behavior in a multi-core processor setting.
2. **Performance Assessment:** It measures and reports crucial performance metrics like turnaround time.
3. **User Interaction and Customization:** The tool offers an intuitive user interface that enables users to interact with the system, input custom processes, modify parameters, and select scheduling policies for simulation.
4. **Visualization and Analysis:** Through Gantt charts, the simulator illustrates the execution and allocation of processes across processors, aiding in the assessment of scheduling policies' efficiency.

Significance:

Understanding the nuances of scheduling policies in a multiprocessor environment is pivotal in optimizing system performance, resource utilization, and responsiveness. This simulator provides an invaluable platform for students, researchers, and system designers to explore.

Scope

The **Process Scheduler Simulator for Multiprocessor Systems** encompasses a wide array of functionalities and capabilities, providing a comprehensive platform for simulating and analyzing various scheduling policies in a multiprocessor environment.

Scheduling Policies Covered:

1. **First-Come, First-Served (FCFS):** Processes are executed in the order they arrive.
2. **Shortest Job First (SJF):** Prioritizes the shortest burst time processes.
3. **Shortest Time-to-Completion First (STCF):** Selects processes based on remaining time to completion.
4. **Round Robin (RR):** Time-sliced scheduling for fair execution among processes.
5. **Priority Scheduling:** Assigns priority levels to processes for execution.
6. **Multilevel Feedback Queue (MLFQ):** Implements multiple queues with varied priorities.
7. **Stride Scheduling:** Utilizes proportional allocation of CPU time based on stride values.

Types of Simulated Processes:

The simulator accommodates a diverse range of processes, comprising both CPU and I/O-bound tasks. Each process is defined by a series of CPU bursts and I/O bursts, mimicking real-world workloads.

User Interaction Capabilities:

Users have an interactive interface that allows for:

- Inputting custom processes with specific burst times and characteristics.
- Modifying system parameters, like quantum size (for RR), Tickets (for Stride).
- Selecting and initiating simulations for different scheduling policies.
- Visualizing results through Gantt charts.

System Architecture

The **Process Scheduler Simulator** exhibits a modular architecture comprising crucial components for emulating a multiprocessor system and implementing various scheduling policies.

Components:

1. Process Representation:

- Defined as a structure encompassing essential attributes like process name, arrival time, phases (execution or I/O), priority, state, tickets, and performance metrics.
- Employs a vector-based representation for each process, allowing flexible management and manipulation during simulation.

2. Scheduler Module:

- Core component responsible for executing the Scheduling policies.
- Houses algorithms and logic for scheduling decisions based on the chosen policy.
- Integrates with process queues, handles context switching, and manages process states.

3. Multiprocessor Environment:

- Simulates a four-processor system, utilizing an array-based representation to manage processor states and process assignments.
- Facilitates parallel execution of processes based on availability and task requirements.

4. User Interface:

- Interaction primarily via the command-line interface for simplicity.
- Provides user prompts to input the number of processes and generates sample processes with randomized attributes within a file and the system takes the input from the file itself.
- Initiates the Scheduler chosen policy and displays the output, including processor-wise execution snapshots.

High-Level Workflow:

1. Initialization and Input:

- Accepts user input for the number of processes or generates sample processes with randomized attributes from the file.
- Initializes process structures and computes the necessary values for each process based on the provided phases and arrival times.

2. Scheduler Execution:

- Utilizes a loop-based mechanism to simulate processor allocation and execution of processes based on Scheduling.
- Manages CPU bursts, I/O phases, context switches, and process completions.

3. Output and Analysis:

- Generates processor-wise execution snapshots using a two-dimensional vector (**output**) to represent the progress of each process over time.
- Calculates process statistics such as turnaround time and completion time for each process.

Scalability and Extension:

The current architecture is tailored specifically for the Scheduling policies within a four-processor environment. Extending this simulator to accommodate additional scheduling policies or processors would require structural modifications and enhanced user interaction capabilities.

Data Structures

1. Process Structure (struct process):

- Attributes: **process_name**, **arrive_time**, **turn_around_time**, **complete_time**, **time_consumed**, **n_phases**, **phase_idx**, **last_processor**, **phases**, **state**, **priority**, **current_burst_time**, **pass_value**, **stride**, **tickets**, **qunta**.
- Represents an individual process with its specific characteristics, including name, arrival time, phases, state, and performance metrics.
- Utilizes a vector to store phase details (execution time and type - CPU burst or I/O burst).

2. Output Matrix (vector<vector<string>> output):

- A two-dimensional vector used to visualize the execution progress of processes on each processor over time.
- Provides a snapshot of process execution in a tabular format, aiding in creating Gantt charts or processor-wise execution logs.

3. Scheduler Data Structures:

- **queue<int>** for handling waiting processes during execution.
- Arrays (**processor[]**, **WillGoToTheQ[]**) to manage process allocation to processors based on the Stride Scheduling policy.

Algorithms Implementation

1. Process Initialization and Input Generation:

- **Mechanism:** Generates or accepts input for the number of processes, their attributes, and phases from a file.
- **Working Principle:**
 - Generates sample processes with randomized attributes for testing and simulation purposes.
 - Accepts user input for process attributes like arrival time, phases (CPU bursts or I/O), and other relevant parameters.
 - Computes necessary values for each process based on provided phase details for each scheduling policy.
- **Integration into Simulator:**
 - Initializes process structures and sets up the simulation environment with sample or user-defined input from a file.
 - Enables the execution of scheduling algorithms by creating a pool of processes for scheduling.

2. SJF Algorithm Implementation

1. Initialization:

- Sorts the processes based on their burst times using the **comparedByBurst** comparison function.
- Initializes variables like **finished_processes**, **processor[]**, **WillGoToTheQ[]**, and a priority queue **waiting** to manage waiting processes.

2. Scheduler Execution:

- Loops through each time unit to simulate the scheduler's behavior.
- Checks for arriving processes at each time unit and allocates available processors to the shortest job among the arrived processes.
- Queues processes that arrive but cannot be immediately executed due to all processors being busy.

- Executes processes on the processors based on their burst times, allowing the shortest job to run on the available processor.
- Tracks the execution progress in the **output** matrix for visual representation.
- Handles completion of phases, updating states, and marking processes as finished when all phases are executed.

3. Processor Allocation and Execution:

- Assigns available processors to the shortest job among the arrived processes.
- Manages the execution of processes based on their burst times, ensuring completion of phases, and marking processes as finished accordingly.

4. IO_handler_bypq Function:

- Handles I/O operations for processes in the priority queue **waiting**, similar to the IO handler function used in other scheduling policies.

5. Completion Check:

- Checks if all processes have finished execution. If so, generates the final output and exits the simulation.

3. FCFS Algorithm Implementation

1. Initialization:

- Initializes variables such as **finished_processes**, **processor[]**, **WillGoToTheQ[]**, and a queue **waiting** to manage waiting processes.

2. Scheduler Execution:

- Loops through each time unit to simulate the scheduler's behavior.
- Checks for arriving processes at each time unit and allocates available processors to the arriving processes based on the FCFS principle.
- Queues processes that arrive but cannot be immediately executed due to all processors being busy.

3. Processor Allocation and Execution:

- Allocates processors to arriving processes in the order of their arrival.
- Manages the execution of processes on processors, allowing them to execute their phases according to their burst times.
- Tracks the execution progress in the **output** matrix for visual representation.

4. IO_handler Function:

- Handles I/O operations for processes in the waiting queue, similar to other scheduling policies.

5. Completion Check:

- Checks if all processes have finished execution. If so, generates the final output and exits the simulation.

4. STCF (Shortest Time-to-Completion First) Algorithm Implementation

1. Initialization:

- Initializes variables like **finished_processes**, **processor[]**, **WillGoToTheQ[]**, and a priority queue **waiting** to manage waiting processes based on their burst times.

2. Scheduler Execution:

- Loops through each time unit to simulate the scheduler's behavior.
- Checks for arriving processes at each time unit and allocates available processors based on the STCF principle, favoring processes with shorter burst times.

3. Processor Allocation and Execution:

- Allocates processors to arriving processes based on their burst times.
- Manages the execution of processes on processors, allowing them to execute their phases according to their burst times.
- Tracks the execution progress in the **output** matrix for visualization.

4. **IO_handler_bypq Function:**

- Handles I/O operations for processes in the waiting queue, similar to other scheduling policies.

5. **Completion Check:**

- Checks if all processes have finished execution. If so, generates the final output and exits the simulation.

5. **Round Robin Algorithm Implementation**

1. **Initialization:**

- Initializes variables like **my_queue** (queue to store processes), **finished_processes**, **processor[]**, **WillGoToTheQ[]**, and **time_slice** (quantum time) for process execution.

2. **Scheduler Execution:**

- Simulates the scheduler's behavior by iterating over each time unit.
- Checks for arriving processes and assigns them to available processors or enqueues them in the **my_queue**.

3. **Processor Allocation and Execution:**

- Allocates processors to arriving processes or those waiting in the queue.
- Executes processes for a fixed time slice (**time_slice**) or until the process finishes its current burst time, whichever occurs first.
- Tracks the progress of process execution in the **output** matrix for visualization.

4. **Match Preferences and IO Handling:**

- Matches preferences for processor allocation.
- Handles I/O operations for processes.

5. **Completion Check:**

- Checks if all processes have finished execution. If so, generates the final output and exits the simulation.

6. Multi-Level Feedback Queue (MLFQ) Algorithm Implementation:

1. Initialization:

- Initializes variables like **my_queue[]** (queues for multiple priority levels), **finished_processes**, **processor[]**, **WillGoToTheQ[]**, **time_slice**, and other related parameters.
- Resets the processors and queues.

2. Scheduler Execution:

- Iterates over each time unit.
- Assigns arriving processes to available processors or to appropriate queues based on priority levels (**my_queue**).

3. Processor Allocation and Execution:

- Executes processes in processors based on their priority levels.
- Tracks the progress of process execution in the **output** matrix for visualization.
- Handles time quantum expiry and phase completion for processes, moving them to the appropriate queue or updating their priorities.

4. Queue Management and Priority Handling:

- Manages queues by shifting processes between different priority queues based on their quantum usage and priorities.
- Handles processor allocation considering process priorities and available queues.

5. Match Preferences and IO Handling:

- Matches preferences for processor allocation.
- Handles I/O operations for processes.

6. Priority Adjustment:

- Adjusts the priority of processes after a certain number of time units (**time_to_moveup**), likely to maintain fairness or adjust scheduling parameters dynamically.

7. Completion Check:

- Checks if all processes have finished execution. If so, generates the final output and exits the simulation.

7. Stride Scheduling Algorithm Implementation:

1. Initialization:

- Initializes variables such as **waiting**, **q**, **finished_processes**, **WillGoToTheQ**, **processor[]**, and **i**.

2. Scheduler Execution:

- Executes a loop representing each time unit.
- Sorts the processes based on their arrival time or their pass value and fills the queue accordingly.
- Assigns arriving processes to available processors or to the waiting queue (**waiting**).

3. Processor Allocation and Execution:

- Executes processes in processors based on their arrival times or pass values.
- Tracks the progress of process execution in the **output** matrix for visualization.
- Updates the pass value for each process based on its stride.
- Handles completion of processes after their time slice or phase completion.

4. Queue Management and Preference Handling:

- Manages the waiting queue and assigns processes to processors based on their states and availability.
- Matches preferences for processor allocation.

5. IO Handling and Completion Check:

- Handles I/O operations for processes.
- Checks if all processes have completed execution. If so, generates the final output and exits the simulation.

6. Completion Check:

- Checks if all processes have finished execution. If so, generates the final output and exits the simulation.

8. Priority Scheduling Algorithm:

1. Initialization:

- Sorts the processes based on priority.
- Initializes variables like **finished_processes**, **processor[]**, **WillGoToTheQ[]**, and queues.

2. Scheduler Execution:

- Executes a loop representing each time unit.
- Assigns arriving processes to available processors based on their priority.
- Allocates processes that arrive when no processors are available to a waiting queue.

3. Processor Allocation and Execution:

- Executes processes in processors based on their priority.
- Tracks the progress of process execution in the **output** matrix for visualization.
- Handles the completion of processes after their time slice or phase completion.

4. Queue Management and Preference Handling:

- Manages the waiting queue and assigns processes to processors based on their states and availability.
- Matches preferences for processor allocation using the **WillGoToTheQ** array.

5. IO Handling and Completion Check:

- Handles I/O operations for processes.
- Checks if all processes have completed execution. If so, generates the final output and exits the simulation.

Code Samples:

Round Robin

7
A 4 0
3 EXE
2 I/O
20 EXE
1 I/O

B 3 0
6 EXE
2 I/O
1 EXE

C 3 0
10 EXE
2 I/O
10 EXE

D 3 0
6 EXE
3 I/O
6 EXE

E 3 0
6 EXE
3 I/O
6 EXE

F 3 0
6 EXE
3 I/O
6 EXE

X 3 2
1 EXE
1 I/O
10 EXE

```
processor 1 : A | 0 A | 1 A | 2 E | 3 E | 4 E | 5 E | 6 E | 7 E | 8 B | 9 X | 10 X | 11 X | 12 X | 13 X | 14 X | 15 X | 16 X | 17 X | 18 X | 19 A | 20 A | 21 A | 22 A | 23 A | 24
A | 25 A | 26 A | 27 A | 28 A
t | 25 t | 26 t | 27 t | 28 t

processor 2 : B | 0 B | 1 B | 2 B | 3 B | 4 B | 5 F | 6 F | 7 F | 8 F | 9 F | 10 F | 11 C | 12 C | 13 C | 14 C | 15 C | 16 C | 17 C | 18 C | 19 C | 20 C | 21 t | 22 t | 23 t | 24
t | 25 t | 26 t | 27 t | 28 t

processor 3 : C | 0 C | 1 C | 2 C | 3 C | 4 C | 5 C | 6 C | 7 C | 8 C | 9 D | 10 D | 11 D | 12 D | 13 D | 14 D | 15 E | 16 E | 17 E | 18 E | 19 E | 20 E | 21 t | 22 t | 23 t | 24
t | 25 t | 26 t | 27 t | 28 t

processor 4 : D | 0 D | 1 D | 2 D | 3 D | 4 D | 5 X | 6 A | 7 A | 8 A | 9 A | 10 A | 11 A | 12 A | 13 A | 14 A | 15 A | 16 F | 17 F | 18 F | 19 F | 20 F | 21 F | 22 t | 23 t | 24
t | 25 t | 26 t | 27 t | 28 t

-----processes-----
A arrived at 0 it's turn around time = 29
B arrived at 0 it's turn around time = 9
C arrived at 0 it's turn around time = 21
D arrived at 0 it's turn around time = 15
E arrived at 0 it's turn around time = 21
F arrived at 0 it's turn around time = 22
X arrived at 2 it's turn around time = 17

average turn around time = 19.1429
```

SJF

7
A 4 0
3 EXE
2 I/O
20 EXE
1 I/O

B 3 0
6 EXE
2 I/O
1 EXE

C 3 0
10 EXE
2 I/O
10 EXE

D 3 0
6 EXE
3 I/O
6 EXE

E 3 0
6 EXE
3 I/O
6 EXE

F 3 0
6 EXE
3 I/O
6 EXE

X 3 2
1 EXE
1 I/O
10 EXE

```
processor 1 : A | 0 A | 1 A | 2 X | 3 F | 4 F | 5 F | 6 F | 7 F | 8 F | 9 B | 10 D | 11 D | 12 D | 13 D | 14 D | 15 D | 16 t | 17 C | 18 C | 19 C | 20 C | 21 C | 22 C | 23 C | 24 C | 25 C | 26 C  
processor 2 : B | 0 B | 1 B | 2 B | 3 B | 4 B | 5 C | 6 C | 7 C | 8 C | 9 C | 10 C | 11 C | 12 C | 13 C | 14 C | 15 E | 16 E | 17 E | 18 E | 19 E | 20 E | 21 t | 22 t | 23 t | 24 t | 25 t | 26 t  
processor 3 : D | 0 D | 1 D | 2 D | 3 D | 4 D | 5 X | 6 X | 7 X | 8 X | 9 X | 10 X | 11 X | 12 X | 13 X | 14 X | 15 F | 16 F | 17 F | 18 F | 19 F | 20 F | 21 t | 22 t | 23 t | 24 t | 25 t | 26 t  
processor 4 : E | 0 E | 1 E | 2 E | 3 E | 4 E | 5 A | 6 A | 7 A | 8 A | 9 A | 10 A | 11 A | 12 A | 13 A | 14 A | 15 A | 16 A | 17 A | 18 A | 19 A | 20 A | 21 A | 22 A | 23 A | 24 A | 25 t | 26 t  
-----processes-----  
A arrived at 0 it's turn around time = 25  
B arrived at 0 it's turn around time = 10  
D arrived at 0 it's turn around time = 16  
E arrived at 0 it's turn around time = 21  
F arrived at 0 it's turn around time = 21  
C arrived at 0 it's turn around time = 27  
X arrived at 2 it's turn around time = 13  
-----  
average turn around time = 19
```

FCFS

7
A 4 0
3 EXE
2 I/O
20 EXE
1 I/O

B 3 0
6 EXE
2 I/O
1 EXE

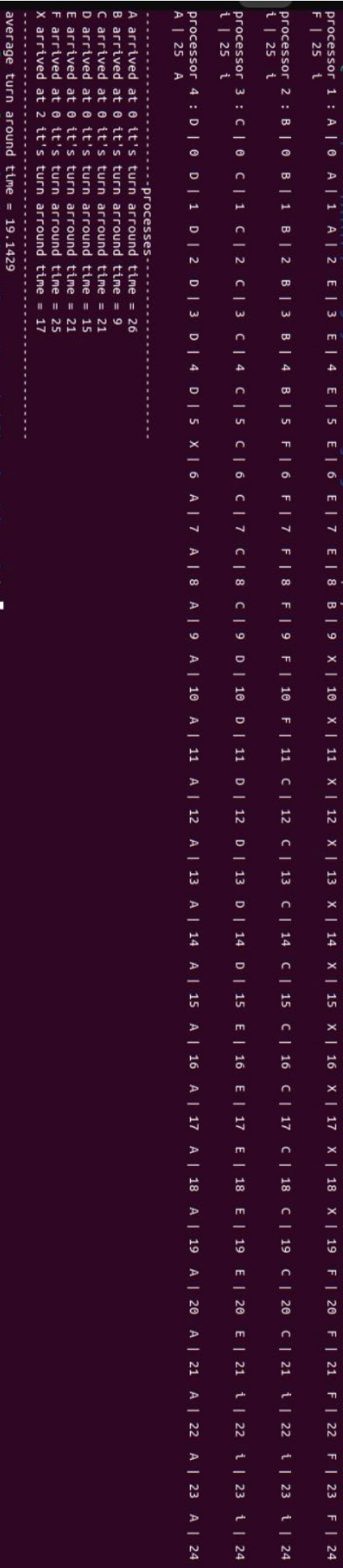
C 3 0
10 EXE
2 I/O
10 EXE

D 3 0
6 EXE
3 I/O
6 EXE

E 3 0
6 EXE
3 I/O
6 EXE

F 3 0
6 EXE
3 I/O
6 EXE

X 3 2
1 EXE
1 I/O
10 EXE



MLFQ

7
A 4 0
3 EXE
2 I/O
20 EXE
1 I/O

B 3 0
6 EXE
2 I/O
1 EXE

C 3 0
10 EXE
2 I/O
10 EXE

D 3 0
6 EXE
3 I/O
6 EXE

E 3 0
6 EXE
3 I/O
6 EXE

F 3 0
6 EXE
3 I/O
6 EXE

X 3 2
1 EXE
1 I/O
10 EXE

```
processor 1 : A | 0 A | 1 X | 2 C | 3 C | 4 C | 5 C | 6 X | 7 X | 8 X | 9 X | 10 X | 11 X | 12 X | 13 X | 14 X | 15 F | 16 F | 17 F | 18 F | 19 t | 20 t | 21 t | 22 t | 23 t | 24
t | 25 t | 26 t | 27 t
processor 2 : B | 0 B | 1 B | 2 B | 3 B | 4 B | 5 F | 6 F | 7 F | 8 F | 9 B | 10 A | 11 A | 12 F | 13 F | 14 D | 15 D | 16 D | 17 D | 18 A | 19 A | 20 A | 21 A | 22 A | 23 A | 24
A | 25 A | 26 A | 27 A
processor 3 : C | 0 C | 1 E | 2 E | 3 X | 4 A | 5 E | 6 E | 7 E | 8 E | 9 C | 10 C | 11 C | 12 E | 13 E | 14 C | 15 E | 16 E | 17 E | 18 E | 19 t | 20 t | 21 t | 22 t | 23 t | 24
t | 25 t | 26 t | 27 t
processor 4 : D | 0 D | 1 F | 2 F | 3 D | 4 D | 5 D | 6 D | 7 A | 8 A | 9 A | 10 D | 11 D | 12 A | 13 A | 14 A | 15 A | 16 A | 17 C | 18 C | 19 C | 20 C | 21 C | 22 C | 23 C | 24
C | 25 C | 26 C | 27 t
-----processes-----
A arrived at 0 it's turn around time = 28
B arrived at 0 it's turn around time = 10
C arrived at 0 it's turn around time = 27
D arrived at 0 it's turn around time = 18
E arrived at 0 it's turn around time = 19
F arrived at 0 it's turn around time = 19
X arrived at 2 it's turn around time = 13
-----
average turn around time = 19.1429
```

STRIDE

7
A 4 0
3 EXE
2 I/O
20 EXE
1 I/O

B 3 0
6 EXE
2 I/O
1 EXE

C 3 0
10 EXE
2 I/O
10 EXE

D 3 0
6 EXE
3 I/O
6 EXE

E 3 0
6 EXE
3 I/O
6 EXE

F 3 0
6 EXE
3 I/O
6 EXE

X 3 2
1 EXE
1 I/O
10 EXE

```
processor 1 : A | 0 A | 1 A | 2 E | 3 E | 4 E | 5 E | 6 E | 7 E | 8 X | 9 X | 10 X | 11 X | 12 X | 13 X | 14 X | 15 X | 16 X | 17 X | 18 C | 19 C | 20 C | 21 C | 22 C | 23 C | 24 C | 25 C | 26 C | 27 C  
t | 25 t | 26 t | 27 t  
processor 2 : B | 0 B | 1 B | 2 B | 3 B | 4 B | 5 F | 6 F | 7 F | 8 F | 9 F | 10 F | 11 E | 12 E | 13 E | 14 E | 15 E | 16 E | 17 B | 18 t | 19 t | 20 t | 21 t | 22 t | 23 t | 24 t | 25 t | 26 t | 27 t  
processor 3 : C | 0 C | 1 C | 2 C | 3 C | 4 C | 5 C | 6 C | 7 C | 8 C | 9 D | 10 D | 11 D | 12 D | 13 D | 14 D | 15 F | 16 F | 17 F | 18 F | 19 F | 20 F | 21 t | 22 t | 23 t | 24 t | 25 t | 26 t | 27 t  
processor 4 : D | 0 D | 1 D | 2 D | 3 D | 4 D | 5 X | 6 A | 7 A | 8 A | 9 A | 10 A | 11 A | 12 A | 13 A | 14 A | 15 A | 16 A | 17 A | 18 A | 19 A | 20 A | 21 A | 22 A | 23 A | 24 A | 25 A | 26 t | 27 t  
-----processes-----  
A arrived at 0 tt's turn around time = 26  
B arrived at 0 tt's turn around time = 18  
C arrived at 0 tt's turn around time = 28  
D arrived at 0 tt's turn around time = 15  
E arrived at 0 tt's turn around time = 17  
F arrived at 0 tt's turn around time = 21  
X arrived at 2 tt's turn around time = 16  
-----  
average turn around time = 20.1429
```

STCF

7
A 4 0
3 EXE
2 I/O
20 EXE
1 I/O

B 3 0
6 EXE
2 I/O
1 EXE

C 3 0
10 EXE
2 I/O
10 EXE

D 3 0
6 EXE
3 I/O
6 EXE

E 3 0
6 EXE
3 I/O
6 EXE

F 3 0
6 EXE
3 I/O
6 EXE

X 3 2
1 EXE
1 I/O
10 EXE

```
processor 1 : A | 0 | A | 1 | A | 2 | F | 3 | F | 4 | F | 5 | F | 6 | F | 7 | F | 8 | X | 9 | X | 10 | X | 11 | X | 12 | X | 13 | X | 14 | X | 15 | t | 16 | t | 17 | A | 18 | A | 19 | A | 20 | A | 21 | A | 22 | A | 23 | A | 24
A | 25 | A | 26 | A | 27 | A | 28 | A | 29 | A | 30 | A | 31 | A | 32 | A | 33 | t

processor 2 : D | 0 | D | 1 | D | 2 | D | 3 | D | 4 | D | 5 | X | 6 | X | 7 | X | 8 | D | 9 | D | 10 | D | 11 | D | 12 | D | 13 | D | 14 | F | 15 | F | 16 | F | 17 | F | 18 | F | 19 | F | 20 | t | 21 | t | 22 | t | 23 | t | 24
t | 25 | t | 26 | t | 27 | t | 28 | t | 29 | t | 30 | t | 31 | t | 32 | t | 33 | t

processor 3 : B | 0 | B | 1 | B | 2 | B | 3 | B | 4 | B | 5 | C | 6 | C | 7 | B | 8 | A | 9 | C | 10 | C | 11 | C | 12 | C | 13 | C | 14 | C | 15 | A | 16 | A | 17 | C | 18 | C | 19 | C | 20 | C | 21 | C | 22 | C | 23 | C | 24
C | 25 | C | 26 | C | 27 | t | 28 | t | 29 | t | 30 | t | 31 | t | 32 | t | 33 | t

processor 4 : E | 0 | E | 1 | X | 2 | E | 3 | E | 4 | E | 5 | E | 6 | A | 7 | C | 8 | C | 9 | E | 10 | E | 11 | E | 12 | E | 13 | E | 14 | E | 15 | t | 16 | t | 17 | t | 18 | t | 19 | t | 20 | t | 21 | t | 22 | t | 23 | t | 24
t | 25 | t | 26 | t | 27 | t | 28 | t | 29 | t | 30 | t | 31 | t | 32 | t | 33 | t

-----Processes-----
A arrived at 0 it's turn around time = 34
B arrived at 0 it's turn around time = 8
D arrived at 0 it's turn around time = 14
E arrived at 0 it's turn around time = 15
F arrived at 0 it's turn around time = 20
X arrived at 2 it's turn around time = 27
average turn around time = 18.7143
```

Priority

7
A 4 0
3 EXE
2 I/O
20 EXE
1 I/O

B 3 0
6 EXE
2 I/O
1 EXE

C 3 0
10 EXE
2 I/O
10 EXE

D 3 0
6 EXE
3 I/O
6 EXE

E 3 0
6 EXE
3 I/O
6 EXE

F 3 0
6 EXE
3 I/O
6 EXE

X 3 2
1 EXE
1 I/O
10 EXE

```
processor 1 : E | 0 | E | 1 | E | 2 | E | 3 | E | 4 | E | 5 | A | 6 | A | 7 | A | 8 | E | 9 | E | 10 | E | 11 | E | 12 | E | 13 | E | 14 | A | 15 | A | 16 | A | 17 | A | 18 | A | 19 | A | 20 | A | 21 | A | 22 | A | 23 | A | 24
A | 25 | A | 26 | A | 27 | A | 28 | A | 29 | A | 30 | A | 31 | A | 32 | A | 33 | A
processor 2 : C | 0 | C | 1 | C | 2 | C | 3 | C | 4 | C | 5 | C | 6 | C | 7 | C | 8 | C | 9 | X | 10 | X | 11 | X | 12 | X | 13 | X | 14 | X | 15 | X | 16 | X | 17 | X | 18 | X | 19 | t | 20 | t | 21 | t | 22 | t | 23 | t | 24
t | 25 | t | 26 | t | 27 | t | 28 | t | 29 | t | 30 | t | 31 | t | 32 | t | 33 | t
processor 3 : B | 0 | B | 1 | B | 2 | B | 3 | B | 4 | B | 5 | F | 6 | F | 7 | F | 8 | F | 9 | F | 10 | F | 11 | C | 12 | C | 13 | C | 14 | C | 15 | C | 16 | C | 17 | C | 18 | C | 19 | C | 20 | C | 21 | t | 22 | t | 23 | t | 24
t | 25 | t | 26 | t | 27 | t | 28 | t | 29 | t | 30 | t | 31 | t | 32 | t | 33 | t
processor 4 : D | 0 | D | 1 | D | 2 | D | 3 | D | 4 | D | 5 | X | 6 | t | 7 | B | 8 | D | 9 | D | 10 | D | 11 | D | 12 | D | 13 | D | 14 | F | 15 | F | 16 | F | 17 | F | 18 | F | 19 | F | 20 | t | 21 | t | 22 | t | 23 | t | 24
t | 25 | t | 26 | t | 27 | t | 28 | t | 29 | t | 30 | t | 31 | t | 32 | t | 33 | t
-----Processes-----
E arrived at 0 it's turn around time = 14
C arrived at 0 it's turn around time = 21
B arrived at 0 it's turn around time = 8
D arrived at 0 it's turn around time = 14
A arrived at 0 it's turn around time = 34
F arrived at 2 it's turn around time = 20
X arrived at 2 it's turn around time = 17
-----
average turn around time = 18.2857
```

