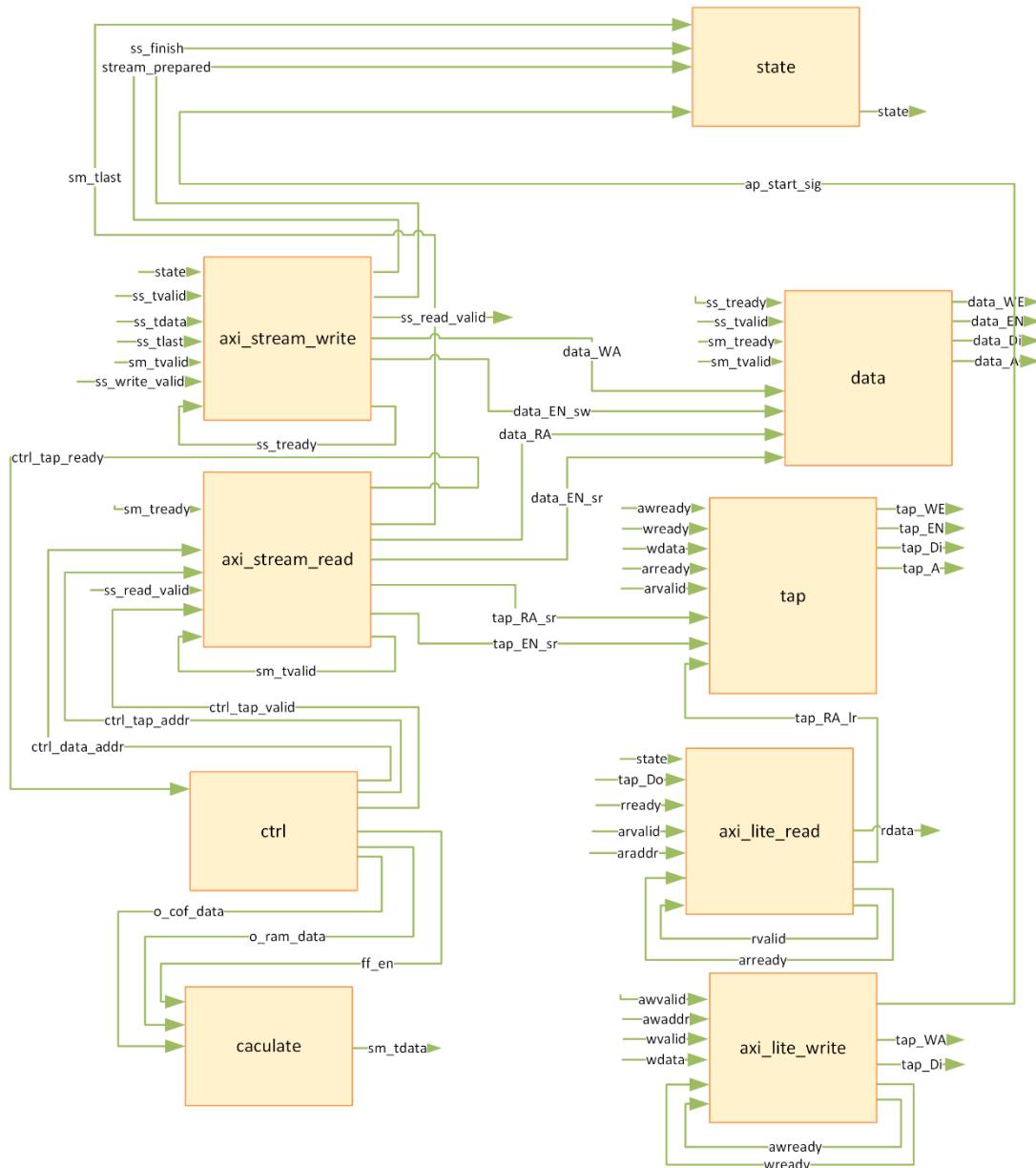


SOC LAB#3 Report

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Name: 曹榮恩

1. Block Diagram

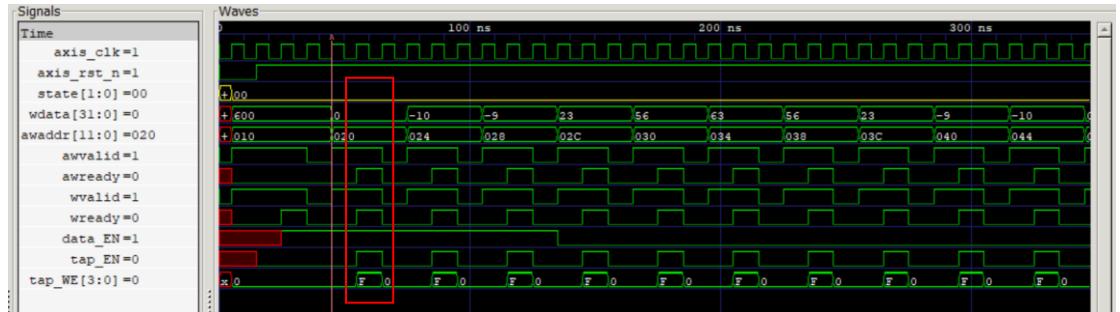


2. Describe operation

- How to receive data-in and tap parameters and place into SRAM

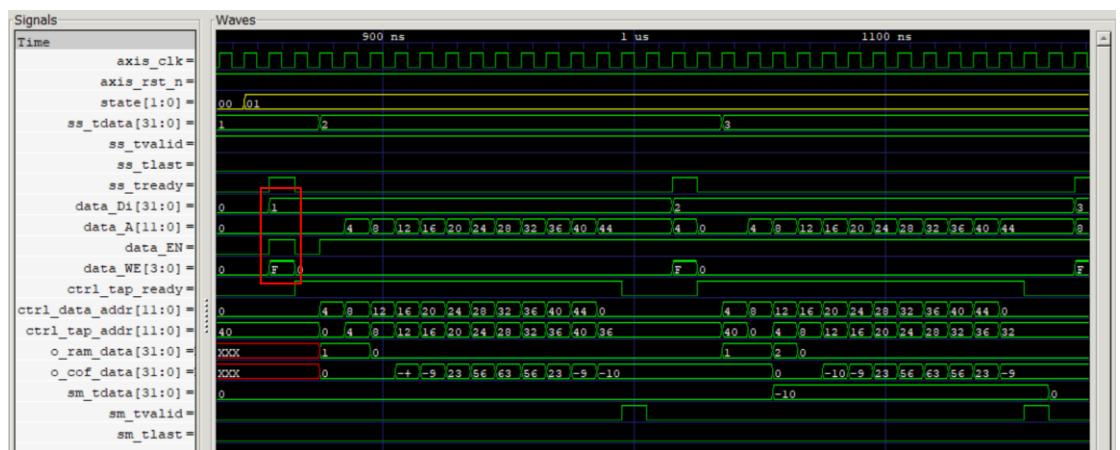
當 tap_EN 的訊號等於 1 以及 tap_WE 訊號等於 4'hF 時，

會將 wdata 寫進去 awaddr (會做 shift) 的位置



當 data_EN 訊號等於 1 以及 data_WE 訊號等於 4'hF 時，會

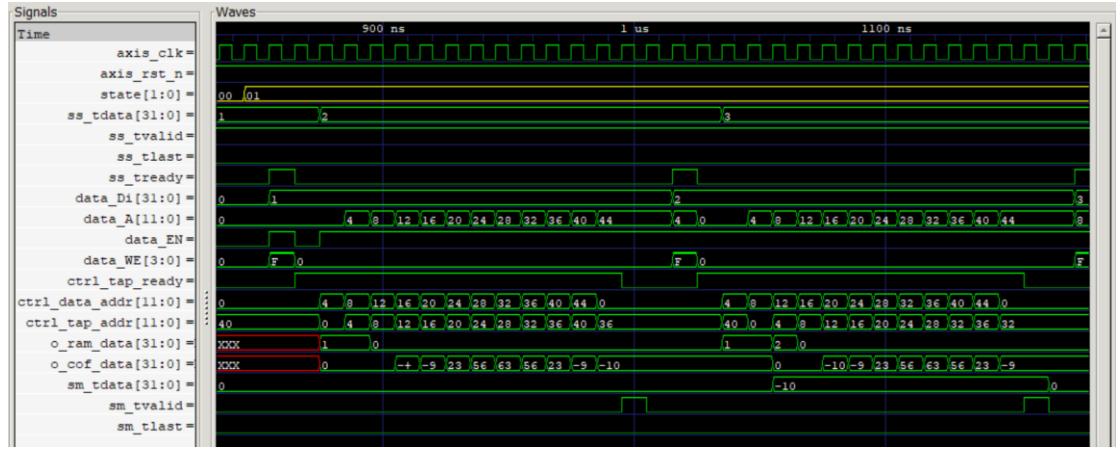
將 ss_tdata 寫進去 data_A 的位置。



- How to access shiftram and tapRAM to do computation

Ctrl module 會輸出對應的 tap_addr 與 data_addr，之後從

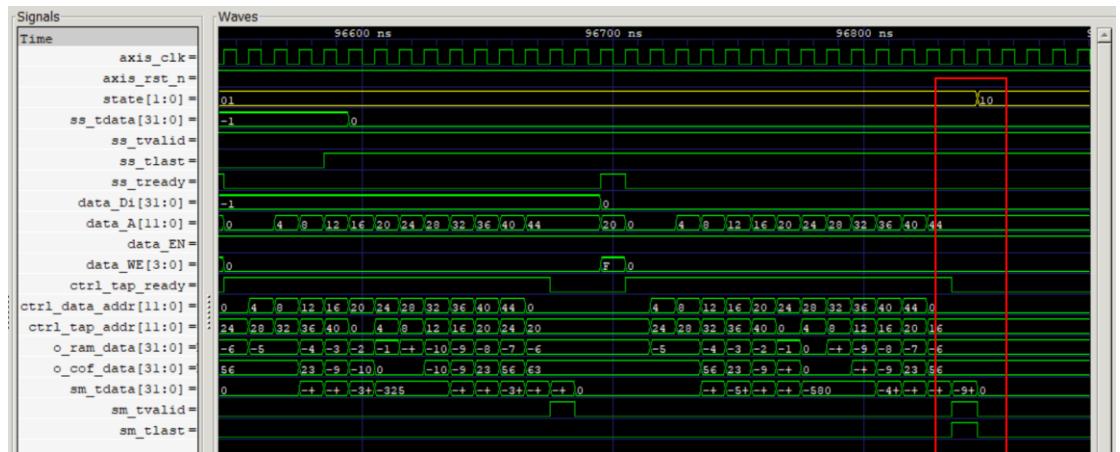
RAM 讀出數值。



- How ap_done is generated.

當 ss_tlast 訊號等於 1 以及 sm_tlast 訊號等於 1 後，state

狀態改為 `ap_done(2'b10)`。



3. Resource usage

Tcl Console	Messages	Log	Reports	Design Runs	Timing	?	—	□													
Search:																					
Name	Constraints	Status	WNS	TNS	WHS	THS	WBSS	TPWS	Total Power	Failed Routes	Methodology	RQA Score	QoR Suggestions	LUT	FF	BRAM	URAM	DSP	Start	Elapsed	Run Strategy
synth_1	consts_1	Synthesis Out-of-date												285	310	0	0	3	10/18/23, 20:05 PM	00:01:32	Vivado Synthesis Defaults
impl_1	consts_1	Not started																			Vivado Implementation Defaults

4. Timing Report

Operation system : Linux

Priod : 15ns

Tco min : 0.01

Tco_max : 0.03

Tsu : 0.01

Thd : 0.03

Trce_dly_min : 0.01

Trce_dly_max : 0.03

Setup worst slack : 3.586 , 如果 Period=12ns 則是 0.586

```

Max Delay Paths
-----
Slack (MET) : 3.586ns (required time - arrival time)
  Source: ctrl_tap/ffen_r_reg/C
    (rising edge-triggered cell FDRE clocked by axis_clk {rise@0.000ns
fall@7.500ns period=15.000ns})
  Destination: sm_tdata_r_reg[29]/D
    (rising edge-triggered cell FDRE clocked by axis_clk {rise@0.000ns
fall@7.500ns period=15.000ns})
Path Group: axis_clk
Path Type: Setup (Max at Slow Process Corner)
Requirement: 15.000ns (axis_clk rise@15.000ns - axis_clk rise@0.000ns)
Data Path Delay: 11.309ns (logic 8.452ns (74.734%) route 2.857ns (25.266%))
Logic Levels: 10 (CARRY4=5 DSP48E1=2 LUT2=2 LUT3=1)
Clock Path Skew: -0.145ns (DCD - SCD + CPR)
  Destination Clock Delay (DCD): 2.128ns = ( 17.128 - 15.000 )
  Source Clock Delay (SCD): 2.456ns
  Clock Pessimism Removal (CPR): 0.184ns
Clock Uncertainty: 0.035ns ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
  Total System Jitter (TSJ): 0.071ns
  Total Input Jitter (TIJ): 0.000ns
  Discrete Jitter (DJ): 0.000ns
  Phase Error (PE): 0.000ns

Location      Delay type      Incr(ns)  Path(ns)   Netlist Resource(s)
-----+-----+-----+-----+-----+-----+
(clock axis_clk rise edge)          0.000    0.000 r
                                      0.000    0.000 r axis_clk (IN)
net (fo=0)                      0.000    0.000 r axis_clk
                                  r axis_clk_IBUF_inst/I
IBUF (Prop_ibuf_I_0)            0.972    0.972 r axis_clk_IBUF_inst/O
net (fo=1, unplaced)           0.800    1.771 r axis_clk_IBUF
                                  r axis_clk_IBUF_BUFG_inst/I
BUFG (Prop_bufg_I_0)           0.101    1.872 r axis_clk_IBUF_BUFG_inst/O
net (fo=310, unplaced)          0.584    2.456 r ctrl_tap/axis_clk_IBUF_BUFG
FDRE                           r ctrl_tap/ffen_r_reg/C
-----+-----+-----+-----+-----+-----+
FDRE (Prop_fdre_C_Q)           0.478    2.934 r ctrl_tap/ffen_r_reg/Q
net (fo=129, unplaced)          0.576    3.510 r ctrl_tap/ffen
                                  r ctrl_tap/sm_tdata_r1_0_i_1/I1
LUT3 (Prop_lut3_I1_0)          0.295    3.805 r ctrl_tap/sm_tdata_r1_0_i_1/O
net (fo=1, unplaced)           0.800    4.605 r o_ram_data[16]
                                  r sm_tdata_r1_0/A[16]
DSP48E1 (Prop_dsp48e1_A[16]_PCOUT[47]) 4.036    8.641 r sm_tdata_r1_0/PCOUT[47]
net (fo=1, unplaced)           0.055    8.696 r sm_tdata_r1_0_n_106
                                  r sm_tdata_r1_0/PIN[47]
DSP48E1 (Prop_dsp48e1_PCIN[47]_P[0]) 1.518    10.214 r sm_tdata_r1_1/P[0]
net (fo=2, unplaced)           0.800    11.014 r sm_tdata_r1_1_n_105
                                  r sm_tdata_r19_i_9/I0
LUT2 (Prop_lut2_I0_0)           0.124    11.138 r sm_tdata_r19_i_9/0
net (fo=1, unplaced)           0.000    11.138 r sm_tdata_r19_i_9_n_0
                                  r sm_tdata_r19_i_6/S[1]
CARRY4 (Prop_carry4_S[1]_CO[3])  0.533    11.671 r sm_tdata_r19_i_6/CO[3]
net (fo=1, unplaced)           0.009    11.680 r sm_tdata_r19_i_6_n_0
                                  r sm_tdata_r19_i_6/CI
CARRY4 (Prop_carry4_CI_CO[3])  0.117    11.797 r sm_tdata_r19_i_6/CO[3]
net (fo=1, unplaced)           0.000    11.797 r sm_tdata_r19_i_6_n_0
                                  r sm_tdata_r19_i_6/CI
CARRY4 (Prop_carry4_CI_O[3])   0.331    12.128 r sm_tdata_r19_i_6_n_0
net (fo=1, unplaced)           0.618    12.746 r sm_tdata_r19_i_6_n_4
                                  r sm_tdata_r19_i_2/I1
LUT2 (Prop_lut2_I1_0)           0.307    13.053 r sm_tdata_r19_i_2/0
net (fo=1, unplaced)           0.000    13.053 r sm_tdata_r19_i_2_n_0
                                  r sm_tdata_r19_i_1/S[3]
CARRY4 (Prop_carry4_S[3]_CO[3]) 0.376    13.429 r sm_tdata_r19_i_1/CO[3]
net (fo=1, unplaced)           0.000    13.429 r sm_tdata_r19_i_1_n_0
                                  r sm_tdata_r19_i_2/CI
CARRY4 (Prop_carry4_CI_O[1])   0.337    13.766 r sm_tdata_r19_i_2/0[1]
net (fo=1, unplaced)           0.000    13.766 r sm_tdata_r19_i_2_n_6
                                  r sm_tdata_r19_i_2/D
FDRE                           r sm_tdata_r19_D
-----+-----+-----+-----+-----+-----+
(clock axis_clk rise edge)          15.000   15.000 r
                                      0.000   15.000 r axis_clk (IN)
net (fo=0)                      0.000   15.000 r axis_clk
                                  r axis_clk_IBUF_inst/I
IBUF (Prop_ibuf_I_0)            0.838   15.838 r axis_clk_IBUF_inst/O
net (fo=1, unplaced)           0.760   16.598 r axis_clk_IBUF
                                  r axis_clk_IBUF_BUFG_inst/I
BUFG (Prop_bufg_I_0)           0.091   16.689 r axis_clk_IBUF_BUFG_inst/O
net (fo=310, unplaced)          0.439   17.128 r axis_clk_IBUF_BUFG
FDRE                           r sm_tdata_r19_D
clock pessimism                0.184    17.311
clock uncertainty              -0.035   17.276
FDRE (Setup_fdre_C_D)          0.076    17.352 r sm_tdata_r19_D
-----+-----+-----+-----+-----+-----+
required time                  17.352
arrival time                   -13.766
-----+-----+-----+-----+-----+-----+
slack                          3.586

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Slack (MET) : 3.592ns (required time - arrival time)
 Source: ctrl_tap/ffen_r_reg/C
 (rising edge-triggered cell FDRE clocked by axis_clk {rise@0.000ns}
fall@7.500ns period=15.000ns}
 Destination: sm_tdata_r_reg[31]/D
 (rising edge-triggered cell FDRE clocked by axis_clk {rise@0.000ns}
fall@7.500ns period=15.000ns}
 Path Group: axis_clk
 Path Type: Setup (Max at Slow Process Corner)
 Requirement: 15.000ns (axis_clk rise@15.000ns - axis_clk rise@0.000ns)
 Data Path Delay: 11.303ns (logic 8.446ns (74.721%) route 2.857ns (25.279%))
 Logic Levels: 10 (CARRY4=5 DSP48E1=2 LUT2=2 LUT3=1)
 Clock Path Skew: -0.145ns (DCD - SCD + CPR)
 Destination Clock Delay (DCD): 2.128ns = (17.128 - 15.000)
 Source Clock Delay (SCD): 2.456ns
 Clock Pessimism Removal (CPR): 0.184ns
 Clock Uncertainty: 0.035ns $((TSJ^2 + TIJ^2)^{1/2} + DJ) / 2 + PE$
 Total System Jitter (TSJ): 0.071ns
 Total Input Jitter (TIJ): 0.000ns
 Discrete Jitter (DJ): 0.000ns
 Phase Error (PE): 0.000ns

Location	Delay type	Incr(ns)	Path(ns)	Netlist Resource(s)
(clock axis_clk rise edge)				
		0.000	0.000	r axis_clk (IN)
net (fo=0)		0.000	0.000	r axis_clk
IBUF (Prop_ibuf_I_0)		0.972	0.972	r axis_clk_IBUF_inst/I
net (fo=1, unplaced)		0.800	1.771	r axis_clk_IBUF
BUFG (Prop_bufg_I_0)		0.101	1.872	r axis_clk_IBUF_BUFG_inst/O
net (fo=310, unplaced)		0.584	2.456	r ctrl_tap/axis_clk_IBUF_BUFG
FDRE				r ctrl_tap/ffen_r_reg/C
FDRE (Prop_fdre_C_Q)				
net (fo=129, unplaced)		0.478	2.934	r ctrl_tap/ffen_r_reg/Q
net (fo=1, unplaced)		0.576	3.510	r ctrl_tap/ffen
LUT3 (Prop_lut3_I1_0)		0.295	3.805	r ctrl_tap/sm_tdata_r1_0_i_1/I1
net (fo=1, unplaced)		0.800	4.605	r o_ram_data[16]
DSP48E1 (Prop_DSP48E1_A[16]_PCOUT[47])		4.036	8.641	r sm_tdata_r1_0/PCOUT[47]
net (fo=1, unplaced)		0.055	8.696	r sm_tdata_r1_0_n_106
DSP48E1 (Prop_DSP48E1_PCIN[47]_P[0])		1.518	10.214	r sm_tdata_r1_1/P[0]
net (fo=2, unplaced)		0.800	11.014	r sm_tdata_r1_1_n_105
LUT2 (Prop_lut2_I0_0)		0.124	11.138	r sm_tdata_r[19]_i_9/I0
net (fo=1, unplaced)		0.000	11.138	r sm_tdata_r[19]_i_9_n_0
CARRY4 (Prop_carry4_S[1]_CO[3])		0.533	11.671	r sm_tdata_r_reg[19]_i_6/CO[3]
net (fo=1, unplaced)		0.009	11.680	r sm_tdata_r_reg[19]_i_6_n_0
CARRY4 (Prop_carry4_CI_CO[3])		0.117	11.797	r sm_tdata_r_reg[23]_i_6/CI
net (fo=1, unplaced)		0.000	11.797	r sm_tdata_r_reg[27]_i_6/CI
CARRY4 (Prop_carry4_CI_0[3])		0.331	12.128	r sm_tdata_r_reg[27]_i_6/0[3]
net (fo=1, unplaced)		0.618	12.746	r sm_tdata_r_reg[27]_i_6_n_4
LUT2 (Prop_lut2_I1_0)		0.307	13.053	r sm_tdata_r[27]_i_2/I1
net (fo=1, unplaced)		0.000	13.053	r sm_tdata_r[27]_i_2_n_0
CARRY4 (Prop_carry4_S[3]_CO[3])		0.376	13.429	r sm_tdata_r_reg[27]_i_1/CO[3]
net (fo=1, unplaced)		0.000	13.429	r sm_tdata_r_reg[27]_i_1_n_0
CARRY4 (Prop_carry4_CI_0[3])		0.331	13.760	r sm_tdata_r_reg[31]_i_2/CI
net (fo=1, unplaced)		0.000	13.760	r sm_tdata_r_reg[31]_i_2_n_4
FDRE				r sm_tdata_r_reg[31]/D
(clock axis_clk rise edge)				
		15.000	15.000	r
net (fo=0)		0.000	15.000	r axis_clk (IN)
IBUF (Prop_ibuf_I_0)		0.838	15.838	r axis_clk_IBUF_inst/O
net (fo=1, unplaced)		0.760	16.598	r axis_clk_IBUF
BUFG (Prop_bufg_I_0)		0.091	16.689	r axis_clk_IBUF_BUFG_inst/O
net (fo=310, unplaced)		0.439	17.128	r axis_clk_IBUF_BUFG
FDRE				r sm_tdata_r_reg[31]/C
clock pessimism		0.184	17.311	
clock uncertainty		-0.035	17.276	
FDRE (Setup_fdre_C_D)		0.076	17.352	r sm_tdata_r_reg[31]
required time			17.352	
arrival time			-13.760	
slack			3.592	

Slack (MET) : 3.667ns (required time - arrival time)
 Source: ctrl_tap/ffen_r_reg/C
 (rising edge-triggered cell FDRE clocked by axis_clk {rise@0.000ns}
fall@7.500ns period=15.000ns)
 Destination: sm_tdata_r_reg[30]/D
 (rising edge-triggered cell FDRE clocked by axis_clk {rise@0.000ns}
fall@7.500ns period=15.000ns)
 Path Group: axis_clk
 Path Type: Setup (Max at Slow Process Corner)
 Requirement: 15.000ns (axis_clk rise@15.000ns - axis_clk rise@0.000ns)
 Data Path Delay: 11.228ns (logic 8.371ns (74.552%) route 2.857ns (25.448%))
 Logic Levels: 10 (CARRY4=5 DSP48E1=2 LUT2=2 LUT3=1)
 Clock Path Skew: -0.145ns (DCD - SCD + CPR)
 Destination Clock Delay (DCD): 2.128ns = (17.128 - 15.000)
 Source Clock Delay (SCD): 2.456ns
 Clock Pessimism Removal (CPR): 0.184ns
 Clock Uncertainty: 0.035ns ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
 Total System Jitter (TSJ): 0.071ns
 Total Input Jitter (TIJ): 0.000ns
 Discrete Jitter (DJ): 0.000ns
 Phase Error (PE): 0.000ns

Location	Delay type	Incr(ns)	Path(ns)	Netlist Resource(s)
(clock axis_clk rise edge)				
		0.000	0.000 r	
		0.000	0.000 r axis_clk (IN)	
net (fo=0)		0.000	0.000 r axis_clk	
			r axis_clk_IBUF_inst/I	
IBUF (Prop_ibuf_I_0)		0.972	0.972 r axis_clk_IBUF_inst/0	
net (fo=1, unplaced)		0.800	1.771 r axis_clk_IBUF	
			r axis_clk_IBUF_BUFG_inst/I	
BUFG (Prop_bufg_I_0)		0.101	1.872 r axis_clk_IBUF_BUFG_inst/0	
net (fo=310, unplaced)		0.584	2.456 r ctrl_tap/axis_clk_IBUF_BUFG	
			r ctrl_tap/ffen_r_reg/C	
FDRE (Prop_fdre_C_Q)				
net (fo=129, unplaced)		0.478	2.934 r ctrl_tap/ffen_r_reg/Q	
		0.576	3.510 r ctrl_tap/ffen	
			r ctrl_tap/sm_tdata_r1__0_i_1/I1	
LUT3 (Prop_lut3_I1_0)		0.295	3.805 r ctrl_tap/sm_tdata_r1__0_i_1/0	
net (fo=1, unplaced)		0.800	4.605 r o_ram_data[16]	
			r sm_tdata_r1__0/A[16]	
DSP48E1 (Prop_DSP48E1_A[16]_PCOUT[47])		4.036	8.641 r sm_tdata_r1__0/PCOUT[47]	
net (fo=1, unplaced)		0.055	8.696 r sm_tdata_r1__0_n_106	
			r sm_tdata_r1__1/PCIN[47]	
DSP48E1 (Prop_DSP48E1_PCIN[47]_P[0])		1.518	10.214 r sm_tdata_r1__1/P[0]	
net (fo=2, unplaced)		0.800	11.014 r sm_tdata_r1__1_n_105	
			r sm_tdata_r1[19].i_9/I0	
LUT2 (Prop_lut2_I0_0)		0.124	11.138 r sm_tdata_r1[19].i_9/0	
net (fo=1, unplaced)		0.000	11.138 r sm_tdata_r1[19].i_9_n_0	
			r sm_tdata_r1[19].i_6/S[1]	
CARRY4 (Prop_carry4_S[1]_CO[3])		0.533	11.671 r sm_tdata_r1[19].i_6/CO[3]	
net (fo=1, unplaced)		0.009	11.680 r sm_tdata_r1[19].i_6_n_0	
			r sm_tdata_r1[23].i_6/CI	
CARRY4 (Prop_carry4_CI_CO[3])		0.117	11.797 r sm_tdata_r1[23].i_6/CO[3]	
net (fo=1, unplaced)		0.000	11.797 r sm_tdata_r1[23].i_6_n_0	
			r sm_tdata_r1[27].i_6/CI	
CARRY4 (Prop_carry4_CI_0[3])		0.331	12.128 r sm_tdata_r1[27].i_6_n_0[3]	
net (fo=1, unplaced)		0.618	12.746 r sm_tdata_r1[27].i_6_n_4	
			r sm_tdata_r1[27].i_2/I1	
LUT2 (Prop_lut2_I1_0)		0.307	13.053 r sm_tdata_r1[27].i_2/0	
net (fo=1, unplaced)		0.000	13.053 r sm_tdata_r1[27].i_2_n_0	
			r sm_tdata_r1[27].i_1/S[3]	
CARRY4 (Prop_carry4_S[3]_CO[3])		0.376	13.429 r sm_tdata_r1[27].i_1/CO[3]	
net (fo=1, unplaced)		0.000	13.429 r sm_tdata_r1[27].i_1_n_0	
			r sm_tdata_r1[31].i_2/CI	
CARRY4 (Prop_carry4_CI_0[2])		0.256	13.685 r sm_tdata_r1[31].i_2/0[2]	
net (fo=1, unplaced)		0.000	13.685 r sm_tdata_r1[31].i_2_n_5	
			r sm_tdata_r1[30]/D	
(clock axis_clk rise edge)				
		15.000	15.000 r	
		0.000	15.000 r axis_clk (IN)	
net (fo=0)		0.000	15.000 r axis_clk	
			r axis_clk_IBUF_inst/I	
IBUF (Prop_ibuf_I_0)		0.838	15.838 r axis_clk_IBUF_inst/0	
net (fo=1, unplaced)		0.760	16.598 r axis_clk_IBUF	
			r axis_clk_IBUF_BUFG_inst/I	
BUFG (Prop_bufg_I_0)		0.091	16.689 r axis_clk_IBUF_BUFG_inst/0	
net (fo=310, unplaced)		0.439	17.128 r axis_clk_IBUF_BUFG	
			r sm_tdata_r1[30]/C	
FDRE (Setup_fdre_C_D)		0.076	17.352 r sm_tdata_r1[30]	
required time 17.352				
arrival time -13.685				
slack 3.667				

Slack (MET) : 3.691ns (required time - arrival time)
 Source: ctrl_tap/ffen_r_reg/C
 (rising edge-triggered cell FDRE clocked by axis_clk {rise@0.000ns}
fall@7.500ns period=15.000ns)
 Destination: sm_tdata_r_reg[28]/D
 (rising edge-triggered cell FDRE clocked by axis_clk {rise@0.000ns}
fall@7.500ns period=15.000ns)
 Path Group: axis_clk
 Path Type: Setup (Max at Slow Process Corner)
 Requirement: 15.000ns (axis_clk rise@15.000ns - axis_clk rise@0.000ns)
 Data Path Delay: 11.204ns (logic 8.347ns (74.497%) route 2.857ns (25.503%))
 Logic Levels: 10 (CARRY4=5 DSP48E1=2 LUT2=2 LUT3=1)
 Clock Path Skew: -0.145ns (DCD - SCD + CPR)
 Destination Clock Delay (DCD): 2.128ns = (17.128 - 15.000)
 Source Clock Delay (SCD): 2.456ns
 Clock Pessimism Removal (CPR): 0.184ns
 Clock Uncertainty: 0.035ns ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
 Total System Jitter (TSJ): 0.071ns
 Total Input Jitter (TIJ): 0.000ns
 Discrete Jitter (DJ): 0.000ns
 Phase Error (PE): 0.000ns

Location	Delay type	Incr(ns)	Path(ns)	Netlist Resource(s)
(clock axis_clk rise edge)				
		0.000	0.000 r	
		0.000	0.000 r axis_clk (IN)	
net (fo=0)		0.000	0.000 r axis_clk	
			r axis_clk_IBUF_inst/I	
IBUF (Prop_ibuf_I_0)		0.972	0.972 r axis_clk_IBUF_inst/0	
net (fo=1, unplaced)		0.800	1.771 r axis_clk_IBUF	
			r axis_clk_IBUF_BUFG_inst/I	
BUFG (Prop_bufg_I_0)		0.101	1.872 r axis_clk_IBUF_BUFG_inst/0	
net (fo=310, unplaced)		0.584	2.456 r ctrl_tap/axis_clk_IBUF_BUFG	
			r ctrl_tap/ffen_r_reg/C	
FDRE (Prop_fdre_C_Q)				
net (fo=129, unplaced)		0.478	2.934 r ctrl_tap/ffen_r_reg/Q	
		0.576	3.510 r ctrl_tap/ffen	
			r ctrl_tap/sm_tdata_r1_0_i_1/I1	
LUT3 (Prop_lut3_I1_0)		0.295	3.805 r ctrl_tap/sm_tdata_r1_0_i_1/I0	
net (fo=1, unplaced)		0.800	4.605 r o_ram_data[16]	
			r sm_tdata_r1_0/A[16]	
DSP48E1 (Prop_DSP48E1_A[16]_PCOUT[47])		4.036	8.641 r sm_tdata_r1_0/PCOUT[47]	
net (fo=1, unplaced)		0.055	8.696 r sm_tdata_r1_0_n_106	
			r sm_tdata_r1_1/PCIN[47]	
DSP48E1 (Prop_DSP48E1_PCIN[47]_P[0])		1.518	10.214 r sm_tdata_r1_1/P[0]	
net (fo=2, unplaced)		0.800	11.014 r sm_tdata_r1_1_n_105	
			r sm_tdata_r19_i_9/I0	
LUT2 (Prop_lut2_I0_0)		0.124	11.138 r sm_tdata_r19_i_9/0	
net (fo=1, unplaced)		0.000	11.138 r sm_tdata_r19_i_9_n_0	
			r sm_tdata_r19_i_6/S[1]	
CARRY4 (Prop_carry4_S[1]_CO[3])		0.533	11.671 r sm_tdata_r19_i_6/CO[3]	
net (fo=1, unplaced)		0.009	11.680 r sm_tdata_r19_i_6_n_0	
			r sm_tdata_r19_i_6/CI	
CARRY4 (Prop_carry4_CI_CO[3])		0.117	11.797 r sm_tdata_r19_i_6/CO[3]	
net (fo=1, unplaced)		0.000	11.797 r sm_tdata_r19_i_6_n_0	
			r sm_tdata_r19_i_6/CI	
CARRY4 (Prop_carry4_CI_0[3])		0.331	12.128 r sm_tdata_r19_i_6_n_0[3]	
net (fo=1, unplaced)		0.618	12.746 r sm_tdata_r19_i_6_n_4	
			r sm_tdata_r19_i_2/I1	
LUT2 (Prop_lut2_I1_0)		0.307	13.053 r sm_tdata_r19_i_2/0	
net (fo=1, unplaced)		0.000	13.053 r sm_tdata_r19_i_2_n_0	
			r sm_tdata_r19_i_1/S[3]	
CARRY4 (Prop_carry4_S[3]_CO[3])		0.376	13.429 r sm_tdata_r19_i_1/CO[3]	
net (fo=1, unplaced)		0.000	13.429 r sm_tdata_r19_i_1_n_0	
			r sm_tdata_r19_i_1/CI	
CARRY4 (Prop_carry4_CI_0[0])		0.232	13.661 r sm_tdata_r19_i_2/0[0]	
net (fo=1, unplaced)		0.000	13.661 r sm_tdata_r19_i_2_n_7	
			r sm_tdata_r19_i_2/D	
(clock axis_clk rise edge)				
		15.000	15.000 r	
		0.000	15.000 r axis_clk (IN)	
net (fo=0)		0.000	15.000 r axis_clk	
			r axis_clk_IBUF_inst/I	
IBUF (Prop_ibuf_I_0)		0.838	15.838 r axis_clk_IBUF_inst/0	
net (fo=1, unplaced)		0.760	16.598 r axis_clk_IBUF	
			r axis_clk_IBUF_BUFG_inst/I	
BUFG (Prop_bufg_I_0)		0.091	16.689 r axis_clk_IBUF_BUFG_inst/0	
net (fo=310, unplaced)		0.439	17.128 r axis_clk_IBUF_BUFG	
			r sm_tdata_r19_i_2/D	
FDRE		0.184	17.311 r sm_tdata_r19_i_2/C	
clock pessimism		-0.035	17.276 r sm_tdata_r19_i_2	
clock uncertainty		-0.035	17.276 r sm_tdata_r19_i_2	
FDRE (Setup_fdre_C_D)		0.076	17.352 r sm_tdata_r19_i_2	
required time 17.352				
arrival time -13.661				
slack 3.691				

```

Slack (MET) : 3.703ns (required time - arrival time)
Source: ctrl_tap/ffen_r_reg/C
          (rising edge-triggered cell FDRE clocked by axis_clk {rise@0.000ns
fall@7.500ns period=15.000ns})
Destination: sm_tdata_r_reg[25]/D
          (rising edge-triggered cell FDRE clocked by axis_clk {rise@0.000ns
fall@7.500ns period=15.000ns})
Path Group: axis_clk
Path Type: Setup (Max at Slow Process Corner)
Requirement: 15.000ns (axis_clk rise@15.000ns - axis_clk rise@0.000ns)
Data Path Delay: 11.192ns (logic 8.335ns (74.47%) route 2.857ns (25.53%))
Logic Levels: 9 (CARRY4=4 DSP48E1=2 LUT2=2 LUT3=1)
Clock Path Skew: -0.145ns (DCD - SCD + CPR)
Destination Clock Delay (DCD): 2.128ns = ( 17.128 - 15.000 )
Source Clock Delay (SCD): 2.456ns
Clock Pessimism Removal (CPR): 0.184ns
Clock Uncertainty: 0.035ns ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
Total System Jitter (TSJ): 0.071ns
Total Input Jitter (TIJ): 0.000ns
Discrete Jitter (DJ): 0.000ns
Phase Error (PE): 0.000ns

Location      Delay type      Incr(ns)  Path(ns)  Netlist Resource(s)
-----+-----+-----+-----+-----+
(clock axis_clk rise edge)
          0.000   0.000 r
          0.000   0.000 r axis_clk (IN)
net (fo=0)    0.000   0.000 r axis_clk
               r axis_clk_IBUF_inst/I
IBUF (Prop_ibuf_I_0)  0.972   0.972 r axis_clk_IBUF_inst/0
net (fo=1, unplaced) 0.800   1.771 r axis_clk_IBUF
               r axis_clk_IBUF_BUFG_inst/I
BUFG (Prop_bufg_I_0)  0.101   1.872 r axis_clk_IBUF_BUFG_inst/0
net (fo=310, unplaced) 0.584   2.456 r ctrl_tap/axis_clk_IBUF_BUFG
               r ctrl_tap/ffen_r_reg/C
FDRE
          0.478   2.934 r ctrl_tap/ffen_r_reg/Q
net (fo=129, unplaced) 0.576   3.510 r ctrl_tap/ffen
               r ctrl_tap/sm_tdata_r1_0_i_1/I1
LUT3 (Prop_lut3_I1_0)  0.295   3.805 r ctrl_tap/sm_tdata_r1_0_i_1/I0
net (fo=1, unplaced)  0.800   4.605 r o_ram_data[16]
               r sm_tdata_r1_0/A[16]
DSP48E1 (Prop_DSP48E1_A[16]_PCOUT[47])
          4.036   8.641 r sm_tdata_r1_0/PCOUT[47]
net (fo=1, unplaced)  0.055   8.696 r sm_tdata_r1_0_n_106
               r sm_tdata_r1_1/PCIN[47]
DSP48E1 (Prop_DSP48E1_PCIN[47]_P[0])
          1.518   10.214 r sm_tdata_r1_1/P[0]
net (fo=2, unplaced)  0.800   11.014 r sm_tdata_r1_1_n_105
               r sm_tdata_r1[19]_i_9/I0
LUT2 (Prop_lut2_I0_0)  0.124   11.138 r sm_tdata_r1[19]_i_9/0
net (fo=1, unplaced)  0.000   11.138 r sm_tdata_r1[19]_i_9_n_0
               r sm_tdata_r1[19]_i_6/S[1]
CARRY4 (Prop_carry4_S[1]_CO[3])
          0.533   11.671 r sm_tdata_r1[19]_i_6/CO[3]
net (fo=1, unplaced)  0.009   11.680 r sm_tdata_r1[19]_i_6_n_0
               r sm_tdata_r1[23]_i_6/CI
CARRY4 (Prop_carry4_CI_0[3])
          0.331   12.011 r sm_tdata_r1[23]_i_6/0[3]
net (fo=1, unplaced)  0.618   12.629 r sm_tdata_r1[23]_i_6_n_4
               r sm_tdata_r1[23]_i_2/I1
LUT2 (Prop_lut2_I1_0)  0.307   12.936 r sm_tdata_r1[23]_i_2/0
net (fo=1, unplaced)  0.000   12.936 r sm_tdata_r1[23]_i_2_n_0
               r sm_tdata_r1[23]_i_1/S[3]
CARRY4 (Prop_carry4_S[3]_CO[3])
          0.376   13.312 r sm_tdata_r1[23]_i_1/CO[3]
net (fo=1, unplaced)  0.000   13.312 r sm_tdata_r1[23]_i_1_n_0
               r sm_tdata_r1[27]_i_1/CI
CARRY4 (Prop_carry4_CI_0[1])
          0.337   13.649 r sm_tdata_r1[27]_i_1/0[1]
net (fo=1, unplaced)  0.000   13.649 r sm_tdata_r1[27]_i_1_n_6
               r sm_tdata_r1[25]/D
FDRE
          15.000   15.000 r
          0.000   15.000 r axis_clk (IN)
net (fo=0)    0.000   15.000 r axis_clk
               r axis_clk_IBUF_inst/I
IBUF (Prop_ibuf_I_0)  0.838   15.838 r axis_clk_IBUF_inst/0
net (fo=1, unplaced) 0.760   16.598 r axis_clk_IBUF
               r axis_clk_IBUF_BUFG_inst/I
BUFG (Prop_bufg_I_0)  0.091   16.689 r axis_clk_IBUF_BUFG_inst/0
net (fo=310, unplaced) 0.439   17.128 r axis_clk_IBUF_BUFG
               r sm_tdata_r1[25]/C
clock pessimism     0.184   17.311
clock uncertainty   -0.035   17.276
FDRE (Setup_fdr_C_D) 0.076   17.352 sm_tdata_r1[25]

-----+-----+
required time        17.352
arrival time         -13.649
-----+-----+
slack                3.703

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Slack (MET) : 3.709ns (required time - arrival time)
Source: ctrl_tap/ffen_r_reg/C
          (rising edge-triggered cell FDRE clocked by axis_clk {rise@0.000ns
fall@7.500ns period=15.000ns})
Destination: sm_tdata_r_reg[27]/D
          (rising edge-triggered cell FDRE clocked by axis_clk {rise@0.000ns
fall@7.500ns period=15.000ns})
Path Group: axis_clk
Path Type: Setup (Max at Slow Process Corner)
Requirement: 15.000ns (axis_clk rise@15.000ns - axis_clk rise@0.000ns)
Data Path Delay: 11.186ns (logic 8.329ns (74.456%) route 2.857ns (25.544%))
Logic Levels: 9 ((CARRY4=4 DSP48E1=2 LUT2=2 LUT3=1)
Clock Path Skew: -0.145ns (DCD - SCD + CPR)
Destination Clock Delay (DCD): 2.128ns = ( 17.128 - 15.000 )
Source Clock Delay (SCD): 2.456ns
Clock Pessimism Removal (CPR): 0.184ns
Clock Uncertainty: 0.035ns  $((TSJ^2 + TIJ^2)^{1/2} + DJ) / 2 + PE$ 
Total System Jitter (TSJ): 0.071ns
Total Input Jitter (TIJ): 0.000ns
Discrete Jitter (DJ): 0.000ns
Phase Error (PE): 0.000ns

Location Delay type Incr(ns) Path(ns) Netlist Resource(s)
-----  

(clock axis_clk rise edge)
      0.000 0.000 r axis_clk (IN)
      0.000 0.000 r axis_clk
net (fo=0) 0.000 0.000 r axis_clk_IBUF_inst/I
IBUF (Prop_ibuf_I_0) 0.072 0.072 r axis_clk_IBUF_inst/0
net (fo=1, unplaced) 0.800 1.771 r axis_clk_IBUF
                           r axis_clk_IBUF_BUFG_inst/I
BUFG (Prop_bufg_I_0) 0.101 1.872 r axis_clk_IBUF_BUFG_inst/0
net (fo=310, unplaced) 0.584 2.456 r ctrl_tap/axis_clk_IBUF_BUFG
FDRE
-----  

FDRE (Prop_fdre_C_Q) 0.478 2.934 r ctrl_tap/ffen_r_reg/Q
net (fo=129, unplaced) 0.576 3.510 r ctrl_tap/ffen
                           r ctrl_tap/sm_tdata_r1_0_i_1/I1
LUT3 (Prop_lut3_I1_0) 0.295 3.805 r ctrl_tap/sm_tdata_r1_0_i_1/0
net (fo=1, unplaced) 0.800 4.605 r o_ram_data[16]
                           r sm_tdata_r1_0/A[16]
DSP48E1 (Prop_DSP48E1_A[16]_PCOUT[47])
      4.036 8.641 r sm_tdata_r1_0/PCOUT[47]
net (fo=1, unplaced) 0.055 8.696 r sm_tdata_r1_0_n_106
                           r sm_tdata_r1_1/PCIN[47]
DSP48E1 (Prop_DSP48E1_PCIN[47]_P[0])
      1.518 10.214 r sm_tdata_r1_1/P[0]
net (fo=2, unplaced) 0.800 11.014 r sm_tdata_r1_1_n_105
                           r sm_tdata_r19_i_9/I0
LUT2 (Prop_lut2_I0_0) 0.124 11.138 r sm_tdata_r19_i_9/0
net (fo=1, unplaced) 0.000 11.138 r sm_tdata_r19_i_9_n_0
                           r sm_tdata_r19_i_6/S[1]
CARRY4 (Prop_carry4_S[1]_CO[3])
      0.533 11.671 r sm_tdata_r19_i_6/CO[3]
net (fo=1, unplaced) 0.009 11.680 r sm_tdata_r19_i_6_n_0
                           r sm_tdata_r19_i_6/CI
CARRY4 (Prop_carry4_CI_0[3])
      0.331 12.011 r sm_tdata_r19_i_6/0[3]
net (fo=1, unplaced) 0.618 12.629 r sm_tdata_r19_i_6_n_4
                           r sm_tdata_r19_i_2/I1
LUT2 (Prop_lut2_I1_0) 0.307 12.936 r sm_tdata_r19_i_2/0
net (fo=1, unplaced) 0.000 12.936 r sm_tdata_r19_i_2_n_0
                           r sm_tdata_r19_i_1/S[3]
CARRY4 (Prop_carry4_S[3]_CO[3])
      0.376 13.312 r sm_tdata_r19_i_1/CO[3]
net (fo=1, unplaced) 0.000 13.312 r sm_tdata_r19_i_1_n_0
                           r sm_tdata_r19_i_1/CI
CARRY4 (Prop_carry4_CI_0[3])
      0.331 13.643 r sm_tdata_r19_i_1/0[3]
net (fo=1, unplaced) 0.000 13.643 r sm_tdata_r19_i_1_n_4
                           r sm_tdata_r19_i_0/D
FDRE
-----  

(clock axis_clk rise edge)
      15.000 15.000 r axis_clk (IN)
      0.000 15.000 r axis_clk
net (fo=0) 0.000 15.000 r axis_clk
                           r axis_clk_IBUF_inst/I
IBUF (Prop_ibuf_I_0) 0.838 15.838 r axis_clk_IBUF_inst/0
net (fo=1, unplaced) 0.760 16.598 r axis_clk_IBUF
                           r axis_clk_IBUF_BUFG_inst/I
BUFG (Prop_bufg_I_0) 0.091 16.689 r axis_clk_IBUF_BUFG_inst/0
net (fo=310, unplaced) 0.439 17.128 r axis_clk_IBUF_BUFG
FDRE
clock pessimism 0.184 17.311
clock uncertainty -0.035 17.276
FDRE (Setup_fdre_C_D) 0.076 17.352 r sm_tdata_r19_i_0/D

required time 17.352
arrival time -13.643
-----  

slack 3.709

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Slack (MET) : 3.784ns (required time - arrival time)
Source: ctrl_tap/ffen_r_reg/C
          (rising edge-triggered cell FDRE clocked by axis_clk {rise@0.000ns
fall@7.500ns period=15.000ns})
Destination: sm_tdata_r_reg[26]/D
          (rising edge-triggered cell FDRE clocked by axis_clk {rise@0.000ns
fall@7.500ns period=15.000ns})
Path Group: axis_clk
Path Type: Setup (Max at Slow Process Corner)
Requirement: 15.000ns (axis_clk rise@15.000ns - axis_clk rise@0.000ns)
Data Path Delay: 11.111ns (logic 8.254ns (74.284%) route 2.857ns (25.716%))
Logic Levels: 9 (CARRY4=4 DSP48E1=2 LUT2=2 LUT3=1)
Clock Path Skew: -0.145ns (DCD - SCD + CPR)
Destination Clock Delay (DCD): 2.128ns = ( 17.128 - 15.000 )
Source Clock Delay (SCD): 2.456ns
Clock Pessimism Removal (CPR): 0.184ns
Clock Uncertainty: 0.035ns ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
Total System Jitter (TSJ): 0.071ns
Total Input Jitter (TIJ): 0.000ns
Discrete Jitter (DJ): 0.000ns
Phase Error (PE): 0.000ns

Location      Delay type      Incr(ns)  Path(ns)  Netlist Resource(s)
-----+-----+-----+-----+-----+
(clock axis_clk rise edge)
          0.000    0.000 r  axis_clk (IN)
net (fo=0)        0.000    0.000   axis_clk
                  r  axis_clk_IBUF_inst/I
IBUF (Prop_ibuf_I_0)  0.972    0.972 r  axis_clk_IBUF_inst/0
net (fo=1, unplaced)  0.800    1.771   axis_clk_IBUF
                  r  axis_clk_IBUF_BUFG_inst/I
BUFG (Prop_bufg_I_0)  0.101    1.872 r  axis_clk_IBUF_BUFG_inst/0
net (fo=310, unplaced)  0.584    2.456   ctrl_tap/axis_clk_BUFG
                  r  ctrl_tap/ffen_r_reg/C
FDRE
          0.478    2.934 r  ctrl_tap/ffen_r_reg/Q
net (fo=129, unplaced)  0.576    3.510   ctrl_tap/ffen
                  r  ctrl_tap/sm_tdata_r1_0_l_1/I1
LUT3 (Prop_lut3_I1_0)  0.295    3.805 r  ctrl_tap/sm_tdata_r1_0_l_1/O
net (fo=1, unplaced)  0.800    4.605   o_ran_data[16]
                  r  sm_tdata_r1_0/A[16]
DSP48E1 (Prop_DSP48E1_A[16]_PCOUT[47])
          4.036    8.641 r  sm_tdata_r1_0/PCOUT[47]
net (fo=1, unplaced)  0.055    8.696   sm_tdata_r1_0_n_106
                  r  sm_tdata_r1_0_n_106
DSP48E1 (Prop_DSP48E1_PCIN[47]_P[0])
          1.518    10.214 r  sm_tdata_r1_1/P[0]
net (fo=2, unplaced)  0.000    11.014   sm_tdata_r1_1_n_105
                  r  sm_tdata_r1_1_n_105
LUT2 (Prop_lut2_I0_0)  0.124    11.138 r  sm_tdata_r1_1_n_9/0
net (fo=1, unplaced)  0.000    11.138   sm_tdata_r1_1_n_9_n_0
                  r  sm_tdata_r1_1_n_9_n_0
                  r  sm_tdata_r1_1_n_9_n_0
CARRY4 (Prop_carry4_S[1]_CO[3])
          0.533    11.671 r  sm_tdata_r1_1_n_6/0[3]
net (fo=1, unplaced)  0.009    11.680   sm_tdata_r1_1_n_6_n_0
                  r  sm_tdata_r1_1_n_6_n_0
CARRY4 (Prop_carry4_CI_0[3])
          0.331    12.011 r  sm_tdata_r1_1_n_6/0[3]
net (fo=1, unplaced)  0.618    12.629   sm_tdata_r1_1_n_6_n_4
                  r  sm_tdata_r1_1_n_6_n_4
LUT2 (Prop_lut2_I1_0)  0.307    12.936 r  sm_tdata_r1_1_n_2/11
net (fo=1, unplaced)  0.000    12.936   sm_tdata_r1_1_n_2/0
                  r  sm_tdata_r1_1_n_2/0
                  r  sm_tdata_r1_1_n_2/0
CARRY4 (Prop_carry4_S[3]_CO[3])
          0.376    13.312 r  sm_tdata_r1_1_n_1/0[3]
net (fo=1, unplaced)  0.000    13.312   sm_tdata_r1_1_n_1_n_0
                  r  sm_tdata_r1_1_n_1_n_0
CARRY4 (Prop_carry4_CI_0[2])
          0.256    13.568 r  sm_tdata_r1_1_n_1/0[2]
net (fo=1, unplaced)  0.000    13.568   sm_tdata_r1_1_n_1_n_5
                  r  sm_tdata_r1_1_n_1_n_5
FDRE
          15.000   15.000 r  sm_tdata_r1_1_n_1_n_5
net (fo=0)        0.000   15.000   axis_clk
                  r  axis_clk_IBUF_inst/I
IBUF (Prop_ibuf_I_0)  0.838    15.838 r  axis_clk_IBUF_inst/0
net (fo=1, unplaced)  0.760    16.598   axis_clk_IBUF
                  r  axis_clk_IBUF_BUFG_inst/I
BUFG (Prop_bufg_I_0)  0.091    16.689 r  axis_clk_IBUF_BUFG_inst/0
net (fo=310, unplaced)  0.439    17.128   axis_clk_IBUF_BUFG
                  r  sm_tdata_r1_1_n_5
clock pessimism     0.184    17.311
clock uncertainty  -0.035    17.276
FDRE (Setup_fdre_C_D)  0.076    17.352   sm_tdata_r1_1_n_5

required time       17.352
arrival time        -13.568
-----+-----+
slack                3.784

Slack (MET) : 3.808ns (required time - arrival time)
Source: ctrl_tap/ffen_r_reg/C
          (rising edge-triggered cell FDRE clocked by axis_clk {rise@0.000ns
fall@7.500ns period=15.000ns})
Destination: sm_tdata_r_reg[24]/D
          (rising edge-triggered cell FDRE clocked by axis_clk {rise@0.000ns
fall@7.500ns period=15.000ns})
Path Group: axis_clk
Path Type: Setup (Max at Slow Process Corner)
Requirement: 15.000ns (axis_clk rise@15.000ns - axis_clk rise@0.000ns)
Data Path Delay: 11.087ns (logic 8.230ns (74.228%) route 2.857ns (25.772%))
Logic Levels: 9 (CARRY4=4 DSP48E1=2 LUT2=2 LUT3=1)
Clock Path Skew: -0.145ns (DCD - SCD + CPR)
Destination Clock Delay (DCD): 2.128ns = ( 17.128 - 15.000 )
Source Clock Delay (SCD): 2.456ns
Clock Pessimism Removal (CPR): 0.184ns
Clock Uncertainty: 0.035ns ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
Total System Jitter (TSJ): 0.071ns
Total Input Jitter (TIJ): 0.000ns
Discrete Jitter (DJ): 0.000ns
Phase Error (PE): 0.000ns

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Location	Delay type	Incr(ns)	Path(ns)	Netlist Resource(s)
<hr/>				
	(clock axis_clk rise edge)			
		0.000	0.000 r	
		0.000	0.000 r axis_clk (IN)	
net (fo=0)		0.000	0.000 r axis_clk	
			r axis_clk_IBUF_inst/I	
IBUF (Prop_ibuf_I_0)		0.972	0.972 r axis_clk_IBUF_inst/0	
net (fo=1, unplaced)		0.800	1.771 r axis_clk_IBUF	
			r axis_clk_IBUF_BUFG_inst/I	
BUFG (Prop_bufg_I_0)		0.101	1.872 r axis_clk_IBUF_BUFG_inst/0	
net (fo=310, unplaced)		0.584	2.456 r ctrl_tap/axis_clk_IBUF_BUFG	
FDRE			r ctrl_tap/ffen_r_reg/C	
FDRE (Prop_fdre_C_Q)		0.478	2.934 r ctrl_tap/ffen_r_reg/Q	
net (fo=129, unplaced)		0.576	3.510 r ctrl_tap/ffen	
			r ctrl_tap/sm_tdata_r1_0_i_1/I1	
LUT3 (Prop_lut3_I1_0)		0.295	3.805 r ctrl_tap/sm_tdata_r1_0_i_1/0	
net (fo=1, unplaced)		0.800	4.605 r o_ram_data[16]	
			r sm_tdata_r1_0/A[16]	
DSP48E1 (Prop_dsp48e1_A[16]_PCOUT[47])		4.036	8.641 r sm_tdata_r1_0/PCOUT[47]	
net (fo=1, unplaced)		0.055	8.696 r sm_tdata_r1_0_n_106	
			r sm_tdata_r1_1/PCIN[47]	
DSP48E1 (Prop_dsp48e1_PCIN[47]_P[0])		1.518	10.214 r sm_tdata_r1_1/P[0]	
net (fo=2, unplaced)		0.800	11.014 r sm_tdata_r1_1_n_105	
			r sm_tdata_r[19]_i_9/I0	
LUT2 (Prop_lut2_I0_0)		0.124	11.138 r sm_tdata_r[19]_i_9/0	
net (fo=1, unplaced)		0.000	11.138 r sm_tdata_r[19]_i_9_n_0	
			r sm_tdata_r_reg[19]_i_6/S[1]	
CARRY4 (Prop_carry4_S[1]_C0[3])		0.533	11.671 r sm_tdata_r_reg[19]_i_6/C0[3]	
net (fo=1, unplaced)		0.009	11.680 r sm_tdata_r_reg[19]_i_6_n_0	
			r sm_tdata_r_reg[23]_i_6/C1	
CARRY4 (Prop_carry4_CI_0[3])		0.331	12.011 r sm_tdata_r_reg[23]_i_6/0[3]	
net (fo=1, unplaced)		0.618	12.629 r sm_tdata_r_reg[23]_i_6_n_4	
			r sm_tdata_r[23]_i_2/I1	
LUT2 (Prop_lut2_I1_0)		0.307	12.936 r sm_tdata_r[23]_i_2/0	
net (fo=1, unplaced)		0.000	12.936 r sm_tdata_r[23]_i_2_n_0	
			r sm_tdata_r_reg[23]_i_1/S[3]	
CARRY4 (Prop_carry4_S[3]_C0[3])		0.376	13.312 r sm_tdata_r_reg[23]_i_1/C0[3]	
net (fo=1, unplaced)		0.000	13.312 r sm_tdata_r_reg[23]_i_1_n_0	
			r sm_tdata_r_reg[27]_i_1/C1	
CARRY4 (Prop_carry4_CI_0[0])		0.232	13.544 r sm_tdata_r_reg[27]_i_1/0[0]	
net (fo=1, unplaced)		0.000	13.544 r sm_tdata_r_reg[27]_i_1_n_7	
FDRE			r sm_tdata_r_reg[24]/D	
<hr/>				
	(clock axis_clk rise edge)			
		15.000	15.000 r	
		0.000	15.000 r axis_clk (IN)	
net (fo=0)		0.000	15.000 r axis_clk	
			r axis_clk_IBUF_inst/I	
IBUF (Prop_ibuf_I_0)		0.838	15.838 r axis_clk_IBUF_inst/0	
net (fo=1, unplaced)		0.760	16.598 r axis_clk_IBUF	
			r axis_clk_IBUF_BUFG_inst/I	
BUFG (Prop_bufg_I_0)		0.091	16.689 r axis_clk_IBUF_BUFG_inst/0	
net (fo=310, unplaced)		0.439	17.128 r axis_clk_IBUF_BUFG	
FDRE			r sm_tdata_r_reg[24]/C	
clock pessimism		0.184	17.311	
clock uncertainty		-0.035	17.276	
FDRE (Setup_fdre_C_D)		0.076	17.352 r sm_tdata_r_reg[24]	
required time			17.352	
arrival time			-13.544	
slack			3.808	

```

● ● ●

Slack (MET) : 3.933ns (required time - arrival time)
  Source: ctrl_tap/ffen_r_reg/C
    (rising edge-triggered cell FDRE clocked by axis_clk {rise@0.000ns
fall@7.500ns period=15.000ns})
  Destination: sm_tdata_r_reg[21]/D
    (rising edge-triggered cell FDRE clocked by axis_clk {rise@0.000ns
fall@7.500ns period=15.000ns})
  Path Group: axis_clk
  Path Type: Setup (Max at Slow Process Corner)
  Requirement: 15.000ns (axis_clk rise@15.000ns - axis_clk rise@0.000ns)
  Data Path Delay: 10.962ns (Logic 8.114ns (74.016%) route 2.848ns (25.984%))
  Logic Levels: 8 (CARRY4=3 DSP48E1=2 LUT2=2 LUT3=1)
  Clock Path Skew: -0.145ns (DCD - SCD + CPR)
    Destination Clock Delay (DCD): 2.128ns = ( 17.128 - 15.000 )
    Source Clock Delay (SCD): 2.456ns
    Clock Pessimism Removal (CPR): 0.184ns
  Clock Uncertainty: 0.035ns ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ): 0.071ns
    Total Input Jitter (TIJ): 0.000ns
    Discrete Jitter (DJ): 0.000ns
    Phase Error (PE): 0.000ns

  Location      Delay type      Incr(ns)  Path(ns)  Netlist Resource(s)
  -----
  (clock axis_clk rise edge)
    0.000      0.000 r  axis_clk (IN)
    0.000      0.000 r  axis_clk
    net (fo=0)  0.000      r  axis_clk_IBUF_inst/I
    IBUF (Prop_ibuf_I_0)  0.972      0.972 r  axis_clk_IBUF_inst/O
    net (fo=1, unplaced)  0.800      1.771 r  axis_clk_IBUF
    BUFG (Prop_bufg_I_0)  0.101      1.872 r  axis_clk_IBUF_BUFG_inst/I
    net (fo=310, unplaced)  0.584      2.456 r  ctrl_tap/axis_clk_IBUF_BUFG
    FDRE
  -----
    FDRE (Prop_fdre_C_Q)  0.478      2.934 r  ctrl_tap/ffen_r_reg/Q
    net (fo=129, unplaced)  0.576      3.510 r  ctrl_tap/ffen
    r  ctrl_tap/sm_tdata_r1__0_i_1/I1
    LUT3 (Prop_lut3_I1_0)  0.295      3.805 r  ctrl_tap/sm_tdata_r1__0_i_1/I0
    net (fo=1, unplaced)  0.800      4.605 r  o_ram_data[16]
    r  sm_tdata_r1__0/A[16]
    DSP48E1 (Prop_DSP48E1_A[16]_PCOUT[47])
      4.036      8.641 r  sm_tdata_r1__0/PCOUT[47]
    net (fo=1, unplaced)  0.055      8.696 r  sm_tdata_r1__0_n_106
    r  sm_tdata_r1__1/PCIN[47]
    DSP48E1 (Prop_DSP48E1_PCIN[47]_P[0])
      1.518      10.214 r  sm_tdata_r1__1/P[0]
    net (fo=2, unplaced)  0.800      11.014 r  sm_tdata_r1__1_n_105
    r  sm_tdata_r1[19]_i_9/I0
    LUT2 (Prop_lut2_I0_0)  0.124      11.138 r  sm_tdata_r1[19]_i_9/0
    net (fo=1, unplaced)  0.000      11.138 r  sm_tdata_r1[19]_i_9_n_0
    r  sm_tdata_r1[19]_i_6/S[1]
    CARRY4 (Prop_carry4_S[1]_0[3])
      0.643      11.781 r  sm_tdata_r1[19]_i_6/0[3]
    net (fo=1, unplaced)  0.618      12.399 r  sm_tdata_r1[19]_i_6_n_4
    r  sm_tdata_r1[19]_i_2/I1
    LUT2 (Prop_lut2_I1_0)  0.307      12.706 r  sm_tdata_r1[19]_i_2/0
    net (fo=1, unplaced)  0.000      12.706 r  sm_tdata_r1[19]_i_2_n_0
    r  sm_tdata_r1[19]_i_1/S[3]
    CARRY4 (Prop_carry4_S[3]_0[3])
      0.376      13.082 r  sm_tdata_r1[19]_i_1/C0[3]
    net (fo=1, unplaced)  0.000      13.082 r  sm_tdata_r1[19]_i_1_n_0
    r  sm_tdata_r1[23]_i_1/C1
    CARRY4 (Prop_carry4_CI_0[1])
      0.337      13.419 r  sm_tdata_r1[23]_i_1/0[1]
    net (fo=1, unplaced)  0.000      13.419 r  sm_tdata_r1[23]_i_1_n_6
    FDRE
  -----
  (clock axis_clk rise edge)
    15.000      15.000 r  axis_clk (IN)
    0.000      15.000 r  axis_clk
    net (fo=0)  0.000      15.000 r  axis_clk_IBUF_inst/I
    IBUF (Prop_ibuf_I_0)  0.838      15.838 r  axis_clk_IBUF_inst/O
    net (fo=1, unplaced)  0.760      16.598 r  axis_clk_IBUF
    BUFG (Prop_bufg_I_0)  0.091      16.689 r  axis_clk_IBUF_BUFG_inst/I
    net (fo=310, unplaced)  0.439      17.128 r  axis_clk_IBUF_BUFG
    FDRE
    clock pessimism  0.184      17.311
    clock uncertainty -0.035      17.276
    FDRE (Setup_fdre_C_D)  0.076      17.352 sm_tdata_r1[21]
  -----
  required time  17.352
  arrival time -13.419
  -----
  slack          3.933
  -----
  slack          3.939

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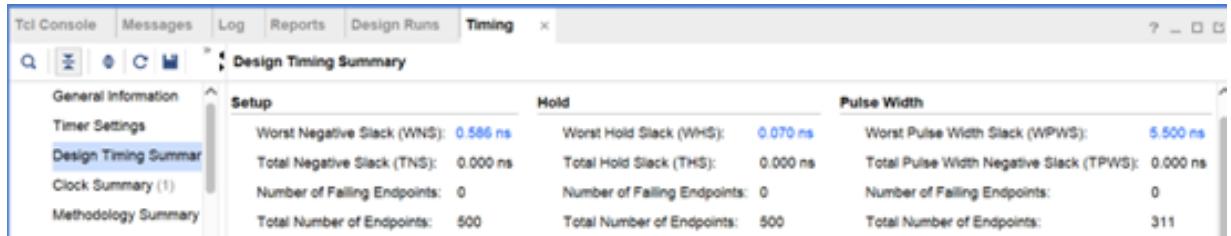
Slack (MET) : 3.939ns (required time - arrival time)
  Source: ctrl_tap/ffen_r_reg/C
    (rising edge-triggered cell FDRE clocked by axis_clk {rise@0.000ns
fall@7.500ns period=15.000ns})
  Destination: sm_tdata_r_reg[23]/D
    (rising edge-triggered cell FDRE clocked by axis_clk {rise@0.000ns
fall@7.500ns period=15.000ns})
  Path Group: axis_clk
  Path Type: Setup (Max at Slow Process Corner)
  Requirement: 15.000ns (axis_clk rise@15.000ns - axis_clk rise@0.000ns)
  Data Path Delay: 10.956ns (logic 8.108ns (74.002%) route 2.848ns (25.998%))
  Logic Levels: 8 (CARRY4=3 DSP48E1=2 LUT2=2 LUT3=1)
  Clock Path Skew: -0.145ns (DCD - SCD + CPR)
  Destination Clock Delay (DCD): 2.128ns = ( 17.128 - 15.000 )
  Source Clock Delay (SCD): 2.456ns
  Clock Pessimism Removal (CPR): 0.184ns
  Clock Uncertainty: 0.035ns ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
  Total System Jitter (TSJ): 0.071ns
  Total Input Jitter (TIJ): 0.000ns
  Discrete Jitter (DJ): 0.000ns
  Phase Error (PE): 0.000ns

  Location      Delay type      Incr(ns)  Path(ns)  Netlist Resource(s)
  -----
  (clock axis_clk rise edge)
  net (fo=0)          0.000      0.000 r axis_clk (IN)
  IBUF (Prop_ibuf_I_0) 0.972      0.972 r axis_clk_IBUF_inst/I
  net (fo=1, unplaced) 0.800      1.771 r axis_clk_IBUF
  BUFG (Prop_bufg_I_0) 0.101      1.872 r axis_clk_IBUF_BUFG_inst/O
  net (fo=310, unplaced) 0.584      2.456 r ctrl_tap/axis_clk_IBUF_BUFG
  FDRE               0.000      2.456 r ctrl_tap/ffen_r_reg/C
  -----
  FDRE (Prop_fdre_C_Q) 0.478      2.934 r ctrl_tap/ffen_r_reg/Q
  net (fo=129, unplaced) 0.576      3.510 r ctrl_tap/ffen
  LUT3 (Prop_lut3_I1_0) 0.295      3.805 r ctrl_tap/sm_tdata_r1_0_i_1/I1
  net (fo=1, unplaced) 0.800      4.605 r o_ram_data[16]
  r sm_tdata_r1_0/A[16]
  DSP48E1 (Prop_dsp48e1_A[16]_PCOUT[47]) 4.036      8.641 r sm_tdata_r1_0/PCOUT[47]
  net (fo=1, unplaced) 0.055      8.696 r sm_tdata_r1_0_n_106
  r sm_tdata_r1_1/PCIN[47]
  DSP48E1 (Prop_dsp48e1_PCIN[47]_P[0]) 1.518      10.214 r sm_tdata_r1_1/P[0]
  net (fo=2, unplaced) 0.800      11.014 r sm_tdata_r1_1_n_105
  r sm_tdata_r[19].i_9/I0
  LUT2 (Prop_lut2_I0_0) 0.124      11.138 r sm_tdata_r[19].i_9/0
  net (fo=1, unplaced) 0.000      11.138 r sm_tdata_r[19].i_9_n_0
  r sm_tdata_r[19].i_6/S[1]
  CARRY4 (Prop_carry4_S[1]_0[3]) 0.643      11.781 r sm_tdata_r_reg[19].i_6/0[3]
  net (fo=1, unplaced) 0.618      12.399 r sm_tdata_r_reg[19].i_6_n_4
  r sm_tdata_r[19].i_2/I1
  LUT2 (Prop_lut2_I1_0) 0.307      12.706 r sm_tdata_r[19].i_2/0
  net (fo=1, unplaced) 0.000      12.706 r sm_tdata_r[19].i_2_n_0
  r sm_tdata_r[19].i_1/S[3]
  CARRY4 (Prop_carry4_S[3]_C0[3]) 0.376      13.082 r sm_tdata_r_reg[19].i_1/C0[3]
  net (fo=1, unplaced) 0.000      13.082 r sm_tdata_r_reg[19].i_1_n_0
  r sm_tdata_r_reg[23].i_1/CI
  CARRY4 (Prop_carry4_CI_0[3]) 0.331      13.413 r sm_tdata_r_reg[23].i_1_0[3]
  net (fo=1, unplaced) 0.000      13.413 r sm_tdata_r_reg[23].i_1_n_4
  r sm_tdata_r_reg[23]/D
  -----
  (clock axis_clk rise edge)
  net (fo=0)          15.000     15.000 r axis_clk (IN)
  IBUF (Prop_ibuf_I_0) 0.838      15.838 r axis_clk_IBUF_inst/O
  net (fo=1, unplaced) 0.760      16.598 r axis_clk_IBUF
  BUFG (Prop_bufg_I_0) 0.091      16.689 r axis_clk_IBUF_BUFG_inst/O
  net (fo=310, unplaced) 0.439      17.128 r axis_clk_IBUF_BUFG
  FDRE               0.076      17.352 r sm_tdata_r_reg[23]
  -----
  required time           17.352
  arrival time            -13.413

```

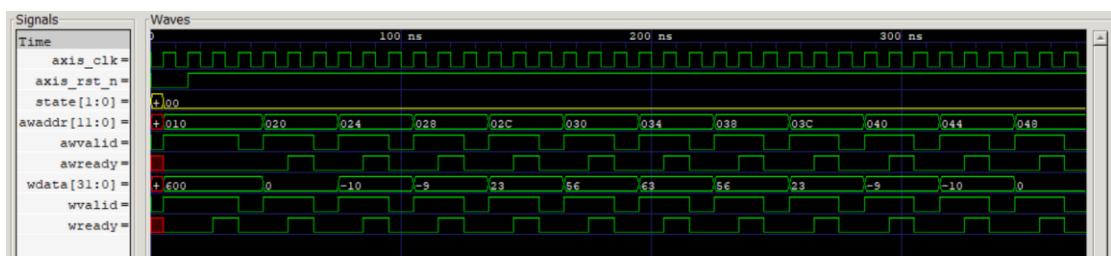
Operation system : Windows

Priod : 12ns

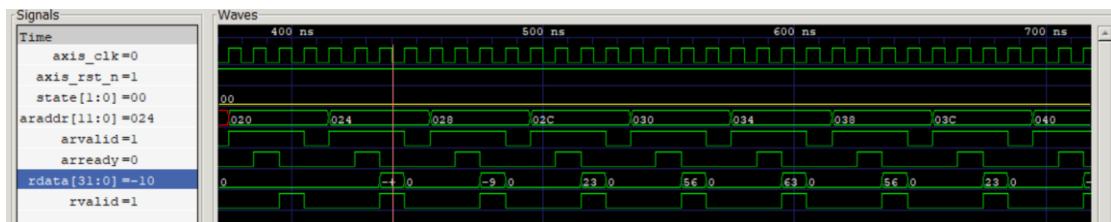


5. Simulation Waveform, show

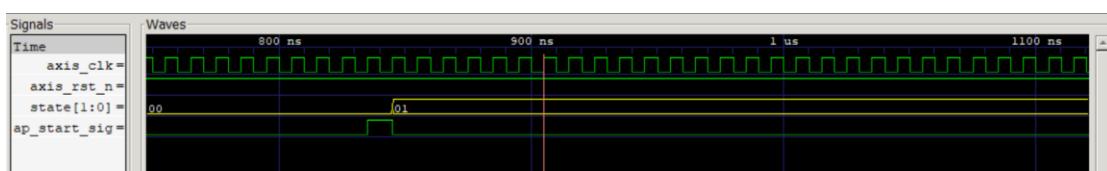
首先一開始 state 狀態為 ap_idle(2'b00) , 並開始的輸入 taps , 將它存在 RAM 。



- testbench 開始的檢查輸出的 taps 。

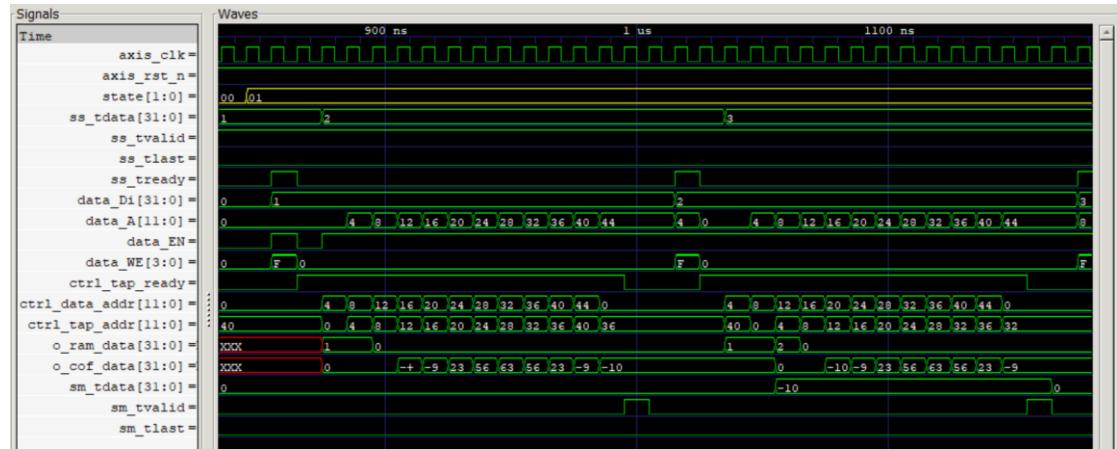


- 當訊號接收到 testbench 的 ap_start 時 , 將 ap_start_sig 改寫為 1 並且 state 狀態更改為 ap_start(2'b01) 。



- state 狀態為 ap_start(2'b01)後 , 會將 ss_tdata 寫入至 RAM ,

並且 $\text{ctrl_tap_ready} = 1$ ，ctrl 模組開始輸出對應的 tap_addr 與 data_addr ，之後從 RAM 讀出數值做相乘累加，輸出結果，且 sm_tvalid 訊號改寫為 1。



- 當 ss_tlast 狀態值為 1 以及 sm_tlast 狀態值為 1 後， state 狀態改寫為 $\text{ap_done}(2'b10)$ ，並且代表已經完成 fir 的運算結果。

