LUND UNIVERSITY

Design and Modeling of $In_XGa_{(1-X)}As/InP$ based Nanosheet Field Effect Transistors for High Frequency Applications

A Goal Document for a Master's Thesis Work

By

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2022

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Project start: 2022-02-10
Course Code: EITM02

1 Introduction

With the development of the semiconductor process, the Integrated Circuit design always needs to handle the balance between performance, power and area. The conventional CMOS technology could be operated at around $0.5V$ without loss of functionality and design robustness [1]. According to equations, a reduced operating voltage will result in lower power consumption. However, the lower operating voltage needs a lower threshold voltage, the short channel effect becoming more serious. Reduction of operating voltage need to compromise the switching speed as well. The relationship between power P_{active} and respond frequency has been shown in equations (1) and (2).

$$f = \alpha(V - V_T) \tag{1}$$

$$P_{active} = \alpha C_{eff} V^2 (V - V_T) + I_{leak} V \tag{2}$$

Where α is a constant depends on process technology, C_{eff} is the total effective load capacitance, V is the operating voltage, V_T is the threshold voltage, and I_{leak} is the leakage current due to the short channel effect. As far we know, the operating voltage can extremely affect the power of the device. Scaling down the transistor could lower the threshold voltage due to the gate width. It could also figure out the problem of operating voltage being too high.

To keep Moore's Law, people never stop to scale down the size of transistors. However, where the gate width is under 22nm, the planer structure cannot fulfill the requirements. The gate will not able to control the electrons due to the short channel effect. Foundries have created a new 3-Dimensional structure of Fin Field-Effect-Transistor (FinFET) which can stably control the electrons to continue Moore's Law. The same problem occurs where the Fin width is beneath 5nm. Reducing the Fin width further would result in a dramatic mobility loss due to quantum confinement and unacceptable threshold variation due to Fin width tolerances in the manufacturing process [2]. Under 5nm, the manufacturers have created two paths, Gate-All-Around Field-Effect-Transistor(GAAFET) and Multi-Bridge-Channel Field-Effect-Transistor (MBCFET). Figure 1 has shown the different structures of

transistors. After changing the structure, electron mobility becomes another serious problem.

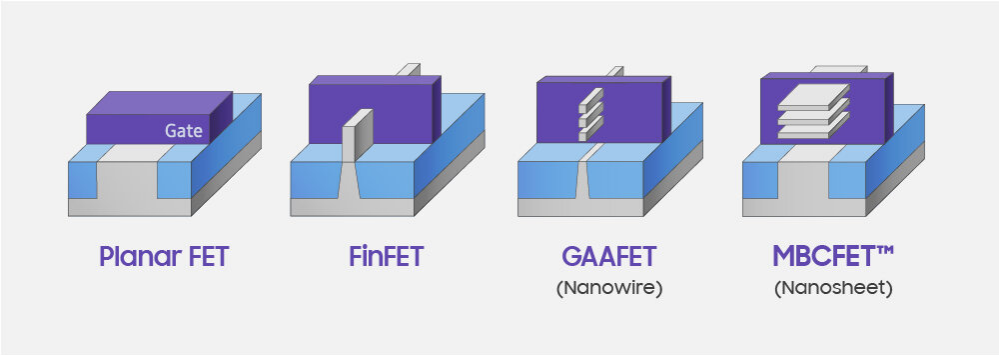

Figure 1 – Different structure of transistors. [3]

Metal-Oxide-Semiconductor Field-Effect-Transistor (MOSFET) scaling entered a phase of 'power-constrained scaling' as the power density dissipated by logic chips hit about $100W/cm^2$ [4]. The silicon-based transistor cannot meet the requirements in some scenarios. Lower electron mobility means lower performance and slower switching speed. The III-V compound semiconductors are a kind of high-electron-mobility transistors (HEMTs). In $InGaAs$ or $InAs$, the electron mobility is more than 10 times higher than in silicon at a comparable sheet density. The outstanding frequency response of III–V transistors is also frequently invoked [5]. Our project's main interest is in high-speed electronics, especially for millimeter-wave (mmW) applications due to their superior f_T/f_{max} [6].

$In_XGa_{1-X}As/InP$ based semiconductor is our main research target. Through stacking multiple Nanosheets in vertical, construct the transistor model by MATLAB and COMSOL to find a better structure in MBCFET.

2 Project Scope

Our Master's thesis work aims to explore the essential physics of stacked $InGaAs$ Nanosheet MOSFETs for RF applications with different geometries. Firstly, we intend to investigate the performance of ballistic 1D MOSFETs to capture the intrinsic characteristics such as current and capacitance. Truly ballistic devices are challenging to achieve in reality due to scattering in the channel. Therefore, modeling quasi-ballistic devices, devices with some amount of scattering, is preferred to obtain an accurate analysis of device performance. Based on the DC and RF performance of 1D ballistic nanotransistors, the 2D ballistic and quasi ballistic models at the end might be obtained.

Aiming for lower parasitic capacitance, the 3D finite element method (FEM) solver (COMSOL Multiphysics) will be used to obtain quantitative values of the extrinsic capacitance of the Nanosheet transistor unit cell. To obtain a deeper understanding of how the transistor structure is best optimized, different wire dimensions and separations, such as the number and the array of stacked sheets will be modeled in this thesis [7]. To further optimize the parameters that give minimized parasitic capacitance and thereby improved transistor performance, we will combine intrinsic and extrinsic modeling and estimate the high-frequency metrics such as f_T, f_{max} and microwave gains [8].

3 Approach and Methodology

The first step of the thesis will be to evaluate the electrostatic properties of ballistic transistors using MATLAB; this can be done by deriving the I-V characteristic. This thesis's simulations and numerical calculations will be mainly performed in the QCL(quantum capacitance limit) regime. The 2D ballistic and quasi ballistic currents will be calculated using the top of the barrier model [9]. The FET DC performance metrics such as trans-conductance (g_m), on-resistance (R_{on}) and output conductance (g_d) will be computed for various channel geometries and compositions.

The next step should be implementing the radio frequency (RF) simulation of Nanowire transistors. The device structure of Nanosheet transistors will be designed first using COMSOL. An optimized vertical FET layout will be used to emphasize the impact of parasitic capacitance and resistances on transistor performance. Essential metrics for transistors such as unity current gain frequency, f_T , and maximum power gain frequency, f_{max} are determined from the hybrid-π small-signal model. Scale the gate length to obtain a minimized intrinsic gate capacitance and high f_T and f_{max}. Finally, Y and Z parameters corresponding to the circuit elements will be derived to examine the transistor response under an AC input. To estimate these parameters, the two-port network is considered during the calculation.

4 Previous work

Research on III–V-based semiconductors started in the 1990s and has matured in the last two decades [10]- [12]. Recently, Nanosheet transistors have been brought to researchers' attention, and this is largely attributed to the following two reasons: good transport properties and excellent electrostatic scaling [13].

GAA Nanosheet devices are evaluated at the 7nm ground-rule [14] as a replacement of FinFET device architecture to enable further scaling down to the 5nm and 3nm nodes. In [15], Loubet, for the first time, demonstrates that the horizontally stacked gate-all-around (GAA) Nanosheet structure is a good candidate for the replacement of FinFET at the 5nm technology node and beyond. Another specific feature of stacked Nanosheet devices is the inner spacer that functions as the effective device spacer for self-aligned junction formation [16], which optimize the inner spacer thickness at 5nm with no degradation of the electrical performance.

Significant progress has been made on $GaAs$ metal-oxide-semiconductor field-effect transistors (MOSFETs) using atomic layer deposition (ALD)-grown Al_2O_3 as gate dielectric [17]. Since then, the III–V based indium gallium arsenide ($InGaAs$) transistors have become the leading interest for high-speed electronics, especially for millimeter-wave (mmW) applications due to their superior f_T/f_{max}. A record gm of $3.45mS/\mu m$ [18] has been reported for $InGaAs$ MOSFET for very-large-scale integration (VLSI) applications. [19] demonstrate the fabrication of $InGaAs$ MOSFET using the self-aligned sacrificial amorphous silicon (a:Si) to reduce parasitic capacitance further.

This work proposes a Nanosheet architecture based on $In_XGa_{1-X}As$ that utilizes MATLAB to understand ballistic transport model and COMSOL to achieve good RF performance.

5 Advancements and Outcome

The outcome of this thesis project is to construct the MBCFET or Nanosheet FETs (NS-FETs) model based on III-V compound materials with the purpose of Radio Frequency (RF).

Using MATLAB to construct a small-signal model of 1-D ballistic and 2-D ballistic transistor. Find the relationship between drain to source voltage and drain current in different scenarios of gate voltage. The intrinsic nanosheet FET performance will be estimated in quasi ballistic regime including short channel effects and DC metrics. The extrinsic part of the Nanosheet FET, especially the parasitic capacitors will be modeled in 3D COMSOL and the design will be optimised further to achiever lower parasitics. After reaching the basic target, the thermal problem will be the next target of the deeper research.

6 Resources

The software needed for the thesis project is mostly based on MATLAB and COMSOL. The Windows or Linux PC based workstations, placed in thesis workers' rooms, will be available for simulation and implementation.

7 Project Plan

The whole project can be divided into several smaller tasks. First, we will implement 1D ballistic modelling. On this basis, we will extract the intrinsic parameters such as current and capacitance using MATLAB. Then 2D and quasi ballistic modelling will be achieved to shape a more realistic simulation.

Then we analyse the extrinsic merits using COMSOL 3D electrostatic models in the second step. Designing the Nanosheet transistor aiming for lower parasitic capacitance. Next, optimization of wire dimensions and separations will be implemented. Finally, we combine intrinsic and extrinsic modelling to estimate the high frequency metrics such as f_T/f_{max} and microwave gains.

Considering our time is not much, we will emphasize quasi ballistic modelling and structure optimization. As for essay writing, we will start at the beginning of 3D electrostatic modelling to save time. To this end, the time plan is as follows.

Each milestone has been shown as below. The Gantt chart has been shown in figure 2.

- 1D-ballistic modelling(3.10-3.31).
- 2D-ballistic modelling(4.1-4.15)
- Quasi-ballistic modelling(4.16-4.30).
- COMSOL 3D electrostatic modelling(4.20-5.10)
- Optimization and comprehensive analysis of intrinsic and extrinsic merits(5.11-5.31)
- Essay writing(5.28-6.10)

If things go according to plan, we will finish our defense in June. Otherwise, We will revise our time plan based on our progress.

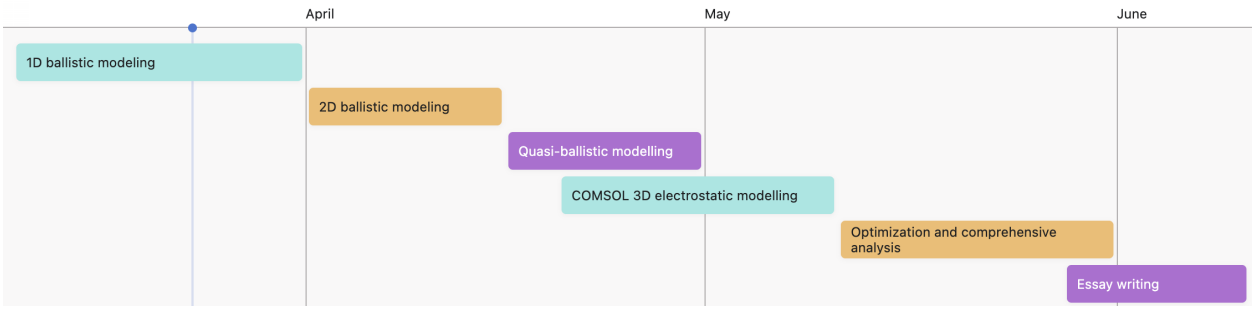

Figure 2 – The Gantt chart of master thesis project.

This goal document is approved by:

Main Supervisor	Examiner
Erik Lind	Mats Gustafsson

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