Computer Organization, Fall, 2013

Lab 4: Pipeline CPU

Due: 2013/12/23 11:59pm

Demo: 2013/12/26 & 27

1. Goal:

Modifying the CPU designed in lab3 and implementing a simple version pipelined CPU.

2. HW requirement:

a. Please use ModelSim or Xilinx as simulation platform.
b. Two people form a group. Must hand in one assignment for one group.
c. Pipe_Reg.v, Reg_File.v and Pipe_CPU_1.are supplied.
d. Must use the supplied Reg_File.v
e. In the top module, please change N to the value which is total lengths of input signal (include data and control) of pipeline register.

Pipe_Reg #(.size(N)) ID_EX

3. Requirement description:

a. Code (120%):

Basic instruction set (80%): Lab3 instruction, ADD, ADDI, SUB, AND, OR, SLT, SLTI, LW, SW, BEQ, MUL, and JUMP.

Advance (40%): Hazard Detection + Forwarding
Need to stall pipelined CPU if it detects load-use.
Need to forward data if instructions have data dependency.

b. Testbench:

Please use the tested pattern CO_P4_test_1.txt to test basic instruction, CO_P4_test_2.txt to test hazard detection and forwarding.

CO_P4_test_1.txt

```
Begin:
addi    $1, $0, 3;      // a = 3
addi    $2, $0, 4;      // b = 4
```

```
addi    $3, $0, 1;      // c = 1
sw      $1, 4($0);      // A[1] = 3
add     $4, $1, $1;     // $4 = 2a
or      $6, $1, $2;     // e = a | b
and     $7, $1, $3;     // f = a & c
sub     $5, $4, $2;     // d = 2a - b
slt     $8, $1, $2;     // g = a < b
beq     $s1, $2, begin
lw      $10, 4($0);     // i = A[1]
```

CO_P4_test_2.txt

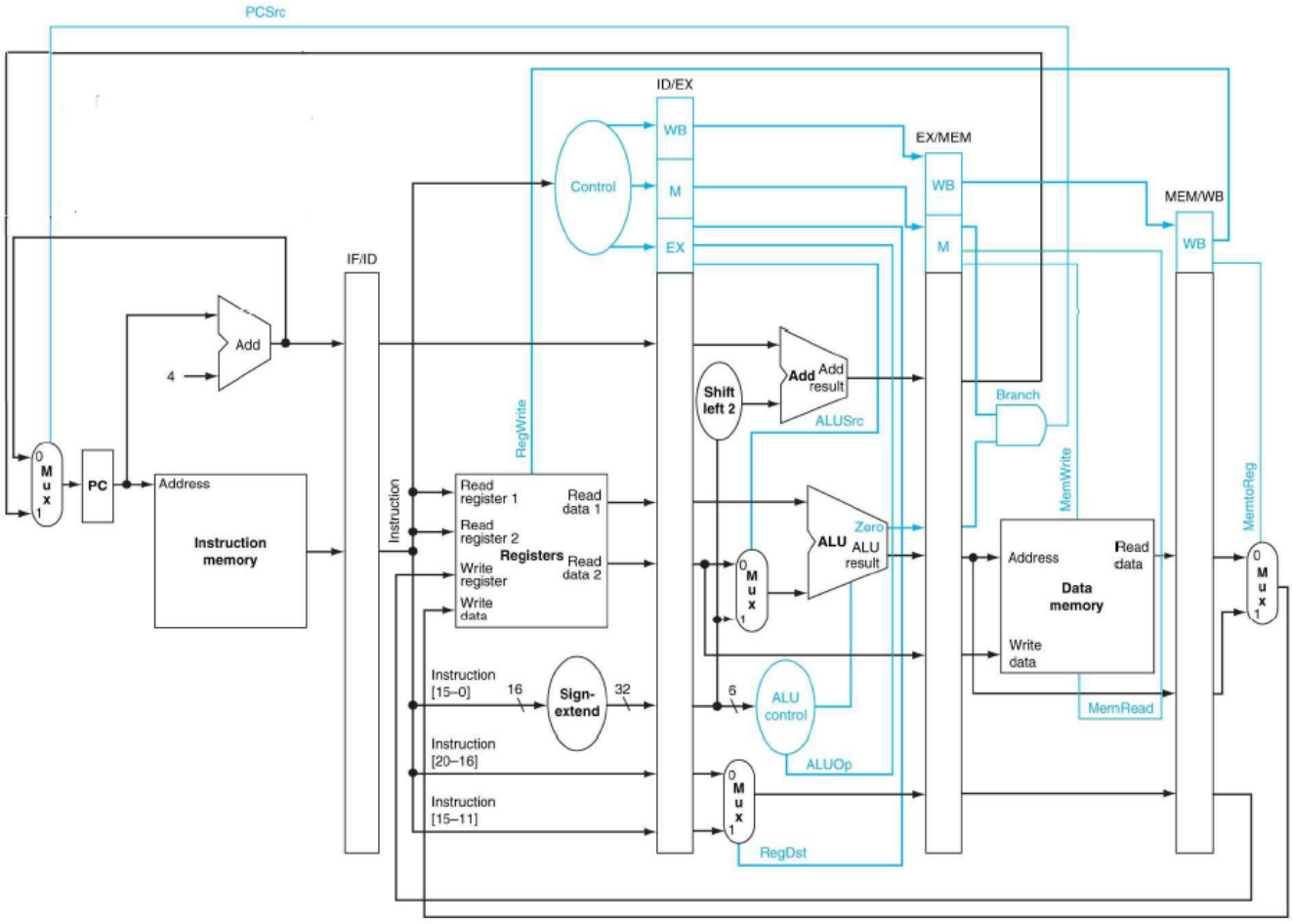
```
addi    $1, $0, 16
addi    $2, $1, 4
addi    $3, $0, 8
sw      $1, 4($0)
lw      $4, 4($0)
sub     $5, $4, $3
add     $6, $3, $1
addi    $7, $1, 10
and     $8, $7, $3
addi    $9, $0, 100
```

c. Report (20%):

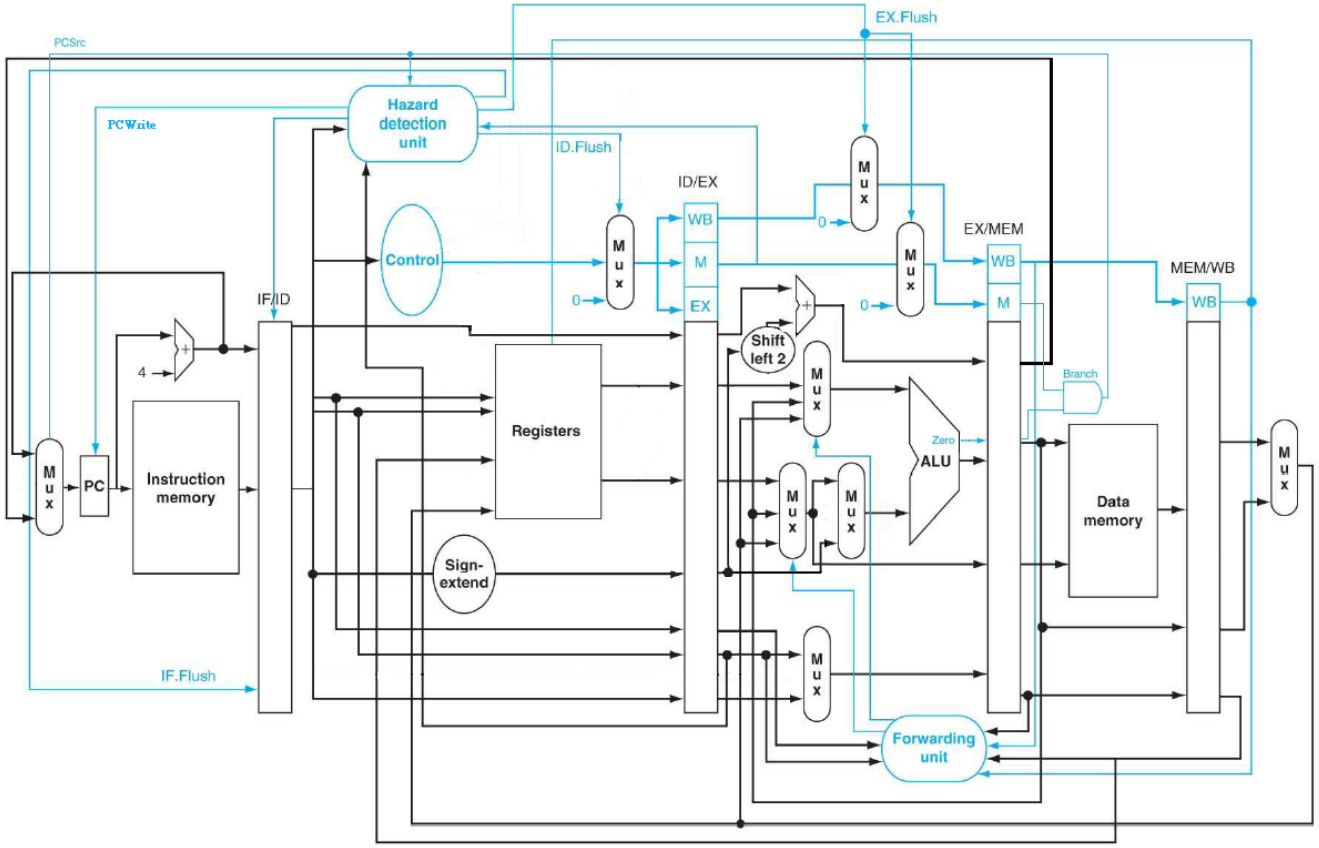
The context must include:

1. Source code and the note
2. Your architecture
3. Hardware module analysis
4. Finished part
5. Problems you met and solutions
6. Division of this work
7. Summary

4. Architecture (basic):



5. Architecture (advance):



6. Grade

a. Total score: 140% COPY WILL GET 0!

b. Basic score: 80%

c. Advance score: 40%

d. Report: 20%

e. Delay: 10% off / day

7. Hand in your Assignment

Please upload the assignment to the E3.

Put all of .v source files and report into same compressed file. (Use your student ID to be the name of your compressed file and must have the form of “student ID 1_student ID 2”. Ex. 0016001_0016002.rar)

8. Demo

Time: 2013/12/26 &27

Please review your code from lab 1 to lab 4. All the questions are relative to the labs. You will get a grade after the demo, and it will be one part of your lab score.

9. Q&A

If you have any question, use E3 discussion or just send email to TAs.