

# Register Map for the OpenHT

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M17 Project, May 2023

## 1 Control registers

### 1.1 Control register 1

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0x0000	SSB	MOD			IO0_SRC			RESERVED			PD	DEMOD			BAND	
0x0000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

Bits [1:0] – **BAND** – select operating band by using one of the DDR receivers

BAND	Value	Description
	0x0	sub-GHz (default)
	0x1	2.4 GHz
	0x2	invalid
	0x3	invalid

Bits [4:2] – **DEM0D** – select the demodulator

<b>DEM0D</b>	<b>Value</b>	<b>Description</b>
	<u>0x0</u>	FM (default)
	0x1	AM
	0x2	SSB
	0x3 to 0x7	reserved

Bit [5] – **PD** – Phase dithering for the FM transmitter submodule

<b>PD</b>	<b>Value</b>	<b>Description</b>
	<u>0x0</u>	phase dithering disabled (default)
	0x1	phase dithering enabled

Bits [8:6] – **RESERVED**

<b>RESERVED</b>	<b>Value</b>	<b>Description</b>
	<u>0x0</u>	-
	0x1 to 0x7	-

Bit [11:9] – **IO0\_SRC** – IO0 signal source mux

<b>IO0_SRC</b>	<b>Value</b>	<b>Description</b>
	<u>0x0</u>	logic low (default)
	0x1	<i>DRDY</i> signal
	0x2 to 0x7	reserved

Bits [14:12] – **MOD** – select modulation

MOD	Value	Description
	0x0	FM (default)
	0x1	AM
	0x2	SSB
	0x3 to 0x7	invalid

Bit [15] – **SSB**

SSB	Value	Description
	0x0	USB (default)
	0x1	LSB

1.2 Control register 2

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0x0001	-	-	-	-	-	-	-	FM_TX_W	CTCSS_TX						STATE	
0x0000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

Bits [1:0] – **STATE** – set the FPGA to one of the operating modes

<b>STATE</b>	<b>Value</b>	<b>Description</b>
	<u>0x0</u>	idle (default)
	0x1	<i>TX</i>
	0x2	<i>RX</i>
	0x3	reserved

Bits [7:2] – **CTCSS\_TX** – set the transmitter's CTCSS frequency (in hertz)

<b>CTCSS_TX</b>	<b>Value</b>	<b>Description</b>
	<u>0x00</u>	disabled (default)
	0x01	67.0
	0x02	69.3
	...	...
	0x3F	254.1

Bit [8] – **FM\_TX\_W** – set the frequency modulator's maximum deviation

<b>FM_TX_W</b>	<b>Value</b>	<b>Description</b>
	<u>0x0</u>	narrow, 12.5 kHz channel (default)
	0x1	wide, 25 kHz channel

**Note:** The actual maximum deviation is half the value from the table above.

Bits [15:9] – reserved.

**1.3 I branch offset null**

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
<b>0x0002</b>	MSB 16-bit signed integer LSB															
0x0000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

Signed 16-bit value to be added to the I branch after applying predistortion.

**1.4 Q branch offset null**

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
<b>0x0003</b>	MSB 16-bit signed integer LSB															
0x0000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

Signed 16-bit value to be added to the Q branch after applying predistortion.

**1.5 I branch linear gain**

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
<b>0x0004</b>	MSB 16-bit signed integer LSB															
0x4000	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

Signed, fixed-point, 16-bit gain value to be applied to the I branch. 0x4000 corresponds to +1.0 (default value).

**1.6 Q branch linear gain**

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
<b>0x0005</b>	MSB 16-bit signed integer LSB															
0x4000	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

Signed, fixed-point, 16-bit gain value to be applied to the Q branch. 0x4000 corresponds to +1.0 (default value).

**1.7 Digital predistortion register 1**

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
<b>0x0006</b>	MSB 16-bit signed integer LSB															
0x4000	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

Polynomial coefficient  $p_1$  value of the formula below:

$$D(x) = p_1 x + p_2 \operatorname{sgn}(x) x^2 + p_3 x^3$$

Signed, fixed-point value, where 0x4000 equals positive unity, “+1.0” (default value). This applies to all 3 registers holding the predistortion coefficients. To disable the predistortion, set  $p_1$  to 0x4000 (+1.0) and both  $p_2$  and  $p_3$  to 0x0000 (0.0).

**1.8 Digital predistortion register 2**

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
<b>0x0007</b>	MSB 16-bit signed integer LSB															
0x0000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

Polynomial coefficient  $p_2$  value. See 1.5 for details. Default value is 0x0000 (zero).

### 1.9 Digital predistortion register 3

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
<b>0x0008</b>	MSB 16-bit signed integer LSB															
0x0000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

Polynomial coefficient  $p_3$  value. See 1.5 for details. Default value is 0x0000 (zero).

## 2 Modulators

### 2.1 Modulation word

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
<b>0x0009</b>	MSB 16-bit signed/unsigned integer LSB															
0x0000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

Depending on the modulation scheme selected by the **MOD** subregister of **Control register 1** (0x0000), the contents are one of the following:

- frequency modulation - instantaneous frequency control word, signed
- amplitude modulation - instantaneous amplitude control word, unsigned
- SSB modulation baseband sample, signed

2.2 Reserved 1

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0x000A	RESERVED															
0x0000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

Instantaneous amplitude control word, unsigned.

2.3 Reserved 2

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0x000B	RESERVED															
0x0000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

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2.4 Reserved 3

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0x000C	RESERVED															
0x0000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

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3 Status registers

3.1 Status register 1

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0x000D	REV															
0x4854	0	1	0	0	1	0	0	0	0	1	0	1	0	1	0	0
	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Readback only register. This is mostly for fun or to check if the SPI comms are OK. Can be used to store revision number. The default **REV** value decodes to “HT”.

3.2 Status register 2

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0x000E	-	-	-	-	-	-	-	-	-	-	-	-	-	-	PLL1	PLL0
0x0000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Values in this register are reset to 0x0000 at start-up and get updated in realtime.

Bit [0] – **PLL0** – Phase locked loop lock flag (38, 64, 152 MHz clocks)

PLL0	Value	Description
	0x0	PLL unlocked (default)
	0x1	PLL locked

Bit [1] – **PLL1** – Phase locked loop lock flag (7.2 MHz sample rate generator master clock)

PLL1	Value	Description
	0x0	PLL unlocked (default)
	0x1	PLL locked

Bits [15:2] – reserved.

## 4 Demodulators and signal info

### 4.1 Demodulator register

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
<b>0x000F</b>	MSB 16-bit signed/unsigned integer LSB															
0x0000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Depending on the **DEMODO** subregister setting of **Control register 1**, the contents of this register are one of the following:

- frequency demodulator – frequency discriminator output, signed
- amplitude demodulator – signal's magnitude, unsigned
- SSB demodulator – baseband sample, signed

### 4.2 RSSI

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
<b>0x0010</b>	MSB 16-bit unsigned integer LSB															
0x0000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

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5 Debug, raw readback

5.1 I branch sample

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0x0011	16-bit signed integer															LSB
0x0000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Raw I branch sample, 16-bit, left justified, signed. Bits [2:0] are always zero.

5.2 Q branch sample

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0x0012	16-bit signed integer															LSB
0x0000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Raw Q branch sample, 16-bit, left justified, signed. Bits [2:0] are always zero.

## 6 Registers summary

Read/write register

Read-only register

Address	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Page(s)
0x0000	SSB	MOD			IO0_SRC			RESERVED			PD	DEM0D			BAND		tbf
0x0001	-	-	-	-	-	-	-	FM_TX_W	CTCSS_TX						STATE		tbf
0x0002	MSB							16-bit signed integer							LSB		tbf
0x0003	MSB							16-bit signed integer							LSB		tbf
0x0004	MSB							16-bit signed integer							LSB		tbf
0x0005	MSB							16-bit signed integer							LSB		tbf
0x0006	MSB							16-bit signed integer							LSB		tbf
0x0007	MSB							16-bit signed integer							LSB		tbf
0x0008	MSB							16-bit signed integer							LSB		tbf
0x0009	MSB							16-bit signed/unsigned integer							LSB		tbf
0x000A	RESERVED																tbf
0x000B	RESERVED																tbf
0x000C	RESERVED																tbf
0x000D	REV																tbf
0x000E	-	-	-	-	-	-	-	-	-	-	-	-	-	-	PLL1	PLL0	tbf
0x000F	MSB							16-bit signed/unsigned integer							LSB		tbf
0x0010	MSB							16-bit unsigned integer							LSB		tbf

0x0011	MSB	16-bit signed integer	LSB	<i>tb</i> <i>f</i>
0x0012	MSB	16-bit signed integer	LSB	<i>tb</i> <i>f</i>