Register Map for the OpenHT

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M17 Project, November 2023

FPGA revision 0.5

1 Glossary

AM	Amplitude Modulation
CTCSS	Continuous Tone Coded Squelch System
FIFO	First In, First Out (buffer type)
FIR	Finite Impulse Response (digital filter type)
FM	Frequency Modulation
IO	Input/Output
IQ	In-phase/Quadrature (complex signal representation)
LSB	Lower Sideband
MUX	Multiplexer
PM	Phase Modulation
RX	Receiver
SSB	Single Sideband
TRX	Transceiver
TX	Transmitter
USB	Upper Sideband

2 APB slaves list

Slave	Address	Description
SLV_COM	0	FPGA common settings
SLV_TX_COM	1	TX chain common settings
SLV_TX_FIR0	2	TX FIR pre-filter settings
SLV_TX_CTCSS	3	TX CTCSS settings
SLV_TX_FIR1	4	TX FIR stage 1 filter settings
SLV_TX_FIR2	5	TX FIR stage 2 filter settings
SLV_TX_FIR3	6	TX FIR stage 3 filter settings
SLV_TX_IQ_GAIN	7	TX IQ gain settings
SLV_TX_IQ_OFFSET	8	TX IQ offset nulling
SLV_RX_FIR0	9	RX FIR stage 1 FIR channel filter
SLV_RX_FIR1	10	RX FIR stage 2 FIR channel filter
SLV_RX_FIR2	11	RX FIR stage 3 FIR channel filter
SLV_RX_FIR3	12	RX FIR FIR post-filter

3 Slave control registers

3.1 Slave 0 – SLV_COM

Register	Address	Bits	Default	Description
VERSION	0	15..8	0x00	FPGA code version - major
		7..0	0x05	FPGA code revision - minor
STATUS	1	15..0	???	???
CTRL	2	15..4	???	???
		3..2	0x00	TRX band selection 0x00 – sub-gigahertz band 0x01 – 2.4 GHz band
		1..0	0x00	TRX state 0x00 – idle 0x01 – TX active 0x02 – RX active

IO	3	15..3	0x00	
		2..0	0x00	IO3 function select MUX 0x00 – global clock PLL lock flag 0x05 – TX FIFO “almost empty” flag
TX_FIFO	4	15..0	???	???
TX_FIFO_STS	5	15..0	???	???
RX_FIFO	6	15..0	???	???
RX_FIFO_STS	7	15..0	???	???

3.2 Slave 1 – SLV_TX_COM

Register	**Address**	**Bits**	**Default**	**Description**
CTRL	0	15..5	0x00	Reserved
		4	0x00	TX SSB sideband selector 0x00 – LSB 0x01 – USB
		3	0x00	TX FM bandwidth selector 0x00 – 12.5 kHz 0x01 – 25 kHz
		2..0	0x00	TX modulation selector 0x00 – FM 0x01 – AM 0x02 – SSB