M17

Connectors

File: conn.kicad_sch

- MCU_NRST
- PGOOD
- PB_INT
- MAIN_KILL
- SPK_P
- SPK_N
- RF_RST
- SW_CTL2
- SW_CTL1
- IRQ_AT86RF215
- IO0
- IO1
- IO2
- IO3
- IO4
- IO5
- IO6
- IO7
- INITN
- DONE
- PROGRAMN
- SPI_MISO
- SPI_MOSI
- SPI_SCK
- SPI_NSS1
- SPI_NSS2
- PTT

LS101
SP-1605
1
2

R101
1kR

C101
1uF

SW101
436351045816

GND
GND

Power supply

File: pwr.kicad_sch

- PWR_RESET
- PGOOD
- PB_INT
- MAIN_KILL

FPGA

File: fpga.kicad_sch

- IO0
- IO1
- IO2
- IO3
- IO4
- IO5
- IO6
- IO7
- INITN
- DONE
- PROGRAMN
- S_SPI_MISO
- S_SPI_MOSI
- S_SPI_CLK
- S_SPI_CS
- CLK_IN
- LVDS_TXCLK_P
- LVDS_TXCLK_N
- LVDS_TX_P
- LVDS_TX_N
- LVDS_RXCLK_P
- LVDS_RXCLK_N
- LVDS_RX09_P
- LVDS_RX09_N
- LVDS_RX24_P
- LVDS_RX24_N

LVDS (×8)

RF

File: rf.kicad_sch

- RESET
- SW_CTL2
- SW_CTL1
- AT86RF215_IRQ
- CLK_OUT
- LVDS_TXCLK_P
- LVDS_TXCLK_N
- LVDS_TX_P
- LVDS_TX_N
- LVDS_RXCLK_P
- LVDS_RXCLK_N
- LVDS_RX09_P
- LVDS_RX09_N
- LVDS_RX24_P
- LVDS_RX24_N
- S_SPI_MISO
- S_SPI_MOSI
- S_SPI_SCLK
- S_SPI_SELN

Authors: Wojciech SP5WWP, Leo Hofer, Morgan ON4MOD
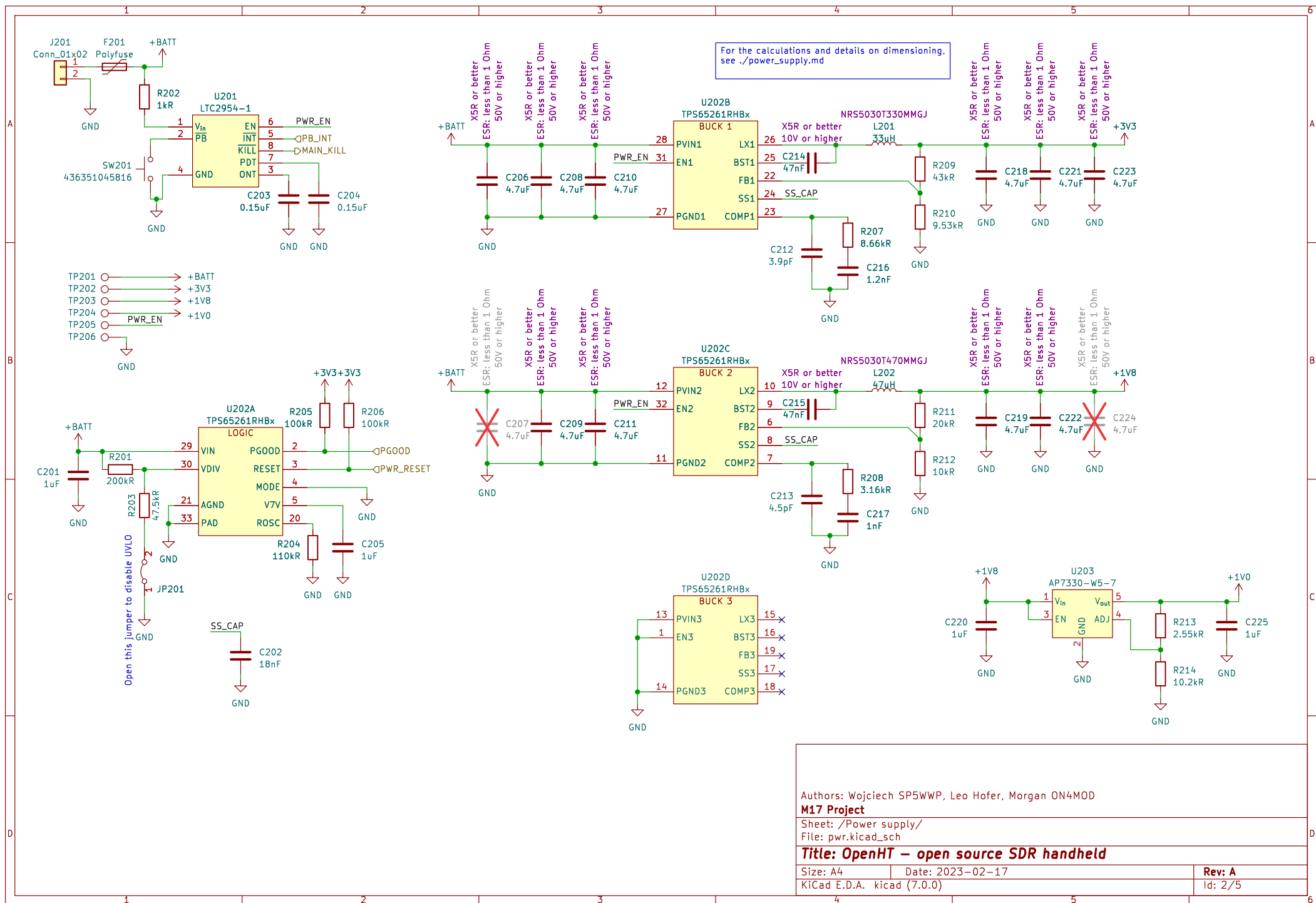
M17 Project

Sheet: /
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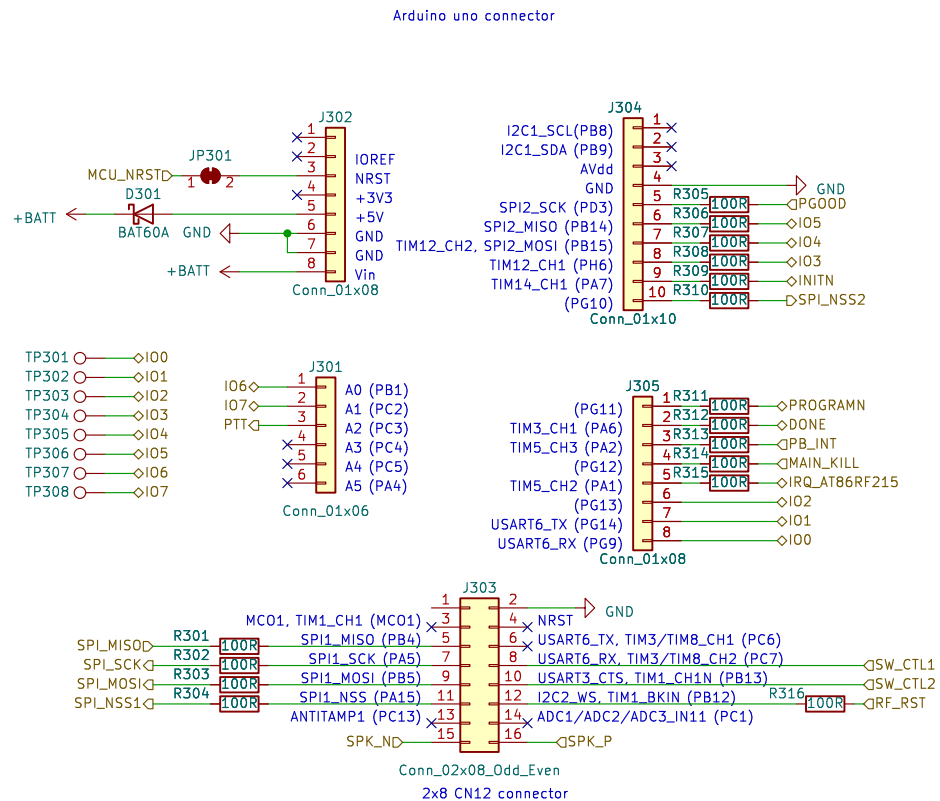
Title: OpenHT – open source SDR handheld

Size: A4 | Date: 2023-02-17 | **Rev: A**
KiCad E.D.A. kicad (7.0.0) | Id: 1/5

J201
Conn_01x02

F201
Polyfuse

+BATT

R202
1kR

GND

U201
LTC2954-1

Vin   EN   6   PWR_EN
PB   INT   5   PB_INT
       KILL 8   MAIN_KILL
       PDT   7
GND   ONT   3

SW201
436351045816

C203
0.15uF

C204
0.15uF

GND   GND

GND

TP201 +BATT
TP202 +3V3
TP203 +1V8
TP204 +1V0
TP205 PWR_EN
TP206

GND

+BATT

C201
1uF

GND

R201
200kR

R203
47.5kR

U202A
TPS65261RHBx
LOGIC

29 VIN   PGOOD 2
30 VDIV   RESET 3
           MODE   4
21 AGND   V7V   5
33 PAD   ROSC   20

+3V3 +3V3

R205   R206
100kR   100kR

PGOOD
PWR_RESET

GND

R204
110kR

C205
1uF

GND   GND

Open this jumper to disable UVLO

JP201

GND

SS_CAP

C202
18nF

GND

+BATT

X5R or better
ESR: less than 1 Ohm
50V or higher

C206   C208   C210
4.7uF   4.7uF   4.7uF

GND

PWR_EN

U202B
TPS65261RHBx
BUCK 1

28 PVIN1   LX1   26
31 EN1   BST1 25
            FB1   22
            SS1   24   SS_CAP
27 PGND1   COMP1 23

X5R or better
10V or higher

C214
47nF

NRS5030T330MMGJ
L201
33uH

R209
43kR

R210
9.53kR

GND

R207
8.66kR

C212
3.9pF

C216
1.2nF

GND

X5R or better
ESR: less than 1 Ohm
50V or higher

C218   C221   C223
4.7uF   4.7uF   4.7uF

GND   GND   GND

+3V3

For the calculations and details on dimensioning,
see ./power_supply.md

+BATT

X5R or better
ESR: less than 1 Ohm
50V or higher

C207   C209   C211
4.7uF   4.7uF   4.7uF

GND

PWR_EN

U202C
TPS65261RHBx
BUCK 2

12 PVIN2   LX2   10
32 EN2   BST2 9
            FB2   6
            SS2   8   SS_CAP
11 PGND2   COMP2 7

X5R or better
10V or higher

C215
47nF

NRS5030T470MMGJ
L202
47uH

R211
20kR

R212
10kR

GND

R208
3.16kR

C213
4.5pF

C217
1nF

GND

X5R or better
ESR: less than 1 Ohm
50V or higher

C219   C222   C224
4.7uF   4.7uF   4.7uF

GND   GND   GND

+1V8

U202D
TPS65261RHBx
BUCK 3

13 PVIN3   LX3   15
1   EN3   BST3 16
            FB3   19
            SS3   17
14 PGND3   COMP3 18

GND

+1V8

C220
1uF

GND

U203
AP7330-W5-7

1 Vin   Vout 5
3 EN   ADJ   4
2 GND

+1V0

R213
2.55kR

C225
1uF

GND

R214
10.2kR

GND

GND

Arduino uno connector

J302

Pin		Label
1		IOREF
2		NRST
3	MCU_NRST JP301 1—2	NRST
4		+3V3
5	+BATT D301 BAT60A	+5V
6	GND	GND
7		GND
8	+BATT	Vin

Conn_01x08

J304

	Pin		
I2C1_SCL(PB8)	1		
I2C1_SDA (PB9)	2		
AVdd	3		
GND	4	R305 100R	GND
SPI2_SCK (PD3)	5	R306 100R	PGOOD
SPI2_MISO (PB14)	6	R307 100R	IO5
TIM12_CH2, SPI2_MOSI (PB15)	7	R308 100R	IO4
TIM12_CH1 (PH6)	8	R309 100R	IO3
TIM14_CH1 (PA7)	9	R310 100R	INITN
(PG10)	10		SPI_NSS2

Conn_01x10

TP301 ⟶ IO0
TP302 ⟶ IO1
TP303 ⟶ IO2
TP304 ⟶ IO3
TP305 ⟶ IO4
TP306 ⟶ IO5
TP307 ⟶ IO6
TP308 ⟶ IO7

J301

	Pin	Label
IO6	1	A0 (PB1)
IO7	2	A1 (PC2)
PTT	3	A2 (PC3)
	4	A3 (PC4)
	5	A4 (PC5)
	6	A5 (PA4)

Conn_01x06

J305

	Pin		
(PG11)	1	R311 100R	PROGRAMN
TIM3_CH1 (PA6)	2	R312 100R	DONE
TIM5_CH3 (PA2)	3	R313 100R	PB_INT
(PG12)	4	R314 100R	MAIN_KILL
TIM5_CH2 (PA1)	5	R315 100R	IRQ_AT86RF215
(PG13)	6		IO2
USART6_TX (PG14)	7		IO1
USART6_RX (PG9)	8		IO0

Conn_01x08

J303

	Odd	Even	
	1	2	GND
MCO1, TIM1_CH1 (MCO1)	3	4	NRST
SPI_MISO R301 100R SPI1_MISO (PB4)	5	6	USART6_TX, TIM3/TIM8_CH1 (PC6)
SPI_SCK R302 100R SPI1_SCK (PA5)	7	8	USART6_RX, TIM3/TIM8_CH2 (PC7)
SPI_MOSI R303 100R SPI1_MOSI (PB5)	9	10	USART3_CTS, TIM1_CH1N (PB13) SW_CTL1
SPI_NSS1 R304 100R SPI1_NSS (PA15)	11	12	I2C2_WS, TIM1_BKIN (PB12) SW_CTL2
ANTITAMP1 (PC13)	13	14	ADC1/ADC2/ADC3_IN11 (PC1) R316 100R RF_RST
SPK_N	15	16	SPK_P

Conn_02x08_Odd_Even
2x8 CN12 connector

H301 M2.5
H302 M2.5
H303 M2.5
H304 M2.5

Authors: Wojciech SP5WWP, Leo Hofer, Morgan ON4MOD
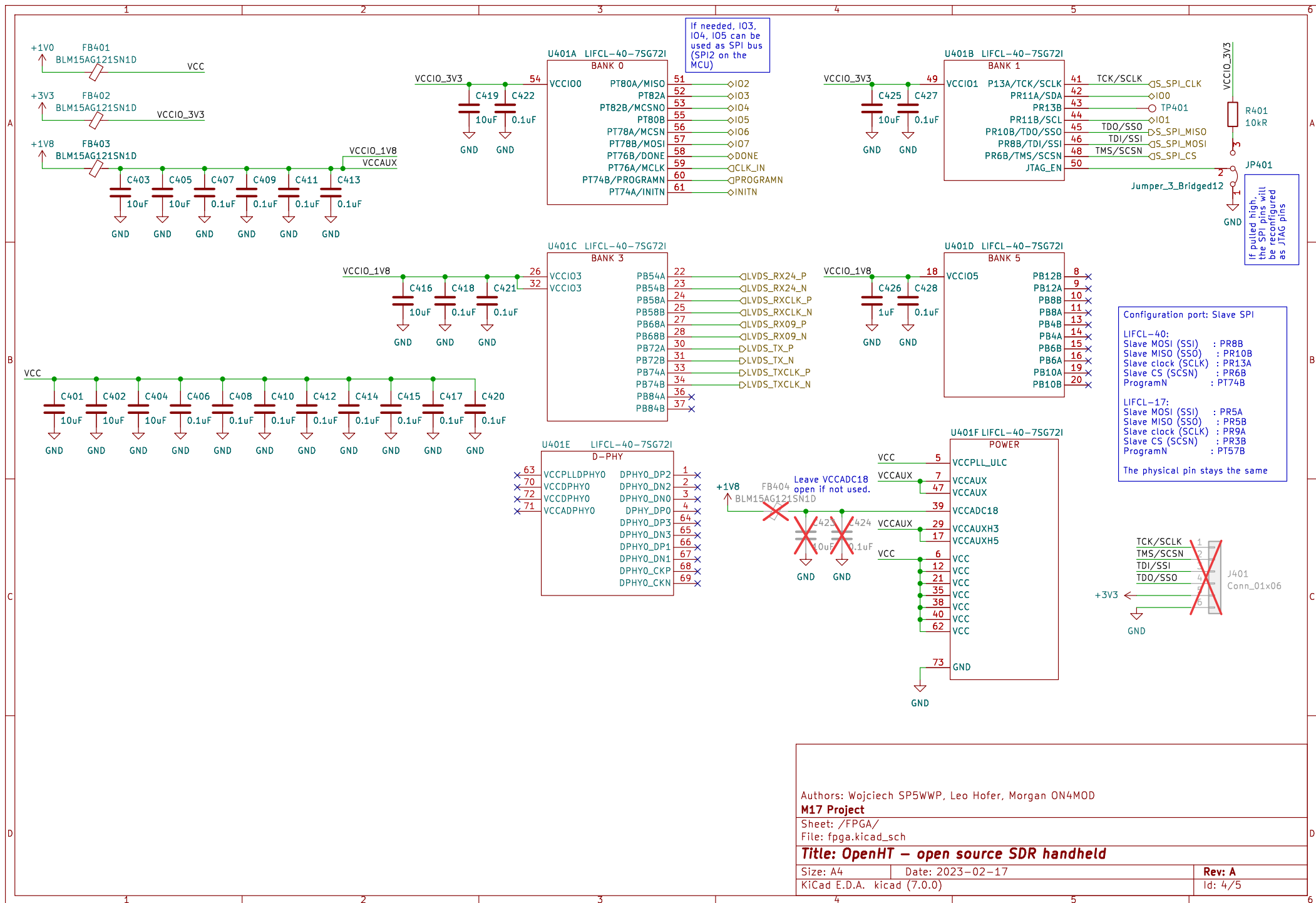**M17 Project**
Sheet: /Connectors/
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Title: OpenHT — open source SDR handheld
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KiCad E.D.A. kicad (7.0.0) | Id: 3/5

FPGA Schematic

If needed, IO3, IO4, IO5 can be used as SPI bus (SPI2 on the MCU)

U401A LIFCL-40-7SG72I — BANK 0

VCCIO_3V3 — 54 VCCIO0

Pin	Signal	Net
51	PT80A/MISO	IO2
52	PT82A	IO3
53	PT82B/MCSN0	IO4
55	PT80B	IO5
56	PT78A/MCSN	IO6
57	PT78B/MOSI	IO7
58	PT76B/DONE	DONE
59	PT76A/MCLK	CLK_IN
60	PT74B/PROGRAMN	PROGRAMN
61	PT74A/INITN	INITN

C419 10uF C422 0.1uF — GND

U401B LIFCL-40-7SG72I — BANK 1

VCCIO_3V3 — 49 VCCIO1

Pin	Signal	Net
41	P13A/TCK/SCLK	TCK/SCLK — S_SPI_CLK
42	PR11A/SDA	IO0
43	PR13B	TP401
44	PR11B/SCL	IO1
45	PR10B/TDO/SSO	TDO/SSO — S_SPI_MISO
46	PR8B/TDI/SSI	TDI/SSI — S_SPI_MOSI
48	PR6B/TMS/SCSN	TMS/SCSN — S_SPI_CS
50	JTAG_EN	

C425 10uF C427 0.1uF — GND

VCCIO_3V3 — R401 10kR

JP401 Jumper_3_Bridged12 — GND

If pulled high, the SPI pins will be reconfigured as JTAG pins

U401C LIFCL-40-7SG72I — BANK 3

VCCIO_1V8 — 26 VCCIO3 / 32 VCCIO3

Pin	Signal	Net
22	PB54A	LVDS_RX24_P
23	PB54B	LVDS_RX24_N
24	PB58A	LVDS_RXCLK_P
25	PB58B	LVDS_RXCLK_N
27	PB68A	LVDS_RX09_P
28	PB68B	LVDS_RX09_N
30	PB72A	LVDS_TX_P
31	PB72B	LVDS_TX_N
33	PB74A	LVDS_TXCLK_P
34	PB74B	LVDS_TXCLK_N
36	PB84A	
37	PB84B	

C416 10uF C418 0.1uF C421 0.1uF — GND

U401D LIFCL-40-7SG72I — BANK 5

VCCIO_1V8 — 18 VCCIO5

Pin	Signal
8	PB12B
9	PB12A
10	PB8B
11	PB8A
13	PB4B
14	PB4A
15	PB6B
16	PB6A
19	PB10A
20	PB10B

C426 1uF C428 0.1uF — GND

U401E LIFCL-40-7SG72I — D-PHY

Pin	Signal
63	VCCPLLDPHY0
70	VCCDPHY0
72	VCCDPHY0
71	VCCADPHY0
1	DPHY0_DP2
2	DPHY0_DN2
3	DPHY0_DN0
4	DPHY_DP0
64	DPHY0_DP3
65	DPHY0_DN3
66	DPHY0_DP1
67	DPHY0_DN1
68	DPHY0_CKP
69	DPHY0_CKN

U401F LIFCL-40-7SG72I — POWER

Pin	Signal
5	VCCPLL_ULC
7	VCCAUX
47	VCCAUX
39	VCCADC18
29	VCCAUXH3
17	VCCAUXH5
6	VCC
12	VCC
21	VCC
35	VCC
38	VCC
40	VCC
62	VCC
73	GND

VCC — VCCPLL_ULC
VCCAUX — VCCAUX
VCCAUX — VCCADC18
VCCAUX — VCCAUXH3 / VCCAUXH5
VCC — VCC

Leave VCCADC18 open if not used.

+1V8 — FB404 BLM15AG121SN1D (crossed out)
C423 10uF (crossed out) C424 0.1uF (crossed out) — GND

Power supply (left side)

+1V0 — FB401 BLM15AG121SN1D — VCC
+3V3 — FB402 BLM15AG121SN1D — VCCIO_3V3
+1V8 — FB403 BLM15AG121SN1D — VCCIO_1V8 / VCCAUX

C403 10uF, C405 10uF, C407 0.1uF, C409 0.1uF, C411 0.1uF, C413 0.1uF — GND

VCC —
C401 10uF, C402 10uF, C404 10uF, C406 0.1uF, C408 0.1uF, C410 0.1uF, C412 0.1uF, C414 0.1uF, C415 0.1uF, C417 0.1uF, C420 0.1uF — GND

Configuration port: Slave SPI

LIFCL-40:
Slave MOSI (SSI) : PR8B
Slave MISO (SSO) : PR10B
Slave clock (SCLK) : PR13A
Slave CS (SCSN)   : PR6B
ProgramN   : PT74B

LIFCL-17:
Slave MOSI (SSI) : PR5A
Slave MISO (SSO) : PR5B
Slave clock (SCLK) : PR9A
Slave CS (SCSN)   : PR3B
ProgramN   : PT57B

The physical pin stays the same

J401 Conn_01x06 (crossed out)

Pin	Signal
1	TCK/SCLK
2	TMS/SCSN
3	TDI/SSI
4	TDO/SSO
5	+3V3
6	GND

U501 — AT86RF215

Pin labels (top): S_SPI_SCLK, S_SPI_SELN, S_SPI_MOSI, S_SPI_MISO, LVDS_TXCLK_N, LVDS_TXCLK_P, LVDS_TX_N, LVDS_TX_P, LVDS_RX09_N, LVDS_RX09_P, LVDS_RXCLK_N, LVDS_RXCLK_P, LVDS_RX24_N, LVDS_RX24_P

Pins: 41 SCLK, 42 SELN, 43 MOSI, 44 MISO, 25 TXCLKN, 26 TXCLKP, 27 TXDN, 28 TXDP, 30 RXDN09, 31 RXDP09, 33 RXCLKN, 34 RXCLKP, 35 RXDN24, 36 RXDP24

- 40 IRQ — AT86RF215_IRQ
- 13 RSTN — RESET
- 22 CLKO
- 18 XTAL2 — R502 100k — GND
- 17 TCXO
- 37 DVDD
- 15 EVDD
- 46 EVDD
- 39 DEVDD
- 29 DEVDD
- 21 DEVDD
- 49 AVSS — GND
- 47 AVDD1 — C515 1uF — GND
- 1 FEA24, 2 FEB24 — J502 Conn_01x02
- 4 RFP24 — RF24_P, 5 RFN24 — RF24_N
- 8 RFP09 — RF09_P, 9 RFN09 — RF09_N
- 11 FEA09, 12 FEB09 — J503 Conn_01x02
- 14 AVDD0 — C514 1uF — GND

DVSS pins: 38, 32, 24, 23, 20 — GND
AVSS pins: 48, 45, 19, 16, 10, 7, 6, 3 — GND

DVSS and AVSS should be routed separately to the GND layer. Do not connect DVSS to exposed pad (see dev. board)

+3V3 — FB501 BLM15AG121SN1D — EVDD / DEVDD

X501 ECS-TXO-20CSMV: 4 VCC, 1 GND, 2 GND, 3 OUT
+3V3, C501 0.1uF

CLK_OUT — R503 220R — C516 2.2pF — GND
C504 1nF
R501 10kR, C506 10pF, C508 1uF

DEVDD — C517 0.1uF, C518 0.1uF, C519 0.1uF — GND
EVDD — C521 0.1uF, C520 0.1uF — GND

RF09_P / RF09_N — L503 ATB2012-50011 — C505 1nF C0G — C507 0.8pF C0G — FL501 LFCN-490+ (IN, OUT, GND) — C509 100pF C0G

RF24_P / RF24_N — C502 1.8pF C0G, C503 1.8pF C0G — L501 5.6nH — L502 2450FB15A050 (OUT1, NC, OUT2, IN, GND) DC_Feed/RF_GND — FL502 LFCN-2500+ (IN, OUT, GND) — C510 100pF C0G

SW501 RFSW8008: 6 RF2, 5 GND, 4 RF1, CTL1, CTL2, 1 CTL2, 2 ANT, 3 VDD — +3V3
SW_CTL1 — C511 220pF — GND
SW_CTL2 — C512 82pF — GND
C513 100pF — J501 Conn_Coaxial — GND