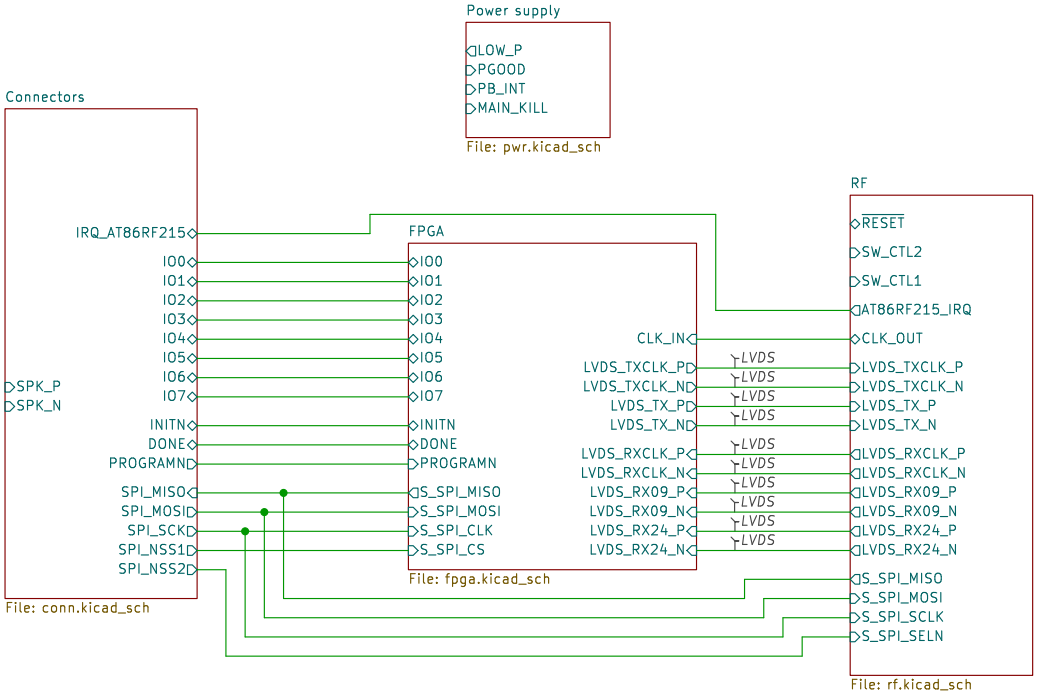

Authors: Wojciech SP5WWP, Leo Hofer, Morgan ON4MOD

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Sheet: /
File: OpenHT-RF.kicad_sch

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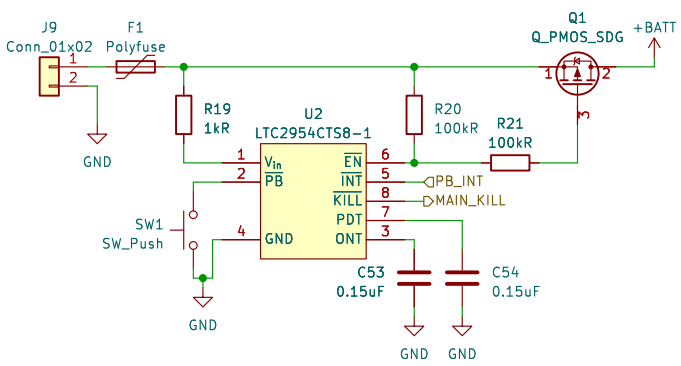
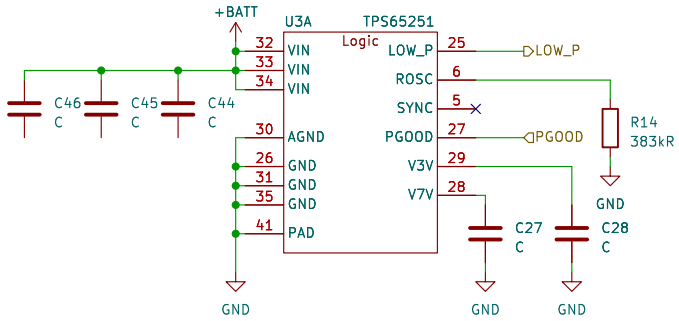


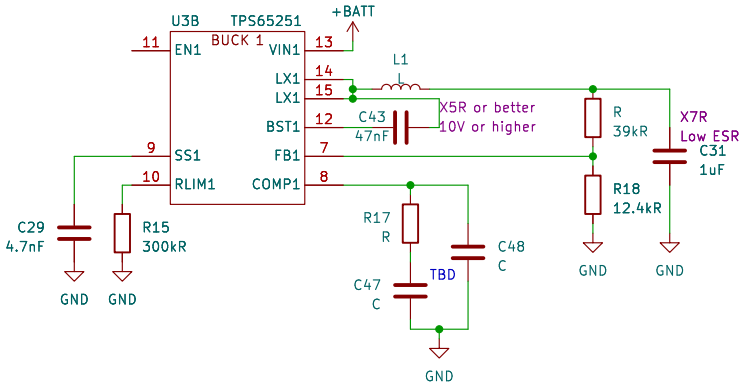
SS capacitors:
4.7nF corresponds to a soft start of about 1ms.
This value can be changed if we want to reduce the number of different components in the BOM

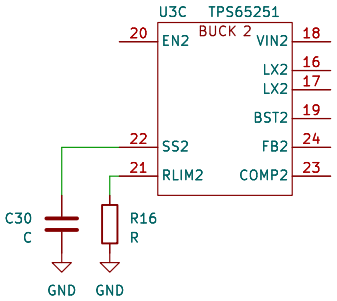


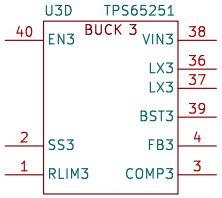
Buck 1:
L: optimised for V_{out} =3.3V, I_{out} =0.35A, f_{sw} =500kHz
C_{out} must be > 0.56uF (optimised for dV=30mV)
R_{lim} : set to max value (correspond to 1.2A)

Buck 2 has higher low-load efficiency and should thus be selected to provide the rail with the lesser load.

1.8V and 1.0V rails feed the FPGA. See with SP5WWP for the details on FPGA's current consumption







Authors: Wojciech SP5WWP, Leo Hofer, Morgan ON4MOD
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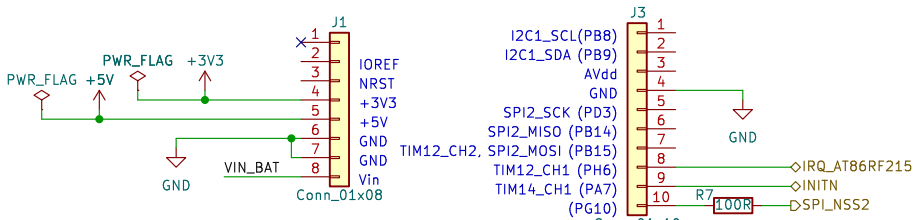
Arduino uno connector



2x8 CN12 connector

Authors: Wojciech SP5WWP, Leo Hofer, Morgan ON4MOD

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File: conn.kicad_sch

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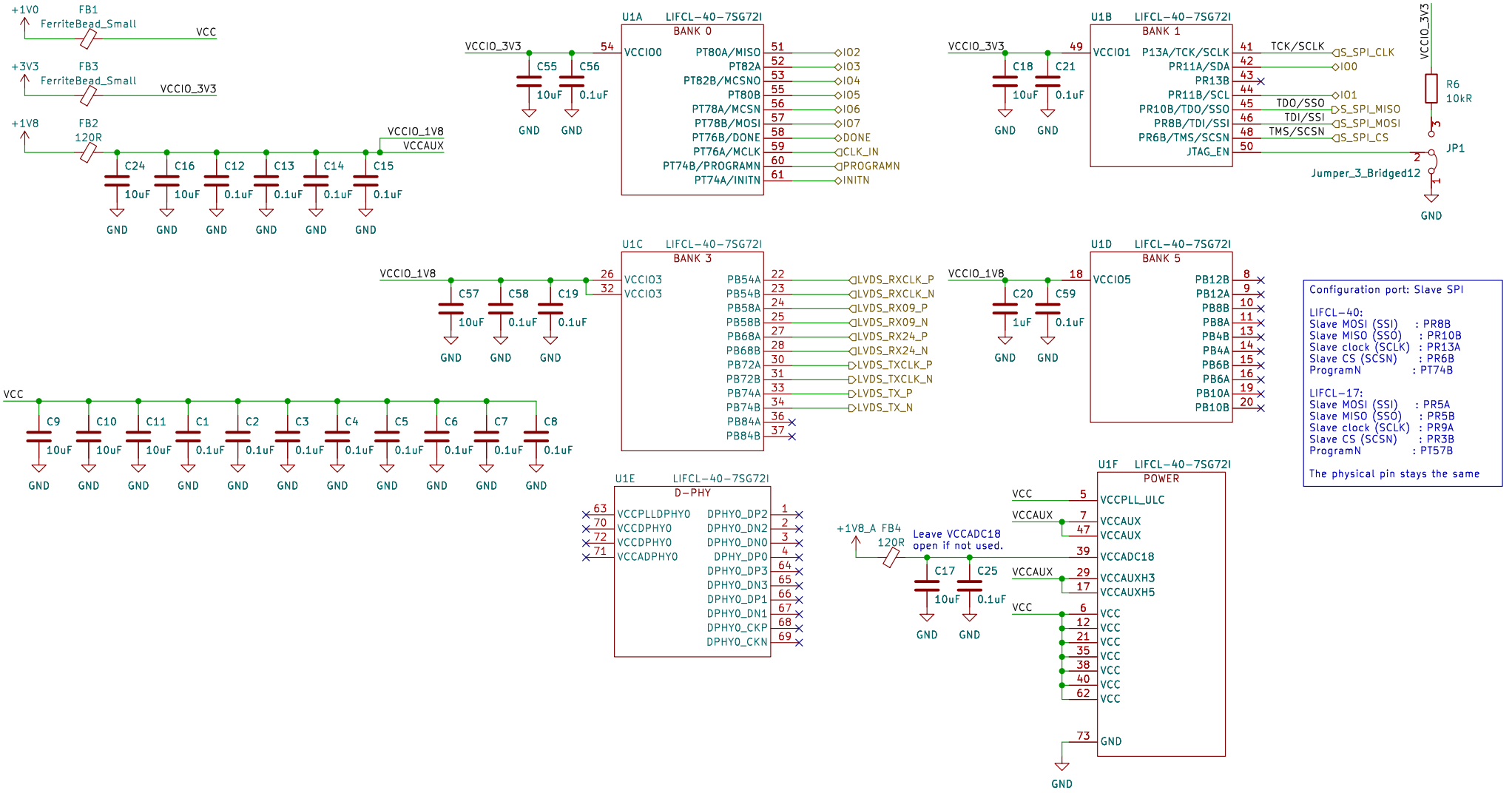
+1V0
FB1
FerriteBead_Small
VCC
+3V3
FB3
FerriteBead_Small
VCCIO_3V3
+1V8
FB2
120R
VCCIO_1V8
VCCAUX
C24 10uF
C16 10uF
C12 0.1uF
C13 0.1uF
C14 0.1uF
C15 0.1uF
GND
U1A LIFCL-40-7SG72I
BANK 0
VCCIO_3V3
54
VCCIO0
C55 10uF
C56 0.1uF
PT80A/MISO 51 IO2
PT82A 52 IO3
PT82B/MCSNO 53 IO4
PT80B 55 IO5
PT78A/MCSN 56 IO6
PT78B/MOSI 57 IO7
PT76B/DONE 58 DONE
PT76A/MCLK 59 CLK_IN
PT74B/PROGRAMN 60 PROGRAMN
PT74A/INITN 61 INITN
U1B LIFCL-40-7SG72I
BANK 1
VCCIO_3V3
49
VCCIO1
C18 10uF
C21 0.1uF
P13A/TCK/SCLK 41 TCK/SCLK S_SPI_CLK
PR11A/SDA 42 IO0
PR13B 43
PR11B/SCL 44 IO1
PR10B/TDO/SSO 45 TDO/SSO S_SPI_MISO
PR8B/TDI/SSI 46 TDI/SSI S_SPI_MOSI
PR6B/TMS/SCSN 48 TMS/SCSN S_SPI_CS
JTAG_EN 50
VCCIO_3V3
R6 10kR
JP1
Jumper_3_Bridged12
U1C LIFCL-40-7SG72I
BANK 3
VCCIO_1V8
26
32
VCCIO3
VCCIO3
C57 10uF
C58 0.1uF
C19 0.1uF
PB54A 22 LVDS_RXCLK_P
PB54B 23 LVDS_RXCLK_N
PB58A 24 LVDS_RX09_P
PB58B 25 LVDS_RX09_N
PB68A 27 LVDS_RX24_P
PB68B 28 LVDS_RX24_N
PB72A 30 LVDS_TXCLK_P
PB72B 31 LVDS_TXCLK_N
PB74A 33 LVDS_TX_P
PB74B 34 LVDS_TX_N
PB84A 36
PB84B 37
U1D LIFCL-40-7SG72I
BANK 5
VCCIO_1V8
18
VCCIO5
C20 1uF
C59 0.1uF
PB12B 8
PB12A 9
PB8B 10
PB8A 11
PB4B 13
PB4A 14
PB6B 15
PB6A 16
PB10A 19
PB10B 20
Configuration port: Slave SPI
LIFCL-40:
Slave MOSI (SSI) : PR8B
Slave MISO (SSO) : PR10B
Slave clock (SCLK) : PR13A
Slave CS (SCSN) : PR6B
ProgramN : PT74B
LIFCL-17:
Slave MOSI (SSI) : PR5A
Slave MISO (SSO) : PR5B
Slave clock (SCLK) : PR9A
Slave CS (SCSN) : PR3B
ProgramN : PT57B
The physical pin stays the same
VCC
C9 10uF
C10 10uF
C11 10uF
C1 0.1uF
C2 0.1uF
C3 0.1uF
C4 0.1uF
C5 0.1uF
C6 0.1uF
C7 0.1uF
C8 0.1uF
U1E LIFCL-40-7SG72I
D-PHY
63 VCCPLLDPHY0
70 VCCDPHY0
72 VCCDPHY0
71 VCCADPHY0
DPHY0_DP2 1
DPHY0_DN2 2
DPHY0_DN0 3
DPHY_DP0 4
DPHY0_DP3 64
DPHY0_DN3 65
DPHY0_DP1 66
DPHY0_DN1 67
DPHY0_CKP 68
DPHY0_CKN 69
+1V8_A FB4
120R
Leave VCCADC18 open if not used.
C17 10uF
C25 0.1uF
U1F LIFCL-40-7SG72I
POWER
VCC 5 VCCPLL_ULC
VCCAUX 7 VCCAUX
47 VCCAUX
39 VCCADC18
VCCAUX 29 VCCAUXH3
17 VCCAUXH5
VCC 6 VCC
12 VCC
21 VCC
35 VCC
38 VCC
40 VCC
62 VCC
73 GND
Authors: Wojciech SP5WWP, Leo Hofer, Morgan ON4MOD
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Sheet: /FPGA/
File: fpga.kicad_sch
Title: OpenHT – open source SDR handheld
Size: A4
Date: 2023-02-17
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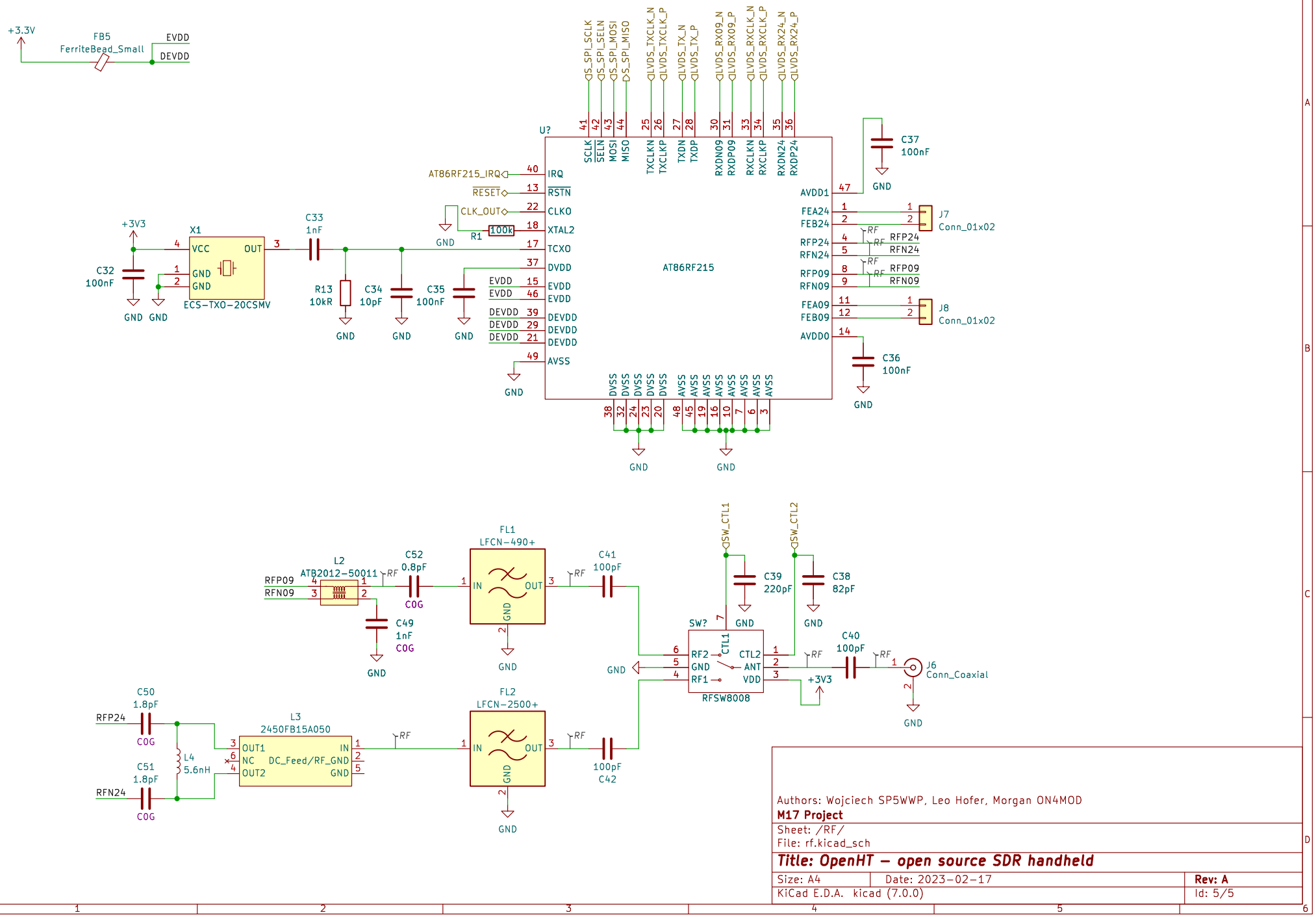

Authors: Wojciech SP5WWP, Leo Hofer, Morgan ON4MOD

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Sheet: /RF/

File: rf.kicad_sch

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