M17

Connectors
File: conn.kicad_sch

- MCU_NRST
- PGOOD
- PB_INT
- MAIN_KILL
- RF_RST
- SW_CTL2
- SW_CTL1
- IRQ_AT86RF215
- IO0
- IO1
- IO2
- IO3
- IO4
- IO5
- IO6
- FPGA_RST
- INITN
- DONE
- PROGRAMN
- SPI_MISO
- SPI_MOSI
- SPI_SCK
- SPI_NSS1
- SPI_NSS2
- SPK_P
- SPK_N
- PTT

LS101
SP-1605
1
2

R101
1kR

C101
1uF

SW101
436351045816

GND
GND

Power supply
File: pwr.kicad_sch

- PWR_RESET
- PGOOD
- PB_INT
- MAIN_KILL

FPGA
File: fpga.kicad_sch

- IO0
- IO1
- IO2
- IO3
- IO4
- IO5
- IO6
- FPGA_RST
- INITN
- DONE
- PROGRAMN
- S_SPI_MISO
- S_SPI_MOSI
- S_SPI_CLK
- S_SPI_CS
- CLK_IN
- LVDS_TXCLK_PD — LVDS
- LVDS_TXCLK_ND — LVDS
- LVDS_TX_PD — LVDS
- LVDS_TX_ND — LVDS
- LVDS_RXCLK_P — LVDS
- LVDS_RXCLK_N — LVDS
- LVDS_RX09_P — LVDS
- LVDS_RX09_N — LVDS
- LVDS_RX24_P — LVDS
- LVDS_RX24_N — LVDS

RF
File: rf.kicad_sch

- $\overline{RESET}$
- SW_CTL2
- SW_CTL1
- AT86RF215_IRQ
- CLK_OUT
- LVDS_TXCLK_P
- LVDS_TXCLK_N
- LVDS_TX_P
- LVDS_TX_N
- LVDS_RXCLK_P
- LVDS_RXCLK_N
- LVDS_RX09_P
- LVDS_RX09_N
- LVDS_RX24_P
- LVDS_RX24_N
- S_SPI_MISO
- S_SPI_MOSI
- S_SPI_SCLK
- S_SPI_SELN

Authors: Wojciech SP5WWP, Leo Hofer, Morgan ON4MOD
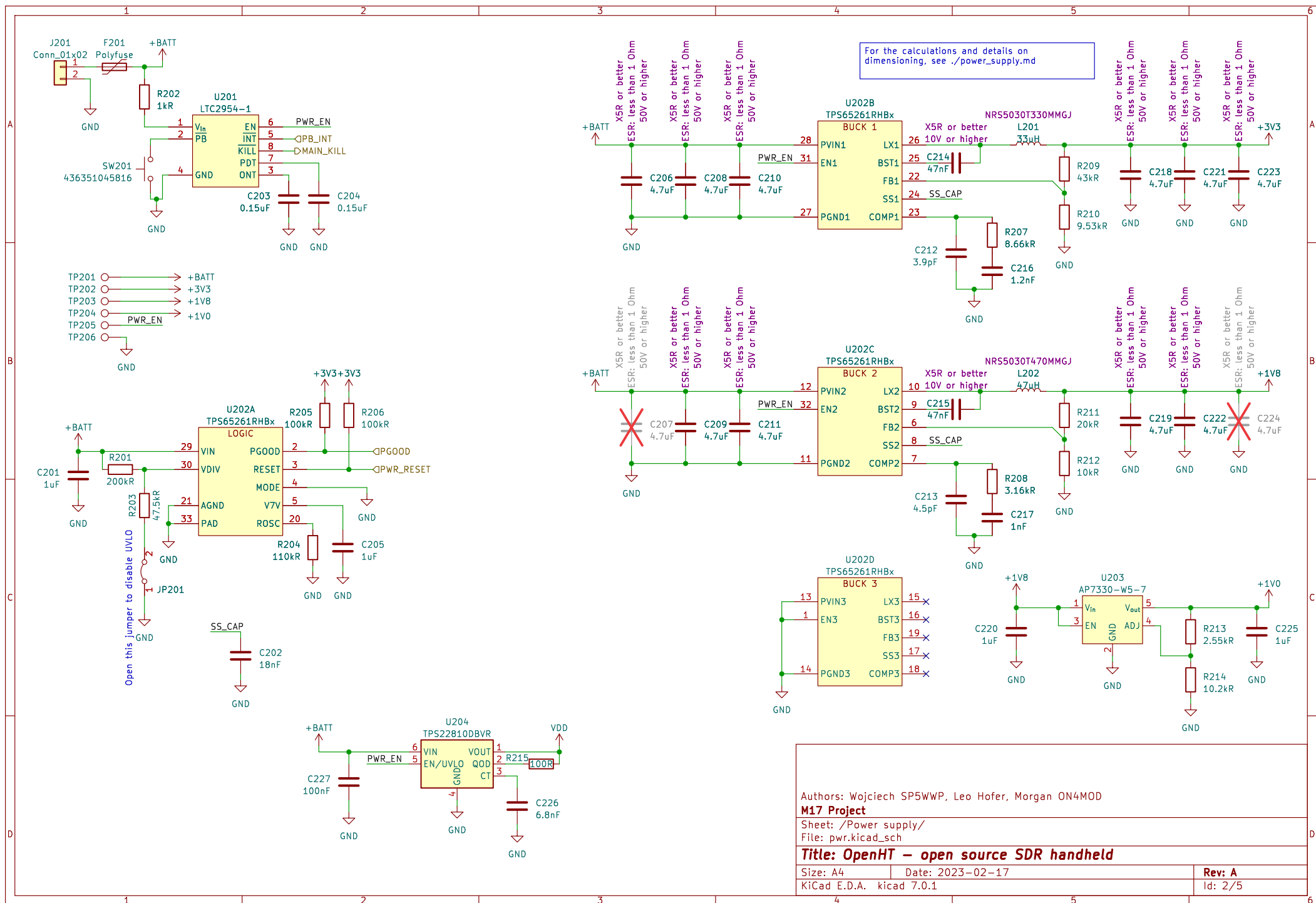
M17 Project
Sheet: /
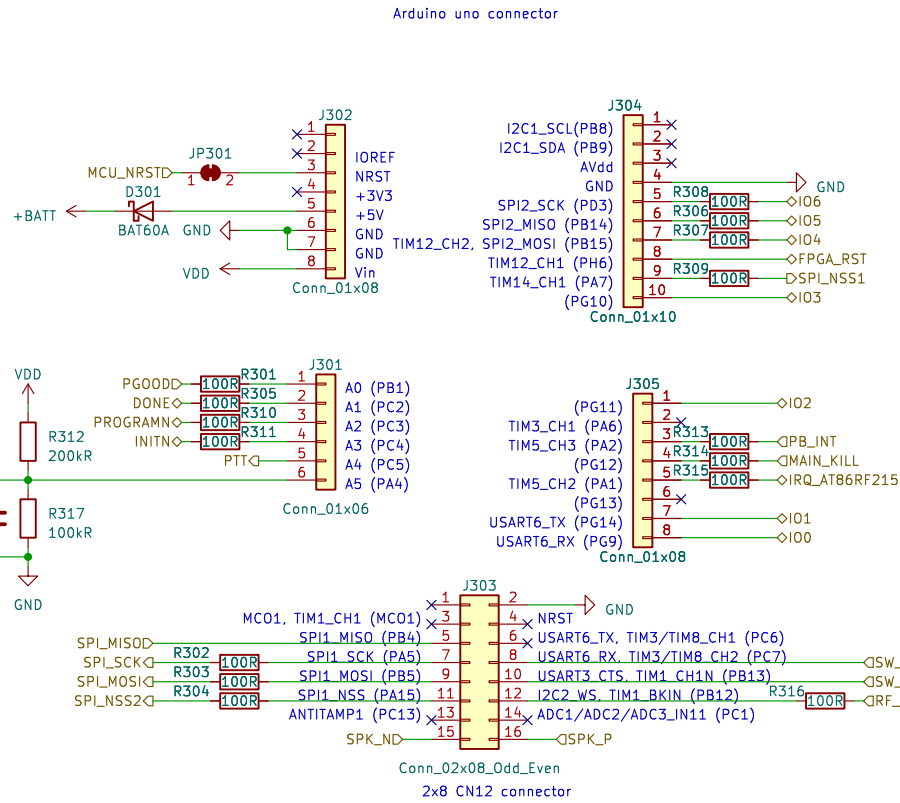File: OpenHT-RF.kicad_sch
Title: OpenHT — open source SDR handheld
Size: A4   Date: 2023-02-17   **Rev: A**
KiCad E.D.A. kicad 7.0.1   Id: 1/5

Power supply schematic

J201 Conn_01x02
F201 Polyfuse
+BATT
R202 1kR
GND

U201 LTC2954-1
- 1 Vin
- 2 PB
- 4 GND
- 6 EN — PWR_EN
- 5 INT — PB_INT
- 8 KILL — MAIN_KILL
- 7 PDT
- 3 ONT

SW201 436351045816

C203 0.15uF
GND
C204 0.15uF
GND

TP201 — +BATT
TP202 — +3V3
TP203 — +1V8
TP204 — +1V0
TP205 — PWR_EN
TP206 — GND

U202A TPS65261RHBx — LOGIC
- 29 VIN
- 30 VDIV
- 21 AGND
- 33 PAD
- 2 PGOOD — PGOOD
- 3 RESET — PWR_RESET
- 4 MODE
- 5 V7V
- 20 ROSC

+BATT
C201 1uF
GND
R201 200kR
R203 47.5kR
JP201
Open this jumper to disable UVLO
GND
GND

R205 100kR +3V3
R206 100kR +3V3

R204 110kR
C205 1uF
GND GND

SS_CAP
C202 18nF
GND

U204 TPS22810DBVR
- 6 VIN
- 2 EN/UVLO
- 4 GND
- 1 VOUT
- 5 QOD
- 3 CT

+BATT
PWR_EN
VDD
R215 100R
C227 100nF
GND
C226 6.8nF
GND
GND

For the calculations and details on dimensioning, see ./power_supply.md

U202B TPS65261RHBx — BUCK 1
- 28 PVIN1
- 31 EN1
- 27 PGND1
- 26 LX1
- 25 BST1
- 22 FB1
- 24 SS1
- 23 COMP1

+BATT
X5R or better / ESR: less than 1 Ohm / 50V or higher
C206 4.7uF
C208 4.7uF
C210 4.7uF
GND
PWR_EN

NRS5030T330MMGJ
L201 33uH
X5R or better / 10V or higher
C214 47nF
C212 3.9pF
R207 8.66kR
C216 1.2nF
GND
R209 43kR
R210 9.53kR
GND

+3V3
X5R or better / ESR: less than 1 Ohm / 50V or higher
C218 4.7uF
C221 4.7uF
C223 4.7uF
GND

U202C TPS65261RHBx — BUCK 2
- 12 PVIN2
- 32 EN2
- 11 PGND2
- 10 LX2
- 9 BST2
- 6 FB2
- 8 SS2
- 7 COMP2

+BATT
X5R or better / ESR: less than 1 Ohm / 50V or higher
C207 4.7uF
C209 4.7uF
C211 4.7uF
GND
PWR_EN

NRS5030T470MMGJ
L202 47uH
X5R or better / 10V or higher
C215 47nF
C213 4.5pF
R208 3.16kR
C217 1nF
GND
R211 20kR
R212 10kR
GND

+1V8
X5R or better / ESR: less than 1 Ohm / 50V or higher
C219 4.7uF
C222 4.7uF
C224 4.7uF
GND

U202D TPS65261RHBx — BUCK 3
- 13 PVIN3
- 1 EN3
- 14 PGND3
- 15 LX3
- 16 BST3
- 19 FB3
- 17 SS3
- 18 COMP3

GND

+1V8
C220 1uF
GND

U203 AP7330-W5-7
- 1 Vin
- 3 EN
- 2 GND
- 5 Vout
- 4 ADJ

R213 2.55kR
R214 10.2kR
GND
+1V0
C225 1uF
GND

Arduino uno connector

J302

Pin	Signal
1	IOREF
2	NRST
3	+3V3
4	+5V
5	GND
6	GND
7	GND
8	Vin

MCU_NRST — JP301 — 1 2
D301 BAT60A
+BATT
GND
VDD
Conn_01x08

J304

Pin	Signal
1	I2C1_SCL(PB8)
2	I2C1_SDA (PB9)
3	AVdd
4	GND
5	SPI2_SCK (PD3) — R308 100R — IO6
6	SPI2_MISO (PB14) — R306 100R — IO5
7	TIM12_CH2, SPI2_MOSI (PB15) — R307 100R — IO4
8	TIM12_CH1 (PH6) — FPGA_RST
9	TIM14_CH1 (PA7) — R309 100R — SPI_NSS1
10	(PG10) — IO3

GND
Conn_01x10

TP301 — IO0
TP302 — IO1
TP303 — IO2
TP304 — IO3
TP305 — IO4
TP306 — IO5
TP307 — IO6
TP308 — IO7

J301

VDD
PGOOD — R301 100R — 1 — A0 (PB1)
DONE — R305 100R — 2 — A1 (PC2)
PROGRAMN — R310 100R — 3 — A2 (PC3)
INITN — R311 100R — 4 — A3 (PC4)
5 — A4 (PC5)
PTT — 6 — A5 (PA4)

R312 200kR
C301 100nF
R317 100kR
GND
Conn_01x06

J305

Pin	Signal
1	(PG11) — IO2
2	TIM3_CH1 (PA6)
3	TIM5_CH3 (PA2) — R313 100R — PB_INT
4	(PG12) — R314 100R — MAIN_KILL
5	TIM5_CH2 (PA1) — R315 100R — IRQ_AT86RF215
6	(PG13)
7	USART6_TX (PG14) — IO1
8	USART6_RX (PG9) — IO0

Conn_01x08

J303

1	MCO1, TIM1_CH1 (MCO1)	2	GND
3		4	NRST
5	SPI1_MISO (PB4)	6	USART6_TX, TIM3/TIM8_CH1 (PC6)
7	SPI_MISO — R302 100R — SPI1_SCK (PA5)	8	USART6_RX, TIM3/TIM8_CH2 (PC7) — SW_CTL1
9	SPI_SCK — R303 100R — SPI1_MOSI (PB5)	10	USART3_CTS, TIM1_CH1N (PB13) — SW_CTL2
11	SPI_MOSI — R304 100R — SPI1_NSS (PA15)	12	I2C2_WS, TIM1_BKIN (PB12) — R316 100R — RF_RST
13	SPI_NSS2 — ANTITAMP1 (PC13)	14	ADC1/ADC2/ADC3_IN11 (PC1)
15	SPK_N	16	SPK_P

Conn_02x08_Odd_Even
2x8 CN12 connector

H301 M2.5
H302 M2.5
H303 M2.5
H304 M2.5

Authors: Wojciech SP5WWP, Leo Hofer, Morgan ON4MOD
M17 Project
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KiCad E.D.A. kicad 7.0.1   Id: 3/5

FPGA Schematic

Power rails (left)

- +1V0 — FB401 BLM15AG121SN1D → VCC
- +3V3 — FB402 BLM15AG121SN1D → VCCIO_3V3
- +1V8 — FB403 BLM15AG121SN1D → VCCIO_1V8, VCCAUX

C403 10uF, C405 10uF, C407 0.1uF, C409 0.1uF, C411 0.1uF, C413 0.1uF — GND

C401 10uF, C402 10uF, C404 10uF, C406 0.1uF, C408 0.1uF, C410 0.1uF, C412 0.1uF, C414 0.1uF, C415 0.1uF, C417 0.1uF, C420 0.1uF — VCC / GND

U401A LIFCL-40-7SG72I BANK 0

VCCIO_3V3 — C419 10uF, C422 0.1uF — GND

Pin	Signal	Net
54	VCCIO0	
51	PT80A/MISO	IO2
52	PT82A	IO3
53	PT82B/MCSNO	FPGA_RST
55	PT80B	IO4
56	PT78A/MCSN	IO5
57	PT78B/MOSI	IO6
58	PT76B/DONE	DONE
59	PT76A/MCLK	CLK_IN
60	PT74B/PROGRAMN	PROGRAMN
61	PT74A/INITN	INITN

If needed, IO4, IO5, IO6 can be used as SPI bus (SPI2 on the MCU)

U401B LIFCL-40-7SG72I BANK 1

VCCIO_3V3 — C425 10uF, C427 0.1uF — GND

Pin	Signal	Net
49	VCCIO1	
41	P13A/TCK/SCLK	TCK/SCLK → S_SPI_CLK
42	PR11A/SDA	IO1
43	PR13B	TP401
44	PR11B/SCL	IO0 / R402
45	PR10B/TDO/SSO	TDO/SSO → 100R → S_SPI_MISO
46	PR8B/TDI/SSI	TDI/SSI → S_SPI_MOSI
48	PR6B/TMS/SCSN	TMS/SCSN → S_SPI_CS
50	JTAG_EN	

VCCIO_3V3 — R401 10kR — JP401

If pulled high, the SPI pins will be reconfigured as JTAG pins

U401C LIFCL-40-7SG72I BANK 3

VCCIO_1V8 — C416 10uF, C418 0.1uF, C421 0.1uF — GND

Pin	Signal	Net
26	VCCIO3	
32	VCCIO3	
22	PB54A	LVDS_RX24_P
23	PB54B	LVDS_RX24_N
24	PB58A	LVDS_RXCLK_P
25	PB58B	LVDS_RXCLK_N
27	PB68A	LVDS_RX09_P
28	PB68B	LVDS_RX09_N
30	PB72A	LVDS_TX_P
31	PB72B	LVDS_TX_N
33	PB74A	LVDS_TXCLK_P
34	PB74B	LVDS_TXCLK_N
36	PB84A	
37	PB84B	

U401D LIFCL-40-7SG72I BANK 5

VCCIO_1V8 — C426 1uF, C428 0.1uF — GND

Pin	Signal
18	VCCIO5
8	PB12B
9	PB12A
10	PB8B
11	PB8A
13	PB4B
14	PB4A
15	PB6B
16	PB6A
19	PB10A
20	PB10B

U401E LIFCL-40-7SG72I D-PHY

Pin	Signal	Pin	Signal
63	VCCPLLDPHY0	1	DPHY0_DP2
70	VCCDPHY0	2	DPHY0_DN2
72	VCCDPHY0	3	DPHY0_DN0
71	VCCADPHY0	4	DPHY_DP0
		64	DPHY0_DP3
		65	DPHY0_DN3
		66	DPHY0_DP1
		67	DPHY0_DN1
		68	DPHY0_CKP
		69	DPHY0_CKN

U401F LIFCL-40-7SG72I POWER

Pin	Signal
5	VCCPLL_ULC (VCC)
7	VCCAUX
47	VCCAUX
39	VCCADC18
29	VCCAUXH3 (VCCAUX)
17	VCCAUXH5
6	VCC
12	VCC
21	VCC
35	VCC
38	VCC
40	VCC
62	VCC
73	GND

+1V8 — FB404 BLM15AG121SN1D — C423 10uF, C424 0.1uF (crossed out)

Leave VCCADC18 open if not used.

Configuration port: Slave SPI

LIFCL-40:
- Slave MOSI (SSI) : PR8B
- Slave MISO (SSO) : PR10B
- Slave clock (SCLK) : PR13A
- Slave CS (SCSN)   : PR6B
- ProgramN   : PT74B

LIFCL-17:
- Slave MOSI (SSI) : PR5A
- Slave MISO (SSO) : PR5B
- Slave clock (SCLK) : PR9A
- Slave CS (SCSN)   : PR3B
- ProgramN   : PT57B

The physical pin stays the same

J401 Conn_01x06 (crossed out)

Pin	Signal
1	TCK/SCLK
2	TMS/SCSN
3	TDI/SSI
4	TDO/SSO
5	+3V3
6	GND

+3V3

FB501
BLM15AG121SN1D

EVDD
DEVDD

LVDS_TXCLK_N
LVDS_TXCLK_P
LVDS_TX_N
LVDS_TX_P
LVDS_RX09_N
LVDS_RX09_P
LVDS_RXCLK_N
LVDS_RXCLK_P
LVDS_RX24_N
LVDS_RX24_P

S_SPI_SCLK
S_SPI_SELN
S_SPI_MOSI
S_SPI_MISO

R504 100R

U501

41	SCLK
42	SELN
43	MOSI
44	MISO
25	TXCLKN
26	TXCLKP
27	TXDN
28	TXDP
30	RXDN09
31	RXDP09
33	RXCLKN
34	RXCLKP
35	RXDN24
36	RXDP24

R503
220R

CLK_OUT

C516
2.2pF

AT86RF215_IRQ
RESET

40	IRQ
13	RSTN
22	CLKO
18	XTAL2
17	TCXO
37	DVDD
15	EVDD
46	EVDD
39	DEVDD
29	DEVDD
21	DEVDD
49	AVSS

GND   R502 100k   GND

+3V3

X501
4 VCC   OUT 3
1 GND
2 GND
ECS-TXO-20CSMV

C501
0.1uF

GND GND

C504
1nF

GND

R501
10kR

C506
10pF

C508
1uF

GND   GND   GND

AT86RF215

AVDD1 47
FEA24 1
FEB24 2
RFP24 4   RF24_P
RFN24 5   RF24_N
RFP09 8   RF09_P
RFN09 9   RF09_N
FEA09 11
FEB09 12
AVDD0 14

C515
1uF
GND

J502
Conn_01x02

J503
Conn_01x02

C514
1uF
GND

DEVDD

C517   C518   C519
0.1uF 0.1uF 0.1uF

GND   GND   GND

EVDD

C521   C520
0.1uF 0.1uF

GND   GND

38	DVSS
32	DVSS
24	DVSS
23	DVSS
20	DVSS
48	AVSS
45	AVSS
19	AVSS
16	AVSS
10	AVSS
7	AVSS
6	AVSS
3	AVSS

GND

DVSS and AVSS should be routed separately to the GND layer. Do not connect DVSS to exposed pad (see dev. board)

GND   GND

C502   1.8pF   C0G
RF24_N   500hm_Diff   500hm_Diff
C503   1.8pF   C0G
RF24_P   500hm_Diff   500hm_Diff

L501
5.6nH

L502
2450FB15A050
3 OUT1   IN 1
6 NC   DC_Feed/RF_GND
4 OUT2   GND 5
GND

FL502
LFCN-2500+
IN 1   OUT 3
GND 2
GND

500hm   500hm   C0G   500hm
C510
100pF

QSW_CTL1   QSW_CTL2

C511
220pF
GND

C512
82pF
GND

SW501
6 RF2   CTL2 1
5 GND   ANT
4 RF1   VDD 3
CTL1
RFSW8008

C513
100pF
500hm   500hm

J501
EMPCB.CSMAFSTJ.A
GND

+3V3

L503
ATB2012-50011
4   1
3   2
RF09_P   500hm_Diff
RF09_N   500hm_Diff

C505
1nF
C0G
GND

C507
0.8pF
C0G
500hm   500hm

FL501
LFCN-490+
IN 1   OUT 3
GND 2
GND

500hm   C0G   500hm
C509
100pF

GND

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