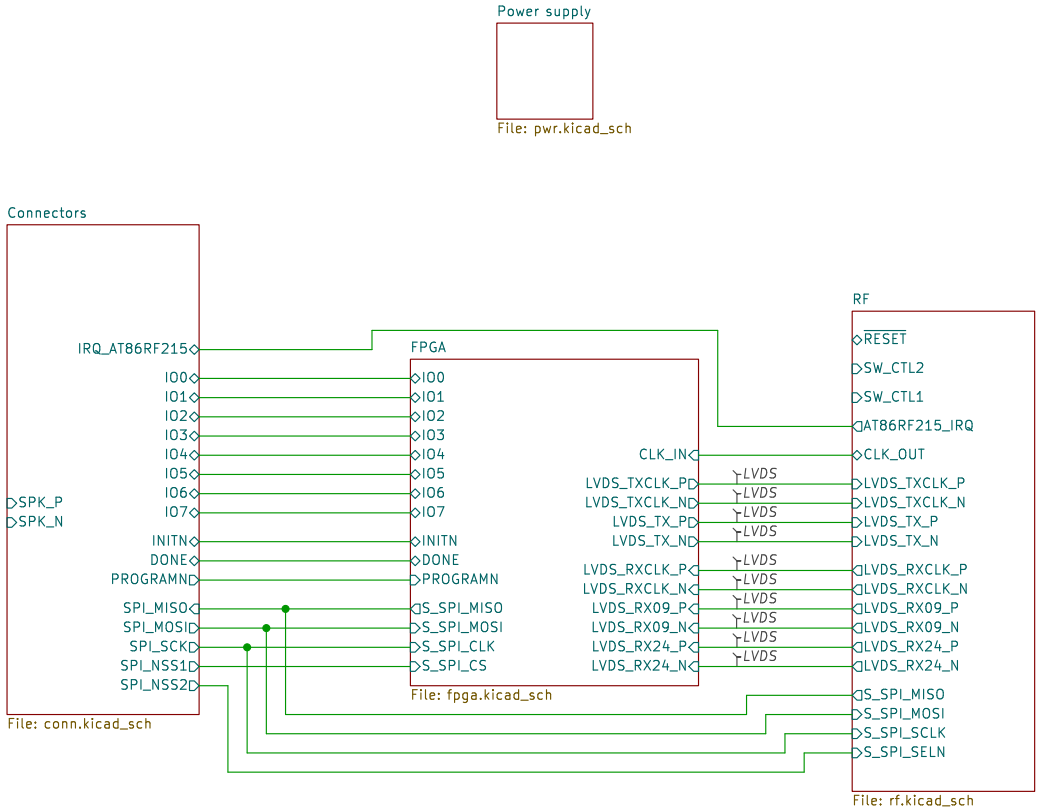

Authors: Wojciech SP5WWP, Leo Hofer, Morgan ON4MOD

M17 Project

Sheet: /

File: OpenHT-RF.kicad_sch

Title: OpenHT – open source SDR handheld

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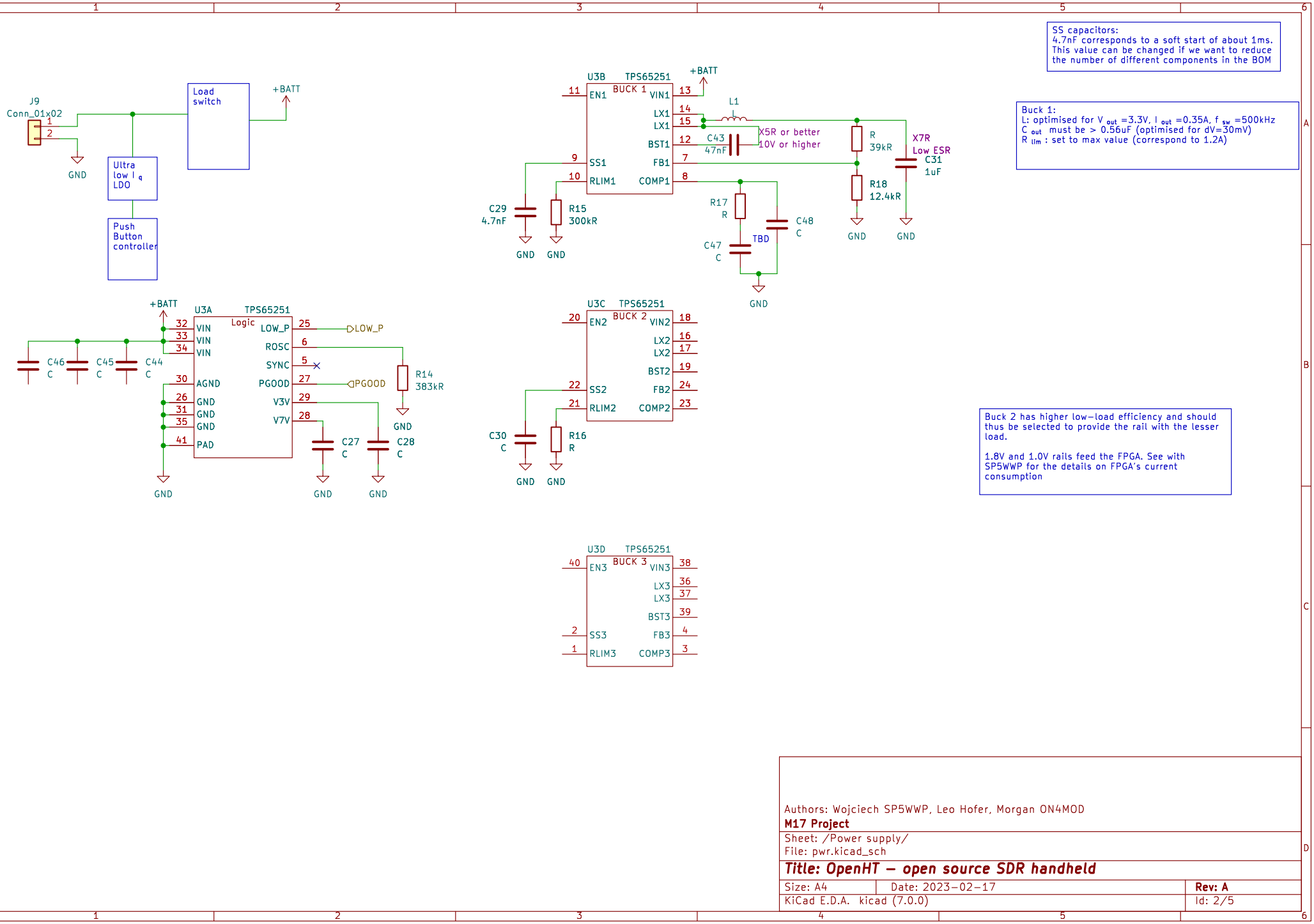
SS capacitors:
4.7nF corresponds to a soft start of about 1ms.
This value can be changed if we want to reduce the number of different components in the BOM
Buck 1:
L: optimised for V out =3.3V, I out =0.35A, f sw =500kHz
C out must be > 0.56uF (optimised for dV=30mV)
R lim : set to max value (correspond to 1.2A)
Buck 2 has higher low-load efficiency and should thus be selected to provide the rail with the lesser load.
1.8V and 1.0V rails feed the FPGA. See with SP5WWP for the details on FPGA's current consumption
J9
Conn_01x02
Load switch
+BATT
Ultra low I q LDO
Push Button controller
GND
U3A
TPS65251
Logic
U3B
BUCK 1
U3C
BUCK 2
U3D
BUCK 3
L1
X5R or better
10V or higher
C43
47nF
R
39kR
X7R
Low ESR
C31
1uF
R18
12.4kR
C29
4.7nF
R15
300kR
R17
R
C48
C
C47
C
TBD
R14
383kR
C46
C
C45
C
C44
C
C27
C
C28
C
C30
C
R16
R
LOW_P
PGOOD
Authors: Wojciech SP5WWP, Leo Hofer, Morgan ON4MOD
M17 Project
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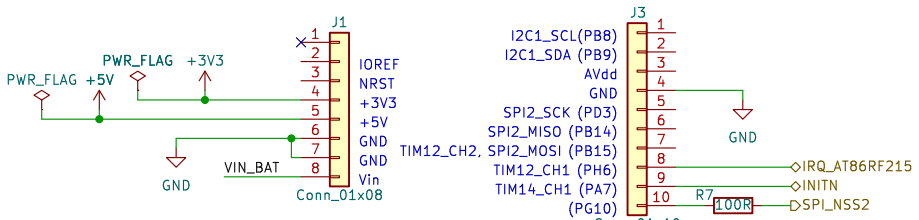
Arduino uno connector



2x8 CN12 connector

Authors: Wojciech SP5WWP, Leo Hofer, Morgan ON4MOD

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Title: OpenHT – open source SDR handheld

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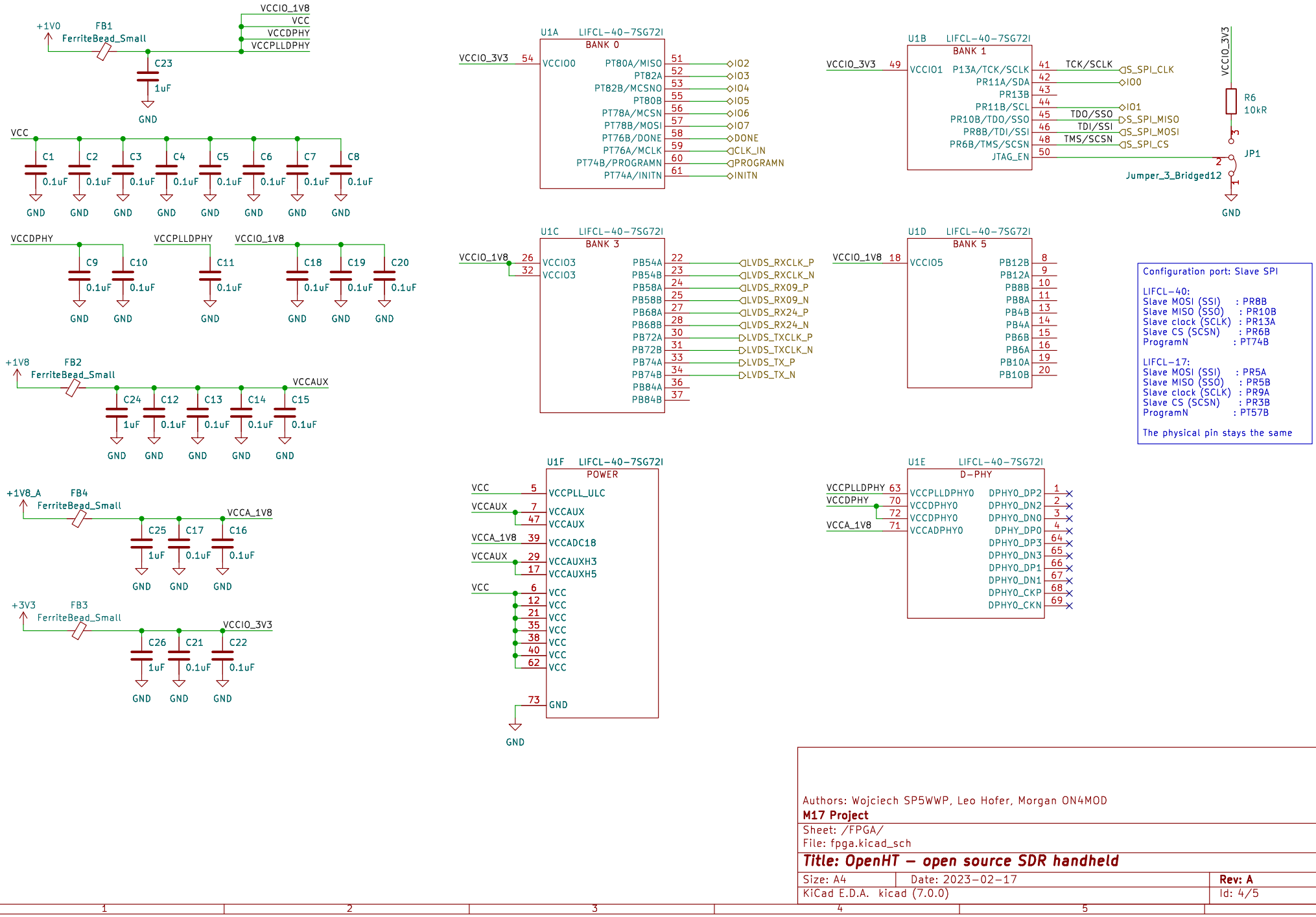
+1V0
FB1
FerriteBead_Small
VCCIO_1V8
VCC
VCCDPHY
VCCPLLDPHY
C23
1uF
GND
VCC
C1 C2 C3 C4 C5 C6 C7 C8
0.1uF
VCCDPHY
VCCPLLDPHY
VCCIO_1V8
C9 C10 C11 C18 C19 C20
+1V8
FB2
VCCAUX
C24 C12 C13 C14 C15
1uF
0.1uF
+1V8_A
FB4
VCCA_1V8
C25 C17 C16
+3V3
FB3
VCCIO_3V3
C26 C21 C22
U1A LIFCL-40-7SG72I
BANK 0
VCCIO_3V3 54
VCCIO0
PT80A/MISO 51
PT82A 52
PT82B/MCSN0 53
PT80B 55
PT78A/MCSN 56
PT78B/MOSI 57
PT76B/DONE 58
PT76A/MCLK 59
PT74B/PROGRAMN 60
PT74A/INITN 61
IO2
IO3
IO4
IO5
IO6
IO7
DONE
CLK_IN
PROGRAMN
INITN
U1B LIFCL-40-7SG72I
BANK 1
VCCIO_3V3 49
VCCIO1
P13A/TCK/SCLK 41
PR11A/SDA 42
PR13B 43
PR11B/SCL 44
PR10B/TDO/SSO 45
PR8B/TDI/SSI 46
PR6B/TMS/SCSN 48
JTAG_EN 50
TCK/SCLK
IO0
IO1
TDO/SSO
TDI/SSI
TMS/SCSN
S_SPI_CLK
S_SPI_MISO
S_SPI_MOSI
S_SPI_CS
R6
10kR
JP1
Jumper_3_Bridged12
U1C LIFCL-40-7SG72I
BANK 3
VCCIO_1V8 26
32
VCCIO3
PB54A 22
PB54B 23
PB58A 24
PB58B 25
PB68A 27
PB68B 28
PB72A 30
PB72B 31
PB74A 33
PB74B 34
PB84A 36
PB84B 37
LVDS_RXCLK_P
LVDS_RXCLK_N
LVDS_RX09_P
LVDS_RX09_N
LVDS_RX24_P
LVDS_RX24_N
LVDS_TXCLK_P
LVDS_TXCLK_N
LVDS_TX_P
LVDS_TX_N
U1D LIFCL-40-7SG72I
BANK 5
VCCIO_1V8 18
VCCIO5
PB12B 8
PB12A 9
PB8B 10
PB8A 11
PB4B 13
PB4A 14
PB6B 15
PB6A 16
PB10A 19
PB10B 20
Configuration port: Slave SPI
LIFCL-40:
Slave MOSI (SSI) : PR8B
Slave MISO (SSO) : PR10B
Slave clock (SCLK) : PR13A
Slave CS (SCSN) : PR6B
ProgramN : PT74B
LIFCL-17:
Slave MOSI (SSI) : PR5A
Slave MISO (SSO) : PR5B
Slave clock (SCLK) : PR9A
Slave CS (SCSN) : PR3B
ProgramN : PT57B
The physical pin stays the same
U1F LIFCL-40-7SG72I
POWER
VCC 5
VCCAUX 7
47
VCCA_1V8 39
VCCAUX 29
17
VCC 6
12
21
35
38
40
62
73
VCCPLL_ULC
VCCAUX
VCCADC18
VCCAUXH3
VCCAUXH5
VCC
GND
U1E LIFCL-40-7SG72I
D-PHY
VCCPLLDPHY 63
VCCDPHY 70
72
VCCA_1V8 71
VCCPLLDPHY0
VCCDPHY0
VCCADPHY0
DPHY0_DP2 1
DPHY0_DN2 2
DPHY0_DN0 3
DPHY_DP0 4
DPHY0_DP3 64
DPHY0_DN3 65
DPHY0_DP1 66
DPHY0_DN1 67
DPHY0_CKP 68
DPHY0_CKN 69
Authors: Wojciech SP5WWP, Leo Hofer, Morgan ON4MOD
M17 Project
Sheet: /FPGA/
File: fpga.kicad_sch
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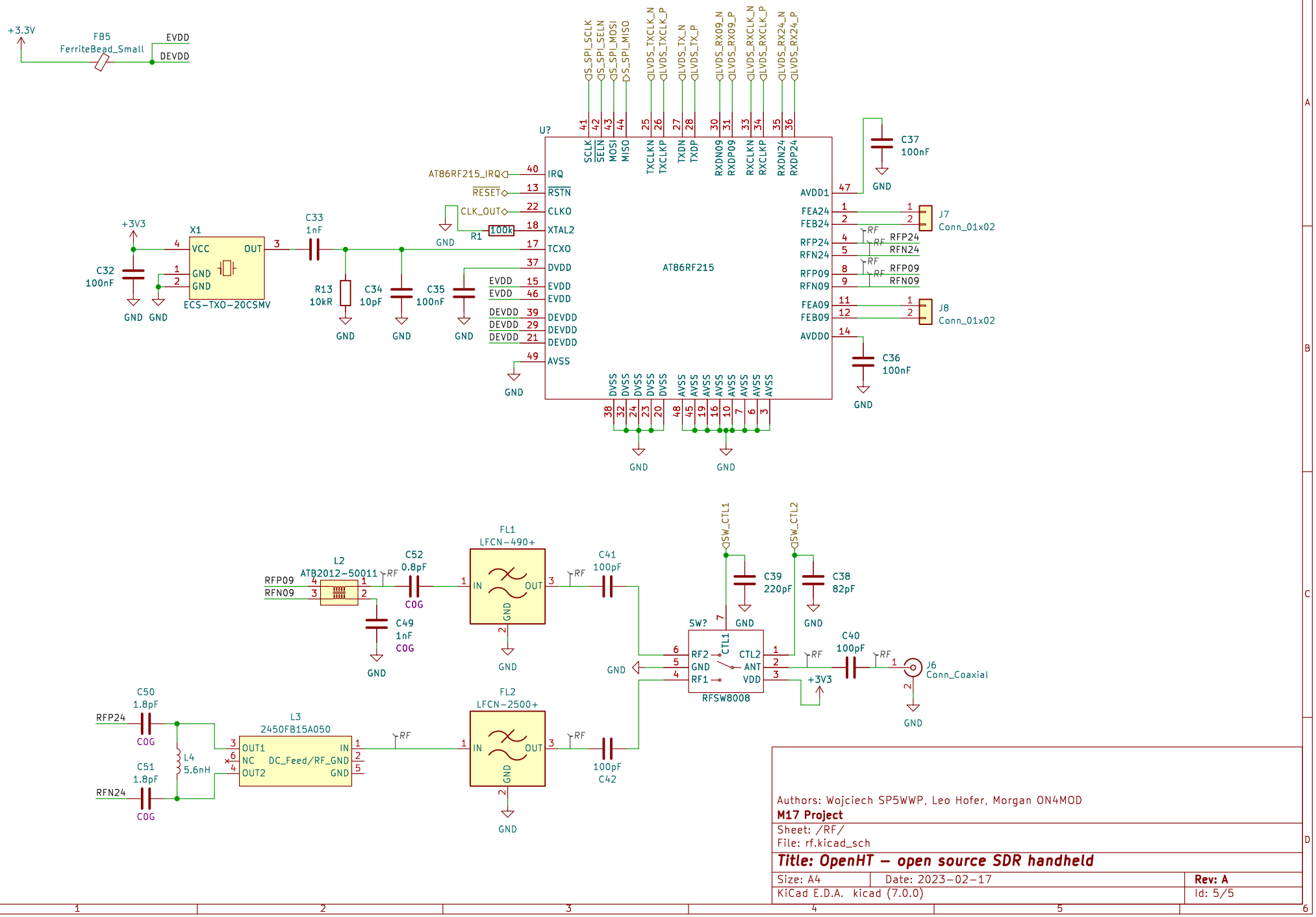

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