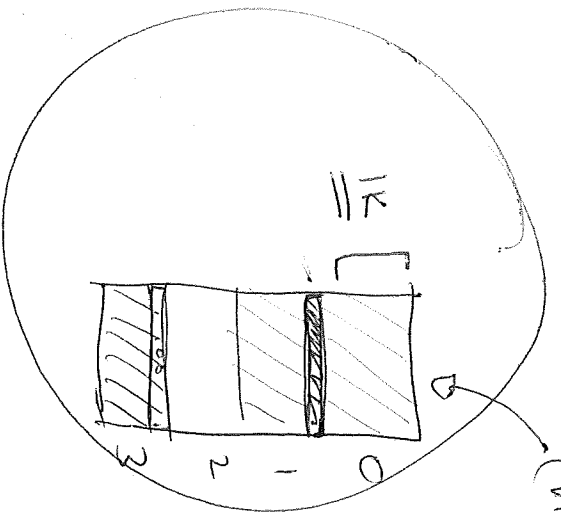


# LECTURE 6:

Detailed Review  
Example

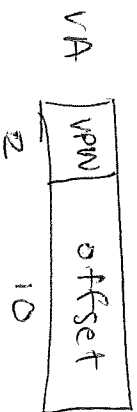
(Paging)

Process A  
(virt.) address space

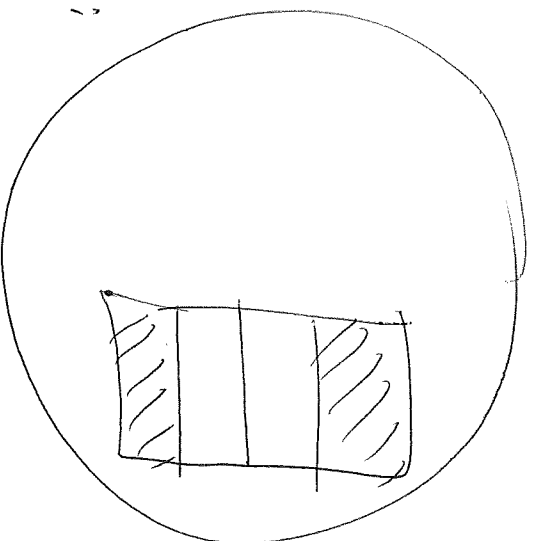


VPN: virtual page number

Virtual Address (VA):



Process B



load 0xC00, R1  
(3072)

Q1) But where are the page tables?

Q2) what is in page table?

PA PT: simple linear array

0	3
1	1
0	---
1	4

valid P=V

7 4 bits

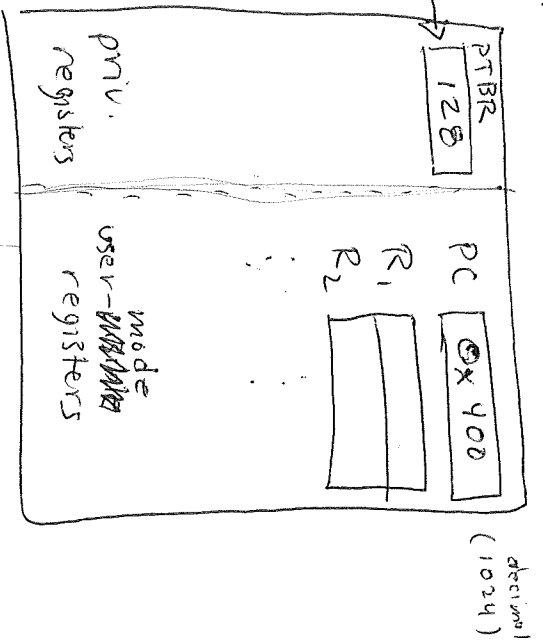
PT<sub>B</sub>

1	7
0	---
0	---
1	2

Q3) Execute an instruction

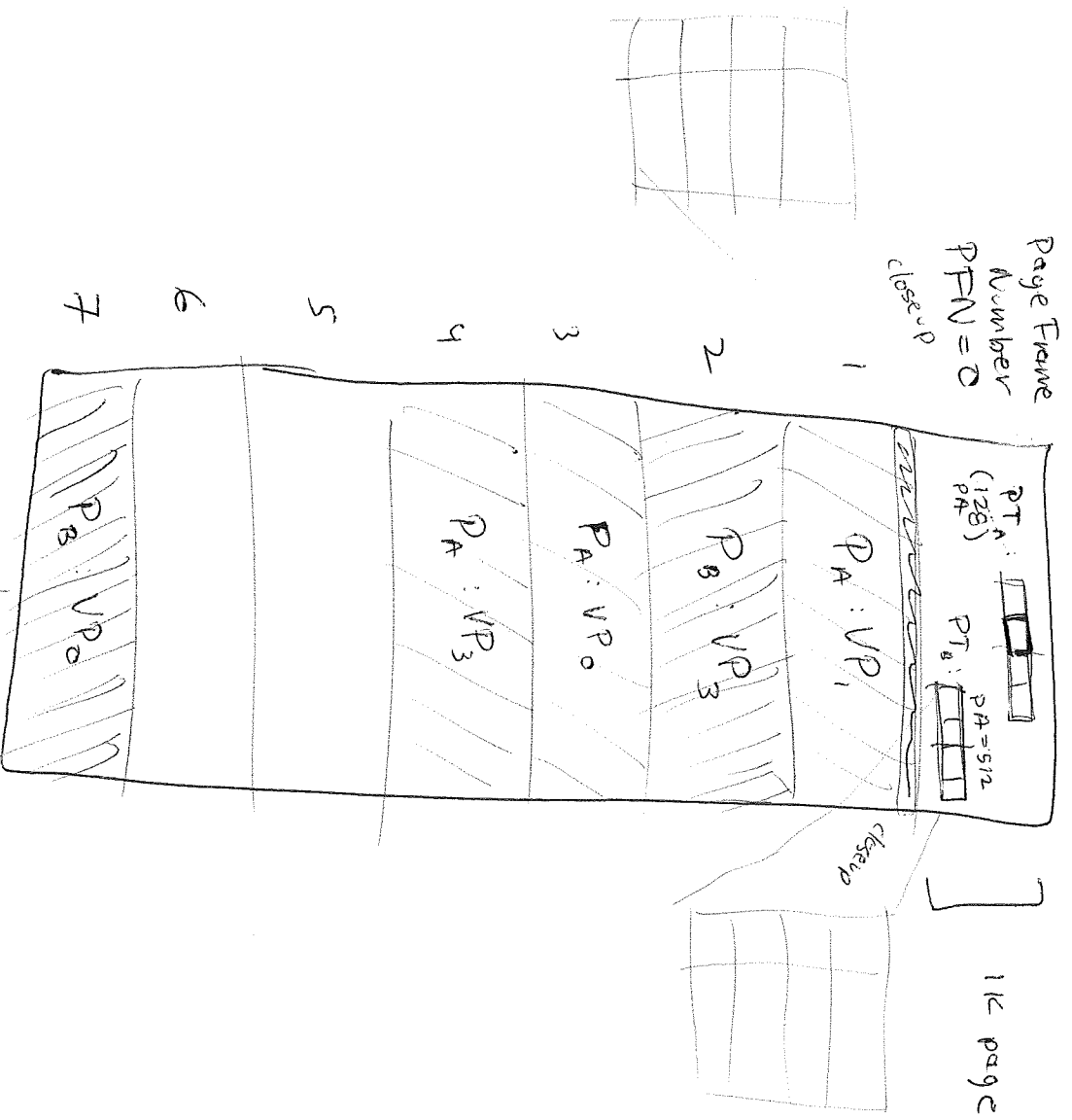
Page Table Base Register

CPU



Physical Memory

Page Frame Number  
PFN = 0  
closed



Thus: Phys. Addr (PA)

has 13 bits

H/W: Fetch instruction  
@ VA = 1024

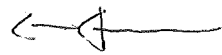
VA: 010000000000

0x4 0 0

000000000000  
VPN offset

$$PTBR: 128 + (VPN * \text{sizeof}(PTE)) + 129$$

translate



000000000000  
offset

PTE [01 | PN = 1]

H/W:

Fetch PTE of VA of instr.  
load 129 => internal register

Now: Fetch inst @ PA 1024

=> load 0x00, R1

if PTE.valid == 0  
Exception (PRDT)  
else  
PA = (PTE.PN << 10) | offset;

PA: 001 000000000000

= 1024