/PICOZED™ SDR

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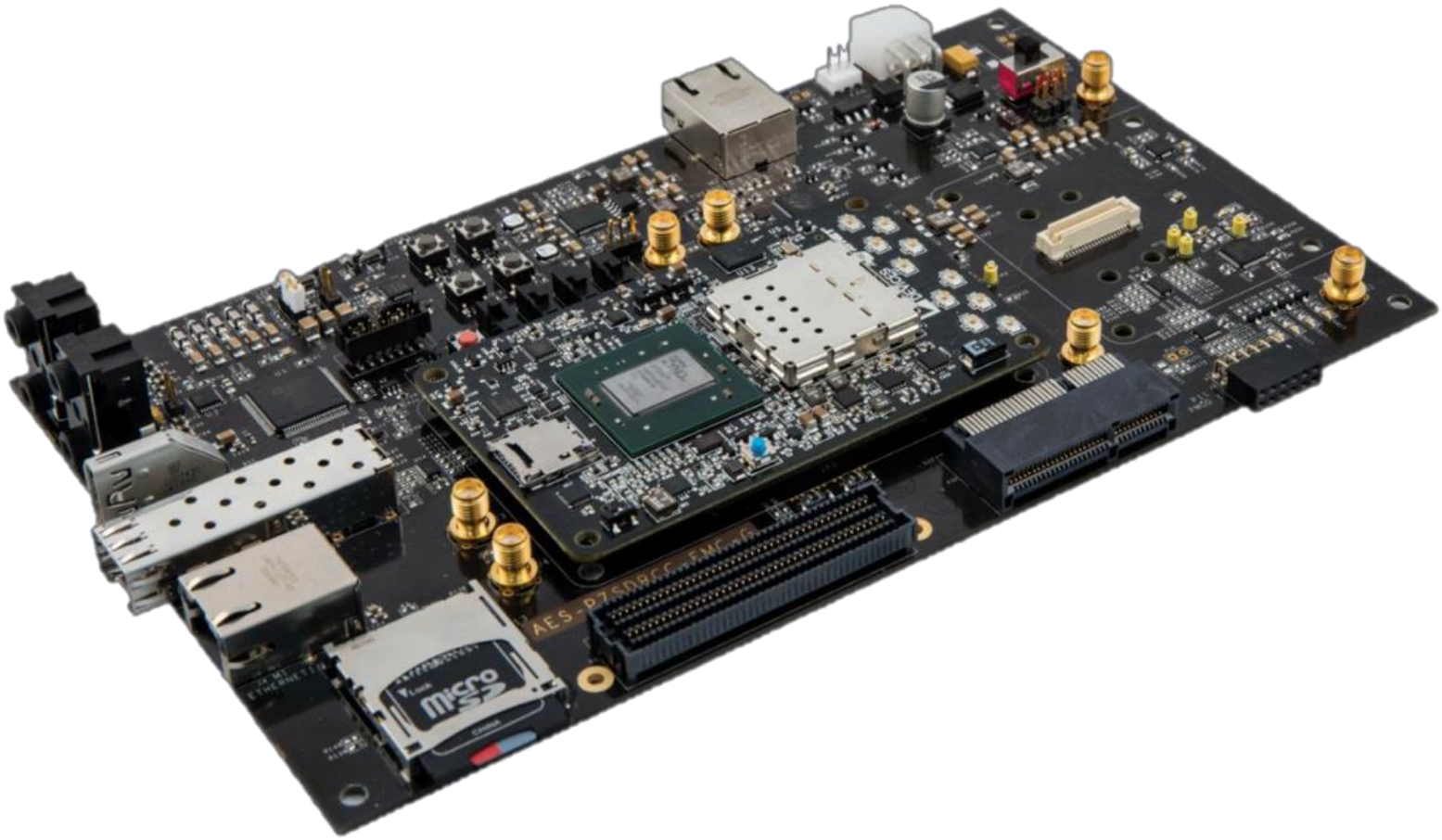

PicoZed™ SDR FMC Carrier Card
AES-PZSDRCC-FMC-G
Hardware User Guide

Version 1.0

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Contents

1 Introduction

The PicoZed™ SDR FMC Carrier Card (Part #: AES-PZSDRCC-FMC-G) gives designers access to a wide variety of peripherals and user I/O required to evaluate and develop with Avnet's PicoZed SDR System-on-Modules (SOM). The FMC carrier is compatible with PicoZed SDR 1x1 and (Part #: AES- Z7PZ-SDR1-G) PicoZed SDR 2x2 (Part #: AES-Z7PZ-SDR2-G).

The carrier card provides all necessary SOM power, reset control, and Zynq SoC I/O pin accessibility through the board-to-board (B2B) micro headers.

This document details the specific features, operation, and configuration of the PicoZed SDR FMC Carrier Card. Please visit www.picozed.org/product/picozed-sdr-development-kit for the latest product information.

1.1 Additional Documentation

This document seeks to simplify user applications by identifying Zynq SoC I/O pins where possible. Further information on the PicoZed SDR SOM is available in the Expansion Headers section of the PicoZed SDR 2x2 SOM User's Guide (http://picozed.org/product/picozed-sdr-som).

Additional information and documentation on Avnet's PicoZed product line can be found at www.picozed.org.

Additional information and documentation on Xilinx's Zynq®-7000 All Programmable SoCs can be found at www.xilinx.com/zynq.

Analog Devices Wiki page for PicoZed SDR support is at http://wiki.analog.com/resources/eval/user-guides/picozed_sdr.

Analog Devices RF Agile Transceivers: AD9361 and AD9364.

1.2 AES-PZSDRCC-FMC-G Features

Expansion Port

- 1x Low Pin Count Zynq PL Mezzanine Card (FMC)
- 2x Digilent Pmod™
- Avnet Camera Module Connector
- RF Personality Module Connector

Configuration and Storage

- Micro SD Card
- I2C EEPROM

External Connectivity

- 2x 10/100/1000 Mb RJ45 Ethernet
- 1x USB-UART
- 1x USB-OTG
- 1x SFP+
- 1x MGT SMA Tx/Rx

Video

- HDMI V1.4, 1080p Output

Audio

- Stereo 24bit 96Khz Codec

User GPIOs

- 4x Push Buttons
- 4x LEDs
- 4x DIP Switches

Clocks

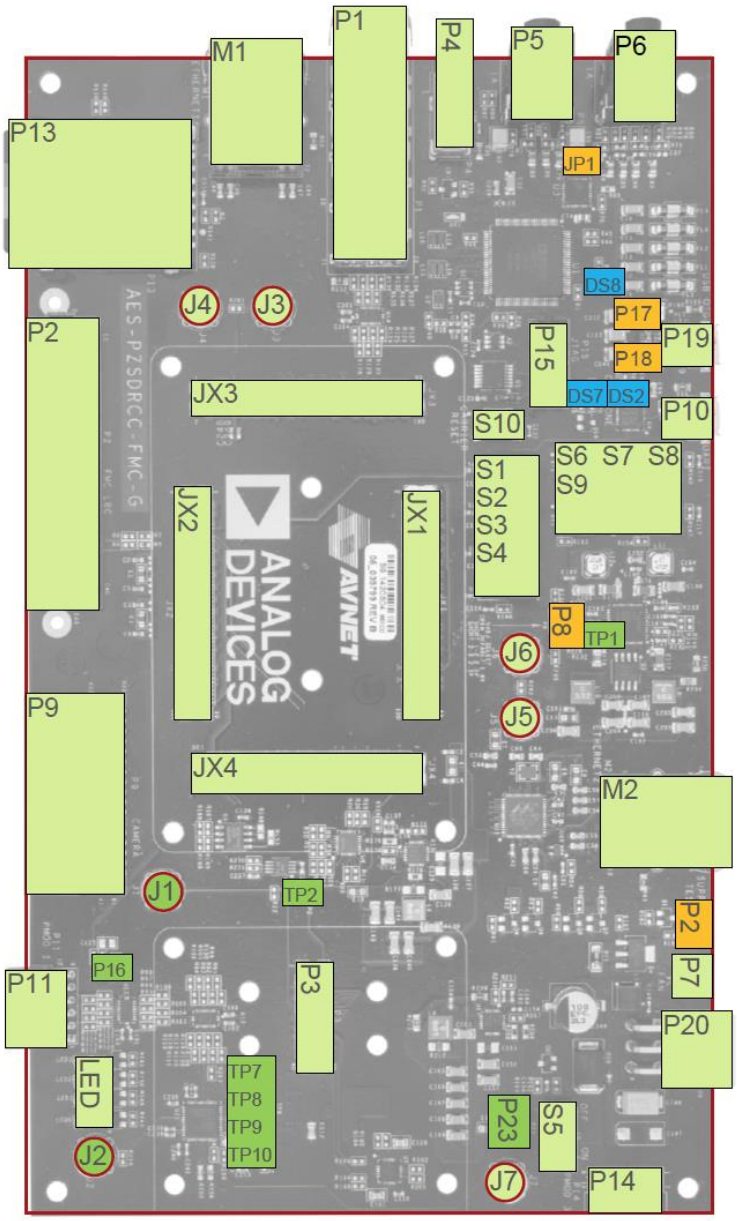
- Programmable Oscillator

Debug

- Xilinx JTAG

Power Supply

- Wall Adapter, Primary 12Vdc @ 5A, 2x3 Connector
- 1.8V, 2.5V or 3.3 Selectable interface voltage
- 5Vdc Fan Header



LEDs

DS2	USB UART
DS7	Config Done
DS8	5V

Jumpers

JP1	Stereo Mic Bias
P8	VADJ
P17	USB OTG Mode
P18	Vbus Bulk Caps
P21	Power Test w/o SOM

Test Points

J2	Clock Generator Test Out
P16	Zynq PL_VBATT_TEST
P23	Voltage Monitor Plug
TP1	PG_MODULE
TP2	AD9361_GPO_VDD
TP7	Clock gen in (-ve)
TP10	Clock gen in (+ve)
TP8	Clock gen reset
TP12	Clock gen monitor

Connectors

J1	AD9361 Clk
J3	MGT TXN
J4	MGT TXP
J5	MGT RXN
J6	MGT RXP
J7	Ext Ref Clk
P1	SFP+
P2	FMC
P3	RF
P4	HDMI
P5	Audio Out
P6	Audio In
P7	Fan
P9	Camera
P10	USB UART
P11	PMOD PL 3.3V
P13	SD Card
P14	PMOD PS 1.8V
P15	JTAG
P19	USB OTG
P20	Power In
JX1-4	B2B Micro Headers

Figure 1: Feature Locations

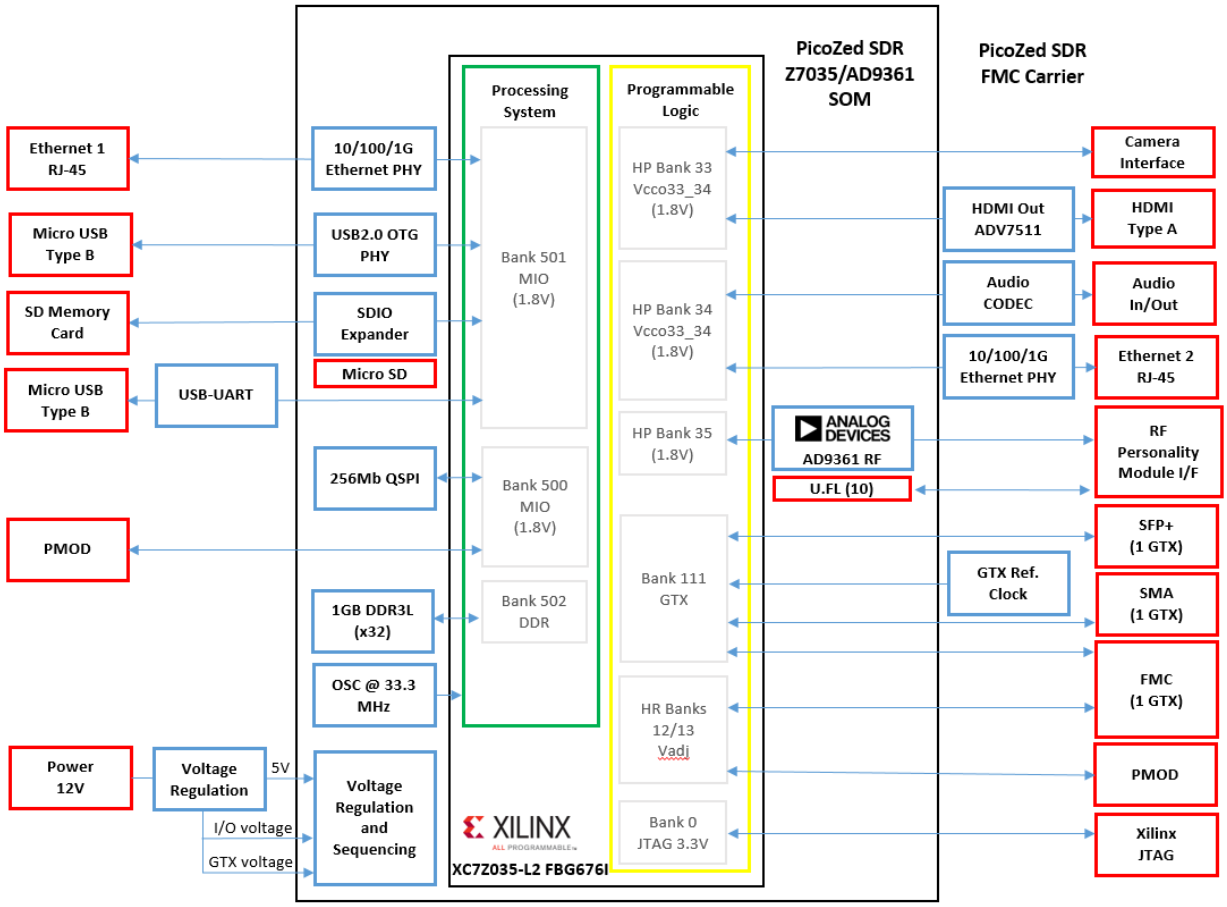


Figure 2 – Carrier Block Diagram with PicoZed SDR 2x2

2 Functional Description

The PicoZed SDR FMC Carrier Card provides power to the SOM and breaks out the I/O signals of the SOM, through appropriate physical interface ICs, to standard industry connectors. This allows you to bypass the stage of developing their own prototyping hardware and focus on developing applications.

The carrier card has video input and output capability through Avnet Camera Module Connector and HDMI interface, respectively. It also has high fidelity audio input and output capability through the on-board audio codec. For connectivity, the carrier card has dual tri-speed Ethernet interfaces, SFP+ cage, and SubMiniature version A (SMA) connectors to multi-gigabit transceivers (MGT). For extra flexibility, one of the Ethernet interfaces is connected to the Zynq PS I/O while the other interface is connected to the Zynq PL I/O. The carrier card provides an alternative bootable SD card connector to the one available on the SOM. Use a slider switch on the SOM to choose between the two.

The USB OTG capability of SOM is also brought out through a Micro USB connector.

If the above I/O interfaces do not meet your requirements, there is a LPC FMC connector and two Digilent Pmod™ connectors which allow you to plug in a wide selection of ready-made modules. You can design interfaces using the four user LEDS, four tact switches, and four slider switches.

2.1 SOM Compatibility

The carrier is compatible with all PicoZed SDR SOMs. Today, the list of supported SOMs includes:

- **PicoZed SDR 1x1** (AES-Z7PZ-SDR1-G): features Xilinx Z7020 and Analog Devices AD9364
- **PicoZed SDR 2x2** (AES-Z7PZ-SDR2-G): features Xilinx Z7035 and Analog Devices AD9361

The available carrier features depends on the SOM being used. The Zynq SoC pin numbers also change between the SOMs. However the signals at the B2B connectors (JX) remain the same. This means the SOMs are 100% electrically compatible, but migrating between the two modules requires software modifications in your Zynq SoC design.

PicoZed SDR 2x2 supports all features on this carrier. PicoZed SDR 1x1 supports a subset of features because the Zynq Z7020 has fewer available user I/Os. The differences are explained in the relevant sections of this document.

2.1.1 SOM Pin Mapping

When working in the Xilinx Vivado tools to create designs for the PicoZed SDR FMC Carrier, you need to understand how the Zynq SoC signals map from the SOM, across the B2B micro headers, and onto the carrier features.

This information can be obtained by referencing the schematics for both the carrier and the SOM. For more than a dozen signals, this can be tedious and error-prone work. We recommend reusing the Xilinx Design Constraints (.xdc) file available for download from the Analog Devices GitHub Repository.

The master XDC file for the PicoZed SDR FMC Carrier can be found in the **hdl/projects/pzsdr/ccfmc** directory of the repository. We highly recommend cloning from the latest official tag (released twice per year) rather than the development branch.

2.2 Reset Sources and Power Monitors

System-ready and reset signals from the SOM are connected on the carrier as described in this section.

2.2.1 Carrier Module Power Good: PG_MODULE

The PG_MODULE is an active low reset signal. The signal ties together the open-drain, power good output of the two DC-DC regulators that produce 1.0V, 1.2V, 1.8V, 1.8V (Audio), 3.3V, and VADJ. When any of these power supplies are below an acceptable threshold, PG_MODULE is pulled to ground to indicate power is not good. When these voltages are healthy, the open-drain outputs become high-impedance state to allow the signal to be pulled up and indicate power ready.

PG_MODULE signal is connected to FMC connector pin D1. An attached FMC can either monitor this signal for power sequencing or reset, or drive this signal to delay Zynq PL boot process.

PG_MODULE signal is a logical AND with ETH1_RESETN (from PicoZed SDR SOM) to reset Ethernet PHYs IC.

PG_MODULE signal is connected to PicoZed SDR SOM through JX2 Pin 11. The SOM does not monitor this signal or use it for power sequencing. Instead, it is connected to a programmable output of power monitor IC. This output can be configured as a power good for all power supplies on the SOM side.

On the PicoZed SDR SOM, PG_MODULE is connected to an LED (D3). When all the voltages on the carrier card and SOM side are within threshold, the LED illuminates.

2.2.2 Carrier Reset

The button, S10, provides an active low signal to net RSTN_C2M which allows you to assert PS_SRST_B signal on the Zynq PL. The PS_SRST_B signal resets all functional IPs on Zynq PS and Zynq PL without disturbing the debug environment. However, asserting PS_SRST_B will cause the Zynq PS to reboot. The Zynq PL may be re-configured if the boot image includes a bit file.

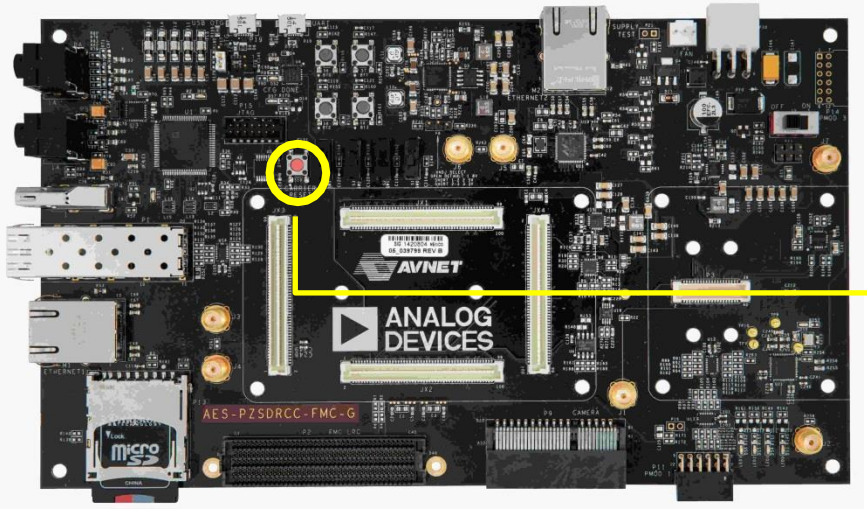


Figure 3 – Carrier Reset

SOM Net Name	Carrier Net Name	B2B Connector	Other Connector
PG_MODULE	PG_MODULE	JX2 Pin 11	P2 Pin D1 (LPC FMC)
CARRIER_RESET	RSTN_C2M	JX1 Pin 6	S10

Table 1 – Connections

SEE FIGURE 27 FOR A PICTURE OF A SUCCESSFULLY CONFIGURED SYSTEM.

2.3 User Buttons, Switches, and LEDs

The carrier provides four switches, four buttons, and four LEDs for prototype.

2.3.1 User Push Buttons

The carrier board provides four user push buttons connected to Zynq PL I/O of the SOM. Each signal has a pull down resistor and noise decoupling capacitor to help reduce switch bounce. When depressed, the button provides a logic high on the respective net.

Note: These signals connect to Zynq PL Banks 33 and 34, powered from the carrier card through B2B connectors.

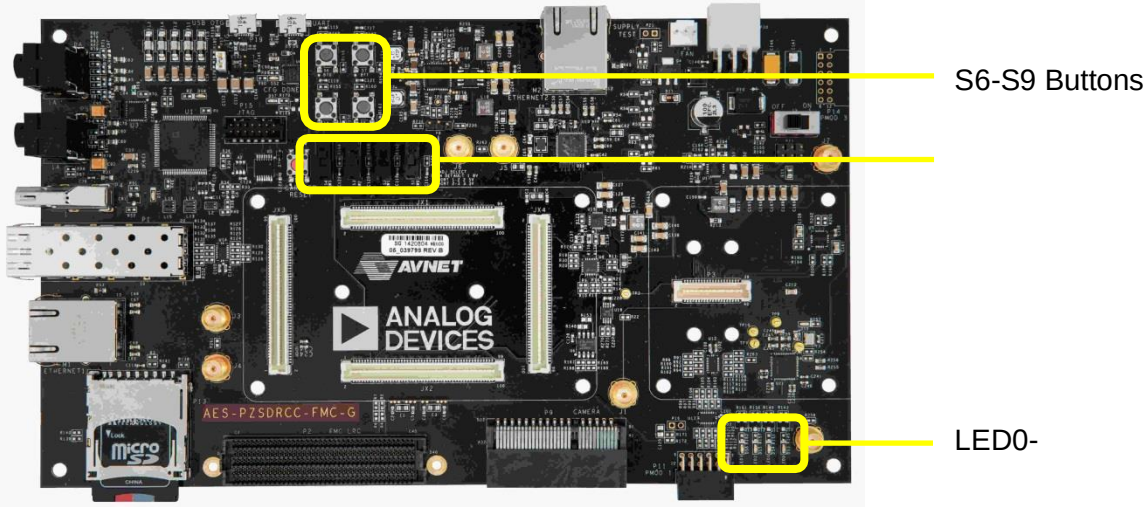


Figure 4 – User Push Buttons

			SDR1x1			SDR2x2		
Switch Name	Carrier Net Name	B2B Connector Pin	Zynq PL Pin	Zynq Bank	Bank Voltage	Zynq PL Pin	Zynq Bank	Bank Voltage
S6	PB_GPIO_0	JX1 Pin 83	n/a	n/a	n/a	J3	33	1.8V
S7	PB_GPIO_1	JX4 Pin 38	Y14	34	1.8V	D8	34	1.8V
S8	PB_GPIO_2	JX4 Pin 41	T16	34	1.8V	F9	34	1.8V
S9	PB_GPIO_3	JX4 Pin 43	U17	34	1.8V	E8	34	1.8V

Table 2 – User Push Button Connections

2.3.2 User LEDs

The carrier board provides four user red LEDs connected to Zynq I/O on the SOM. The LEDs are turned on when their respective I/O pins are driven high. The LEDs are turned off when the Zynq PL pins are not in use or high-impedance state.

Note: The LEDs signals connect to Zynq PL Banks 12 and 34, powered from the carrier card through B2B connectors. Bank 12 I/O voltage is adjustable, while Bank 34 is fixed.

			SDR1x1			SDR2x2		
LED Name	Carrier Net Name	B2B Connector Pin	Zynq PL Pin	Zynq Bank	Bank Voltage	Zynq PL Pin	Zynq Bank	Zynq Voltage
LED0	LED_GPIO_0	JX4 Pin 69	Y19	34	1.8V	A8	34	1.8V
LED1	LED_GPIO_1	JX4 Pin 14	n/a	n/a	n/a	W14	12	VADJ
LED2	LED_GPIO_2	JX4 Pin 16	n/a	n/a	n/a	W17	12	VADJ
LED3	LED_GPIO_3	JX2 Pin 97	E6	500	1.8V	Y16	12	VADJ

Table 3 – User LED Connections

2.3.3 User DIP Switches

The carrier board provides four user DIP switches connected to SDR2x2 PL I/O on SDR2x2. Each DIP output is low-pass filtered to reduce switching noise. When switch positions are set to close pin 1 and 2, the DIP switches outputs logic high to Zynq PL. None of the DIP switches are connected to SDR1x1.

Note: The switch signals connect to Zynq PL Bank 12 and 13, provided from the carrier card through B2B connectors. Bank 12 and 13 I/O voltages are adjustable.

			SDR2x2		
Switch Name	**Carrier Net Name**	**B2B Connector Pin**	**Zynq PL Pin**	**Zynq Bank**	**Bank Voltage**
S1	DIP_GPIO_0	JX2 Pin 99	Y15	12	VADJ
S2	DIP_GPIO_1	JX4 Pin 13	W16	12	VADJ
S3	DIP_GPIO_2	JX4 Pin 15	W15	12	VADJ
S4	DIP_GPIO_3	JX2 Pin 13	V19	13	VADJ

Table 4 – User DIP Switches Connections

2.4 I2C Address Space and Registers

The carrier board provides an I2C connection to the Zynq PL I/O of the SOM to the I2C-enabled slave devices on the carrier board.

			SDR1x1			SDR2x2		
I2C Name	**Carrier Net Name**	**B2B Connector Pin**	**Zynq PL Pin**	**Zynq PL Bank**	**Bank Voltage**	**Zynq PL Pin**	**Zynq PL Bank**	**Bank Voltage**
SDA	SDA	JX2 Pin 19	V6	13	VADJ	AF25	13	VADJ
SCL	SCL	JX2 Pin 17	W6	13	VADJ	AF24	13	VADJ

Table 5 – I2C Connections to PicoZed SDR SOM

The I2C circuit design on the carrier board can adapt to any I/O voltage (VADJ) you set. The circuit includes an 8-channel I2C switch to interface with the I2C slave devices on the carrier board and to any new slaves added through FMC, RF Personality Module, and Avnet Camera Module connectors. The I2C switch can be used to resolve any I2C address conflicts that may arise. The I2C switch also performs voltage translation for existing I2C slaves on the carrier board and for any new slaves added through FMC, RF Personality Module, and Avnet Camera Module connectors.

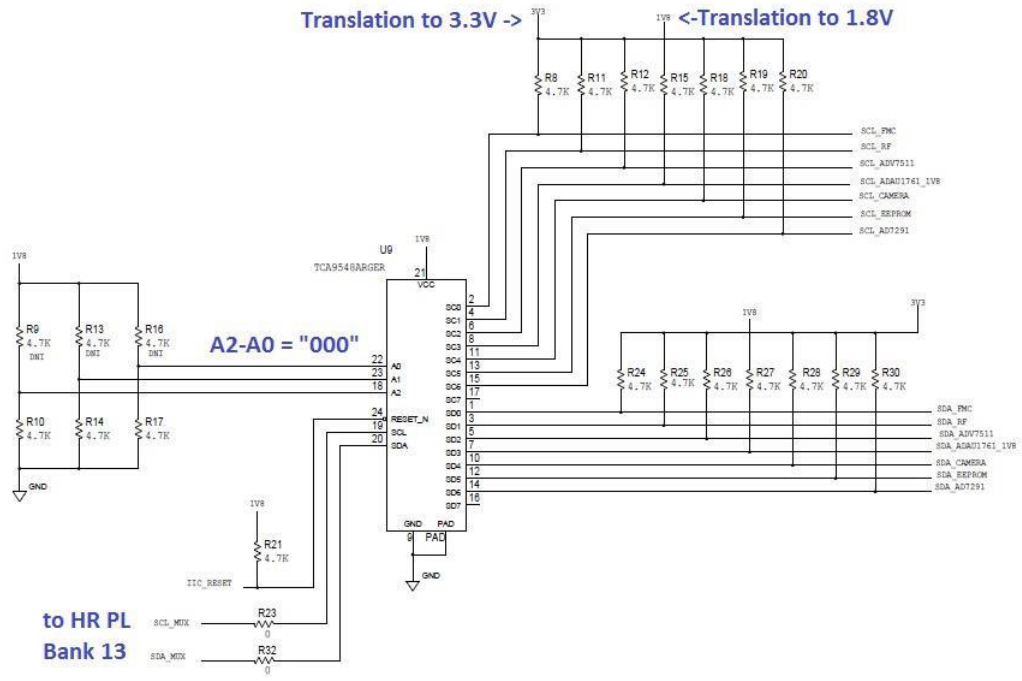


Figure 5 – I2C MUX/Voltage Translator Circuit

At power up, the default I2C switch condition has none of the eight channels enabled. The I2C addresses are as follows:

PCB Ref	Part	Description	Switch Channel	Address MSB						LSB	Remarks
U9	TCA9548ARGER	I2C Switch	-	1	1	1	0	0	0	0	
P2	-	To FMC Connector	0	-	-	-	-	-	-	-	
P3	-	To RF Connector	1	-	-	-	-	-	-	-	
U1	ADV7511KSTZ	HDMI Transmitter	2	0	1	1	1	0	0	1	PD=0
U1	ADV7511KSTZ	HDMI Transmitter	2	0	1	1	1	1	0	1	PD=1
U3	ADAU1761BCPZ	Audio Codec	3	0	1	1	1	0	1	1	
P9	-	To Camera Connector	4	-	-	-	-	-	-	-	
U6	AT24C32D-SSHM-B	I2C Serial EEPROM	5	1	0	1	0	0	0	0	
U7	AD7291BCPZ	8-Chan 12-bit ADC	6	0	1	0	1	1	1	1	

Table 6 – I2C Addresses

2.5 Clocks

The carrier includes a programmable clock synthesizer to provide references for the Zynq MGT or other off-board connections. The carrier provides the option to inject an external clock on the AD936x on the SOM.

2.5.1 Clock Synthesizer IC

The carrier board contains an Analog Device AD9517-3ABCPZ programmable clock synthesizer (U21) to offer maximum clocking flexibility. The clock synthesizer circuit can choose from three options as reference clock.

1. Internal VCO
2. 25MHz Oscillator
3. SMA Input

The synthesizer is wired to provide two outputs as follows:

- LVDS differential clock to MGTREFCLK pins for MGT bank on SDR2x2
- CMOS clock to SMA connector J2

Note: On Rev B of the carrier card, this output is obtained from pin OUT5A of the clock synthesizer IC whereas for Rev C of the carrier card, this output is from OUT7B.

The board design includes a green LED DS9 to indicate the internal PLL has achieved lock. The clock synthesizer needs to be programmed to enable outputs. Programming can be performed through its SPI interface connected to the Zynq PL I/O of the SOM.

			SDR1x1	SDR2x2 Rev C or older	SDR2x2 Rev D and later		
AD9517 pin	**Description**	**B2B Connector Pin**	**Zynq PL Pin**	**Zynq PL Pin**	**Zynq PL Pin**	**Bank Voltage**	
OUT4_OUT4A	LVDS out p	JX3 Pin 2		AA6 Bank 111	U6 Bank 112	1.2V	
OUT4_N_OUT4B	LVDS out n	JX3 Pin 4		AA5 Bank 111	U5 Bank 112	1.2V	
CS_N	SPI CS	JX4 Pin 76	R18	B4	B4	1.8V	All SPI signals are connected to Bank 34
SDIO	MOSI	JX4 Pin 75	R17	C3	C3	1.8V	
SDO	MISO	JX4 Pin 74	T17	B5	B5	1.8V	
SCLK	SPI CLK	JX4 Pin 73	R16	C4	C4	1.8V	

Table 7 – Clock Generator Connections

2.5.2 External AD9361 Clock

By default, AD9361 on the SOM gets its reference clock from an oscillator on board the SOM. However, the SOM can be configured to get the reference clock from connector J1 on the carrier card by asserting a signal from the Zynq SoC.

			AD9361 Datasheet, Input Specifications		
Reference Designator	Connector Type	B2B Pin	Frequency Range	Nominal Input Level	Input Coupling
J1	SMA	JX4 Pin 63	10-80MHz	1.3Vpp	AC

Table 8 – External AD9361 Specifications

The clock signal on the carrier has a parallel 49.9Ω termination resistor (R22). The intent is that external test equipment will be connected to the SMA (J1) to inject a clock into the system.

Note 1: Double Termination and AC coupling on Rev B/C SDR2x2

A few aspects of the external clock circuit on early SDR2x2 SOMs were not optimal. For Rev B and Rev C SDR2x2 SOMs the clock signal is terminated with 49.9Ω (R5). Therefore, the combined termination impedance is 25 Ω. You can desolder R22 on the carrier card to increase input level, if necessary. In addition, the external clock signal lacks any AC coupling.

SDR2x2 (Rev E and later) and all SDR1x1 SOMs have an improved circuit that removes the parallel termination and relies on the carrier to provide proper termination. These SOMs also place an 18pF AC coupling capacitor (C216) at the XTLAN pin of the AD936x as required by the datasheet.

See Figure 6 and Figure 7 for simplified diagrams of the two different external clocking circuits.

Note 2: Connecting Clock Synthesizer (J2) to AD936x input (J1)

AD9361 input level is nominally 1.3Vpp, AC coupled, whereas clock synthesizer output is CMOS 3.3V DC. It is recommended to use an AC coupled attenuation network to connect J2 to J1.

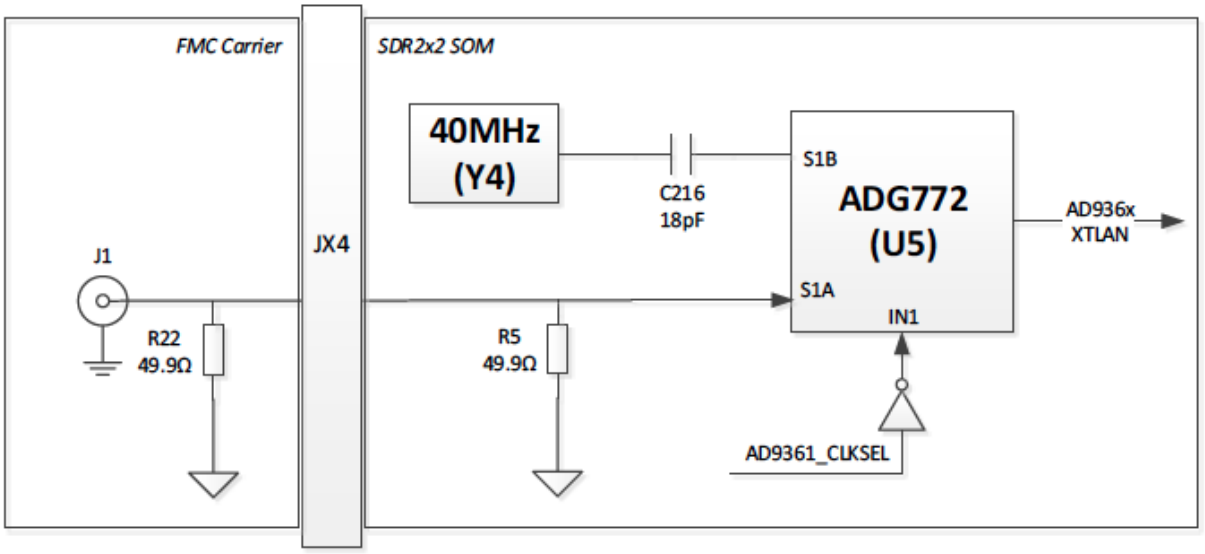


Figure 6 – SDR2x2 (Rev B/C) AD9361 Clock Diagram

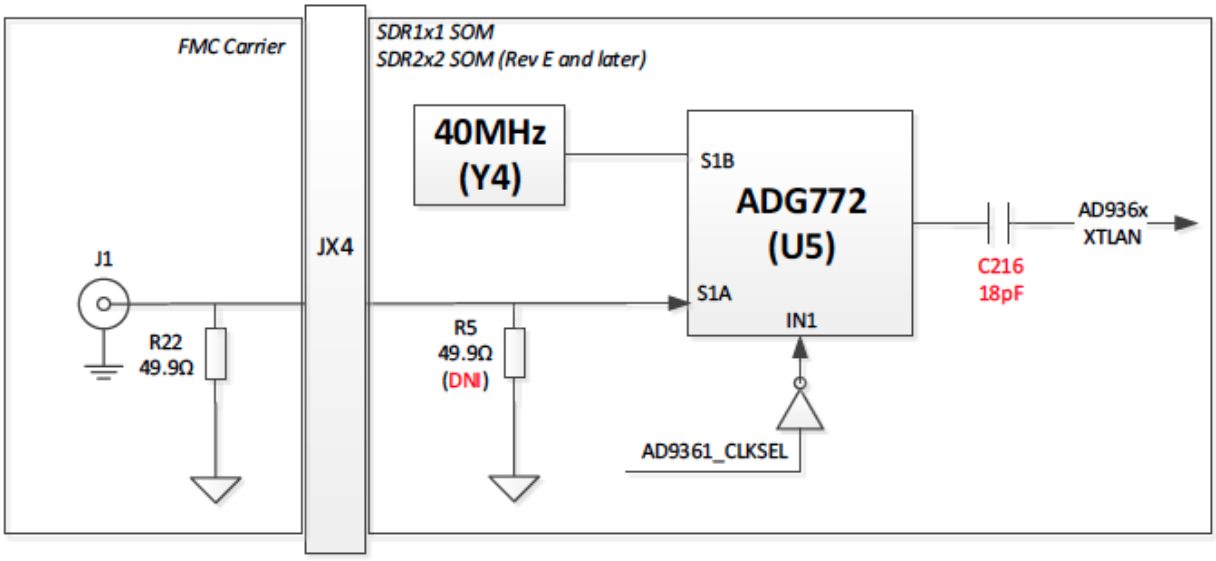


Figure 7 – SDR1x1 (all), SDR2x2 (Rev E and later) AD936x Clock Diagram

2.6 Low Pin Count FMC Connector

A single Low Pin Count (LPC) FMC connector (P2) is implemented on the carrier board to support FMC plug-in modules. The block diagram shows the PicoZed SOM connections to the FMC LPC connectors. The FMC signals are wired to HR Banks 12 and 13 of the Zynq PL and powered by VADJ to allow maximum flexibility in choice of FMC module voltages. See Figure 8 – FMC Connections for topology overview.

When an FMC board is plugged in, the FMC_PRSNT signals are driven low per the FMC specification. The FMC_PRSNT signal is used to switch the JTAG signals so the FMC card can be accessed through the JTAG interface. When a FMC card is not present, FMC_PRSNT is pulled high and the JTAG interface is isolated to the SOM only. See *JTAG*.

The FMC_PRSNT signal can be used as an indicator to the SOM that an FMC device has been attached.

There are two mounting holes in the FMC card area to facilitate secure FMC module mounting and match the FMC specification.

The following guidelines have been observed in the design of the FMC interface:

CLK_#_M2C

- 50 ohm single-ended impedance
- Less than 10mil skew in P/N pair
- Connected to MRCC pins of Zynq PL on PicoZed SDR SOM (same bank as LA bus signals)
- Length matching to any other feature

LA bus

- 50 ohm single-ended impedance
- Less than 10mil skew in P/N pair
- Less than 100mil length skew across all bits in a bus
- LA Bus 0:16 located in Bank 12
- LA Bus 17:33 located in Bank 13
- CC Pairs LA00 on MRCC, LA01 on SRCC pins, Bank 12
- CC Pairs LA17 on MRCC, LA18 on SRCC pins, Bank 13

To conserve SoC pins, GA [1:0] pins are pulled down to “00” via resistors on the carrier card for address selection.

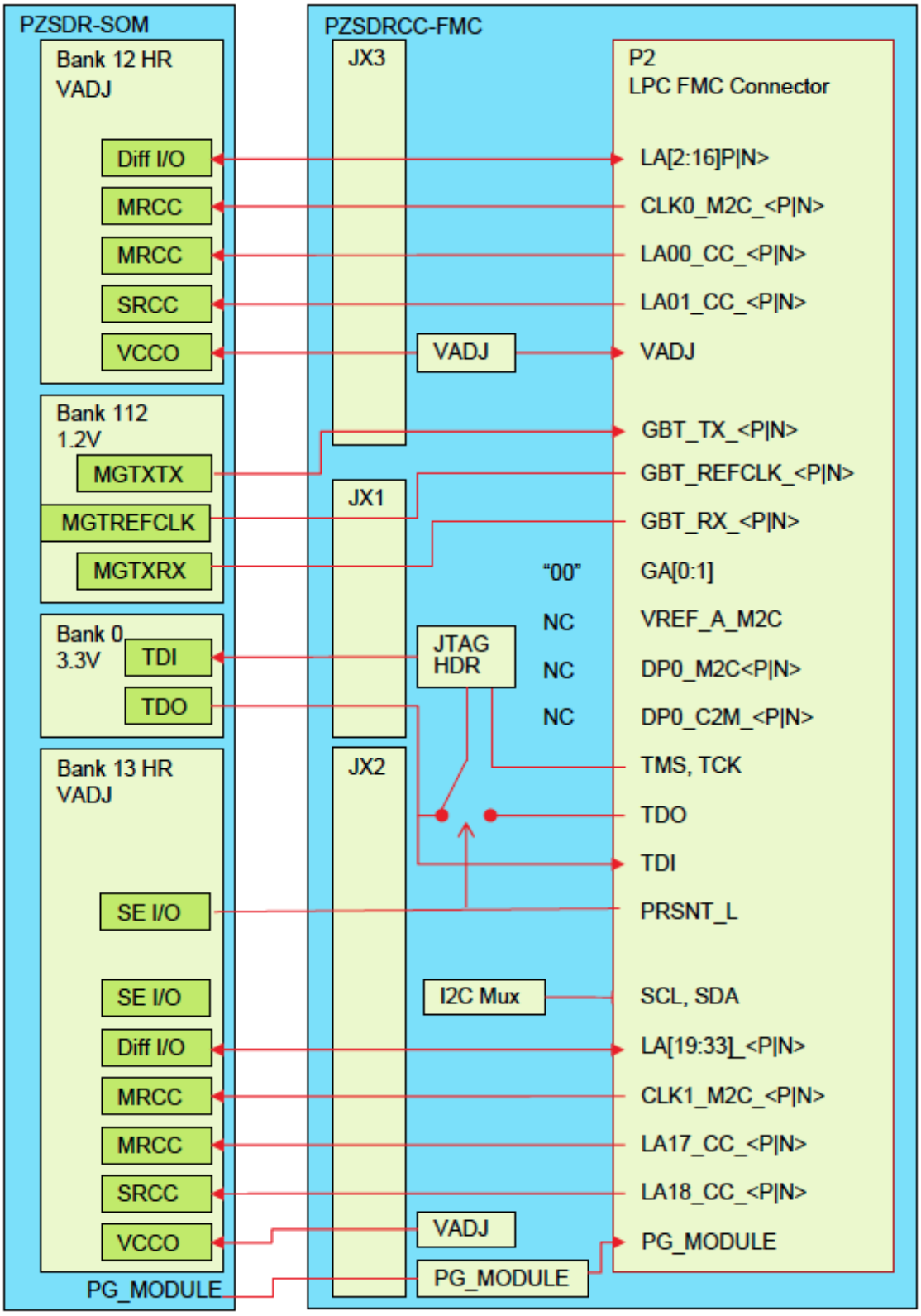


Figure 8 – FMC Connections

2.7 SFP+ Interface

A single SFP+ connector and cage (P1) is available on the carrier board. The SFP+ data interface is connected to one of SDR2x2's Zynq MGT banks. The same MGT bank also receives output from the clock generator described in *Clocks.* The SFP+ function is not available on SDR1x1 because it does not have any Zynq MGT transceivers.

Note: Starting with Rev D SDR 2x2 SOMs, the SFP+ connection moved from Zynq Bank 111 to Bank 112 to meet Xilinx recommendations for PCIe implementation.

The SFP+ seven status and control signals are connected to six I/Os from Zynq PL Bank 12 on SDR2x2. RS0 and RS1 are shorted together and driven from the same Zynq PL I/O pin. For designs requiring separate control of RS0 and RS1, resistor R252 may be removed. See the schematic for details.

SFP+ modules operate from 3.3V supply, but status and control signals from Bank 12 are powered from VADJ. Therefore, a voltage translator is used. This allows you to use SFP+ interface even when operating Bank 12 at non-3.3V levels. The interface has been tested to meet the Zynq GTX performance level of 6.6 Gbps.

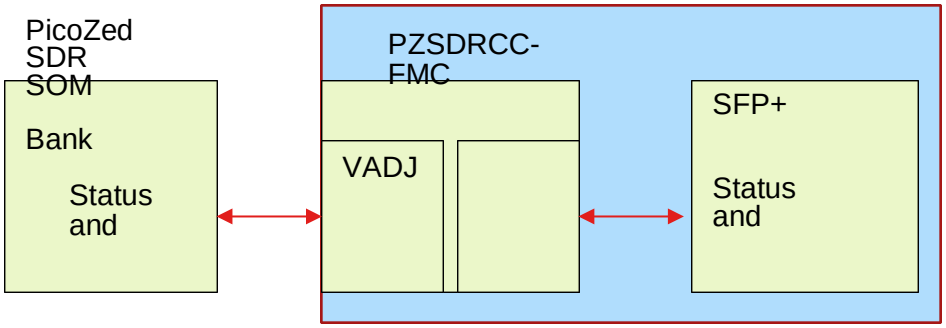


Figure 9 – Voltage Translation SFP+ Status and Control

SFP+ Signal	Carrier Net Name	B2B Connector Pin	Zynq PL Pin	Zynq Bank	Bank Voltage
TX_FAULT	SFP_GPIO_0_3V3	JX2 Pin 88	Y17	12	VADJ
TX_DISABLE	SFP_GPIO_1_3V3	JX2 Pin 90	AA17	12	VADJ
MOD_DEF2(SDL)	SFP_GPIO_2_3V3	JX2 Pin 87	AB17	12	VADJ
MOD_DEF1(SCL)	SFP_GPIO_3_3V3	JX2 Pin 89	AB16	12	VADJ
MOD_DEF0(ABSENT)	SFP_GPIO_4_3V3	JX2 Pin 93	AC17	12	VADJ
RATESEL0	SFP_GPIO_5_3V3	JX2 Pin 95	AC16	12	VADJ
LOS	SFP_GPIO_6_3V3	JX2 Pin 94	AA15	12	VADJ
RATESEL1	SFP_GPIO_5_3V3		Same as RATESEL0		

Table 9 – SFP+ Control Connections

			SDR2x2 Rev C or Older		SDR2x2 Rev D and later		
SFP+ Signal	Carrier Net Name	B2B Connector Pin	Zynq PL Pin	Zynq Bank	Zynq PL Pin	Zynq Bank	Bank Voltage
RXD+	SFP_GBT_RX_P	JX1 Pin 91	AE6	111	Y4	112	1.2V
RXD-	SFP_GBT_RX_N	JX1 Pin 93	AE5	111	Y3	112	1.2V
TXD+	SFP_GBT_TX_P	JX3 Pin 13	AF4	111	W2	112	1.2V
TXD-	SFP_GBT_TX_N	JX3 Pin 15	AF3	111	W1	112	1.2V

Table 10 – SFP+ Data Connections for SDR2x2

2.8 Digilent PMOD™ Interfaces

The carrier has two Digilent Pmod™ right angle 0.1" female sockets (2x6). Pmod connector P11 is connected to the Zynq PL I/O on the SOM while Pmod connector P14 is connected to the Zynq PS I/O.

Visit https://www.digilentinc.com/Pmods/Digilent-Pmod_%20Interface_Specification.pdf for the latest specification.

Connector P11 is supplied from 3.3V rail. The interface signal from PicoZed SDR SOM is connected to Bank 13 which is supplied from VADJ, not necessarily powered at 3.3V. So a voltage translator is included to translate Zynq PL I/Os from VADJ to 3.3V.

Note: Due to a shortage of I/O pins on SDR1x1, only two of the eight PMOD signals are implemented.

Connector P14 is supplied from 1.8V rail. This connector interfaces with Zynq PL I/Os from PicoZed SDR SOM I/O bank 500 and 501 which are also powered from 1.8V. Therefore, no translator is needed. However, the PicoZed SDR carrier card is delivered with P14 unmounted because the 1.8V voltage is not compliant with the Pmod standard. You can solder a compatible connector to use it.

The following table is for P11 to Zynq PL I/O.

			SDR1x1	SDR2x2		
Pin Number	**Carrier Net Name**	**B2B Connector Pin**	**Zynq PL Pin**	**Zynq PL Pin**	**Zynq Bank**	**Bank Voltage**
1	PMOD0_D0_3V3	JX2 Pin 67	V11	AC18	13	VADJ
2	PMOD0_D1_3V3	JX2 Pin 69	V10	AC19	13	VADJ
3	PMOD0_D2_3V3	JX2 Pin 68		AA19	13	VADJ
4	PMOD0_D3_3V3	JX2 Pin 70		AB19	13	VADJ
5, 11	GND					
6, 12	3V3					
7	PMOD0_D4_3V3	JX2 Pin 73		W18	13	VADJ
8	PMOD0_D5_3V3	JX2 Pin 75		W19	13	VADJ
9	PMOD0_D6_3V3	JX2 Pin 74		Y18	13	VADJ
10	PMOD0_D7_3V3	JX2 Pin 76		AA18	13	VADJ

Table 11 – PMOD P11 Connections

The following table is for P14 to Zynq PS I/O.

			SDR1x1	SDR2x2		
Pin Number	Carrier Net Name	B2B Connector Pin	Zynq PL Pin	Zynq PL Pin	Zynq Bank	Bank Voltage
1	PMOD_MIO_D0	JX4 Pin 85	C8	C24	500	1.8V
2	PMOD_MIO_D1	JX4 Pin 87	E9	A25	500	1.8V
3	PMOD_MIO_D2	JX4 Pin 86	D9	A23	500	1.8V
4	PMOD_MIO_D3	JX4 Pin 88	C6	B26	500	1.8V
5, 11	GND					
6, 12	1.8V					
7	PMOD_MIO_D4	JX4 Pin 91	E8	B25	500	1.8V
8	PMOD_MIO_D5	JX4 Pin 93	C5	D23	500	1.8V
9	PMOD_MIO_D6	JX4 Pin 92	D16	E17	501	1.8V
10	PMOD_MIO_D7	JX4 Pin 94	B14	B19	501	1.8V

Table 12 – PMOD P14 Connections

2.9 SOM Interface Micro Headers

The carrier has four 100-pin FCI Bergstak 0.8mm Micro Headers (FCI, 61083-101400LF) for connection to the SOM (JX1, JX2, JX3, and JX4). These are often referred to as Board-to-Board (B2B) connectors.

Key connector features for this application include the following:

- 100 mating cycles
- 8 Gbps data rate
  (Greater than the Zynq device on the PicoZed SDR SOM which is max 6.25 Gbps)
- Current carrying capacity = 500mA per pin

Further information on connectors can be obtained from BergStak® 0.8mm Mezzanine Connectors at http://www.fci.com/en/products/board-to-board-wire-to-board/board-to-board/08mm-board-to-board-signal/bergstak-08mm-pitch.html.

CAUTION: Extra care must be exercised when separating the PicoZed SDR SOM from the carrier card. Although the FCI Bergstak connector specification allows for a length-wise peeling method to separate plugs from the receptacle, the carrier card arranges its four connectors at right angles to each other. If the PicoZed SDR SOM is removed by lifting up from one edge only, the connector at the far end may be subject to undue stress. Users should separate the SOM by incrementally lifting the SOM at all four corners until fully separated.

	Micro Header JX1			
	Signal Name	**Source**	**SDR1x1 Pins**	**SDR2x2 Pins**
JTAG	TMS	Zynq Bank 0	1	1
	TCK	Zynq Bank 0	1	1
	TDI	Zynq Bank 0	1	1
	TDO	Zynq Bank 0	1	1
CTRL	PWR_ENABLE		1	1
	RSTN_C2M	Carrier to Zynq Bank 501	1	1
	CFG_DONE	Zynq Bank 0	1	1
HP PL	HDMI	Zynq Bank 33		24
	CAM	Carrier to Zynq Bank 33		22
	CAM SPI	Zynq Bank 33		4
MGT	FMC MGT	Zynq Bank 112		4
	SFP+ MGT	Zynq Bank 112		2
	SMA MGT	Zynq Bank 112		2
Power	VIN, 5V	Carrier	4	4
	VADJ	Carrier to Bank 12 Supply	0	3
	CFG_VBATT	Carrier	1	1
	GND	Carrier	23	23
NC	No Connects	No Connects	65	4
Total			**100**	**100**

Table 13 – Micro Headers JX1 Overview

Micro Header JX2				
	Signal Name	Source	SDR1x1 Pins	SDR2x2 Pins
HR PL	FMC_PRSNT	Zynq Bank 13		1
	FMC LA_[17-33] , Clk1,	Zynq Bank 13	23	36
	FMC LA_[15-16]	Zynq Bank 12		4
	SCL	Zynq Bank 13	1	1
	SDA	Zynq Bank 13	1	1
	DIP	Zynq Bank 13		1
	DIP	Zynq Bank 12		1
	PMOD	Zynq Bank 13	2	8
	SFP+ Ctrl & Status	Zynq Bank 12		7
	LED	Zynq Bank 12		1
	RF GPIO	Zynq Bank 13		2
	RF GPIO	Zynq Bank 12		1
CTRL	CFG_INIT_B	Zynq Bank 0	1	1
	PG_MODULE	Carrier	1	1
	VCCIO_EN	Carrier		1
Power	Vin, 5V	Carrier	5	5
	VCCO_33, VCCO_34, 1.8V	Carrier	3	3
	VADJ	Carrier to Bank 13 Supply	1	1
	GND	Carrier	23	23
NC	No Connects	No Connects	41	1
Total			**1000**	**100**

Table 14 – Micro Headers JX2 Overview

Micro Headers JX3				
	Signal Name	Source	SDR1x1 Pins	SDR2x2 Pins
PS	SDCARD	Zynq Bank 501	7	7
SOM	Gigabit Ethernet	SOM PHY	10	10
	USB OTG – TYPE A (Data & Ctrl)	SOM PHY	4	4
HR PL	FMC LA_[0-14] , Clk1	Zynq Bank 12		32
MGT	FMC MGT	Zynq Bank 112		2
	MGT REFCLK	Carrier		2
	SFP+ MGT	Zynq Bank 112		2
	SMA MGT	Zynq Bank 112		2
Power	AVCC, 1V	Carrier		4
	AVTT, 1.2V	Carrier		2
	VCCO_13	Carrier	2	2
	GND	Carrier	26	26
	USB_VBUS_OTG	Carrier		1
NC	No Connects	No Connects	58	4
Total			**100**	**100**

Table 15 – Micro Header JX3 Overview

Micro Headers JX4				
	Signal Name	**Source**	**SDR1x1 Pins**	**SDR2x2 Pins**
HR PL	DIP	Carrier to Zynq Bank 12		2
	LED	Zynq Bank 12		2
HP PL	CAM	Carrier to Zynq Bank 34	9	9
	I2S	Carrier to Zynq Bank 34	5	5
	PB	Carrier to Zynq Bank 34	3	3
	RGMII	Zynq Bank 34	12	12
	MDIO	Zynq Bank 34	2	2
	RF GPIO	Zynq Bank 34	3	3
	FAN	Zynq Bank 34	2	2
	Programmable Clock Synthesizer	Zynq Bank 34	8	8
	LED	Zynq Bank 34	1	1
PS	PMOD	Zynq Bank 500	8	8
	UART	Zynq Bank 501	2	2
	Eth Resetn	Zynq Bank 501	1	1
	Spare	Zynq Bank 500	1	1
AD9361	AD9361 Control, Status, ADC, DAC and clk	SOM AD9361	8	8
NC Power	AD9361 VDDA_GPO	SOM	1	1
	GND	Carrier	28	28
	No Connects	No Connects	6	2
Total			**100**	**100**

Table 16 – Micro Header JX4 Overview

2.10 Multi-Gigabit Transceivers

SDR2x2 has two GTX Multi-Gigabit Transceiver (MGT) Quads. Each Quad consists of four transceivers capable of 6.6 Gbps data rate. Of the four transceivers routed on the SOM, the carrier card connects three transceivers to the following interfaces:

1. LPC FMC (*See Low Pin Count FMC Connector*)
2. SFP+ (*See SFP+ Interface*)
3. SMAs (*See SMA Data TX/RX_P/N Pairs*)

The fourth transceiver is left unconnected.

Each MGT quad has two inputs for reference clocks. Both of these clocks are provided by the carrier card. One of them is connected to the clock generator (see *Clocks*). The other clock is connected to the FMC connector (see *Low Pin Count FMC Connector*). This allows you to implement various protocols requiring different line rates.

Note: The PicoZed SDR 1x1 (AES-Z7PZ-SDR1-G) SOM does not include MGT serial transceivers. Therefore, the MGT peripherals of the FMC Carrier will not be enabled when a PicoZed SDR 1x1 SOM is connected.

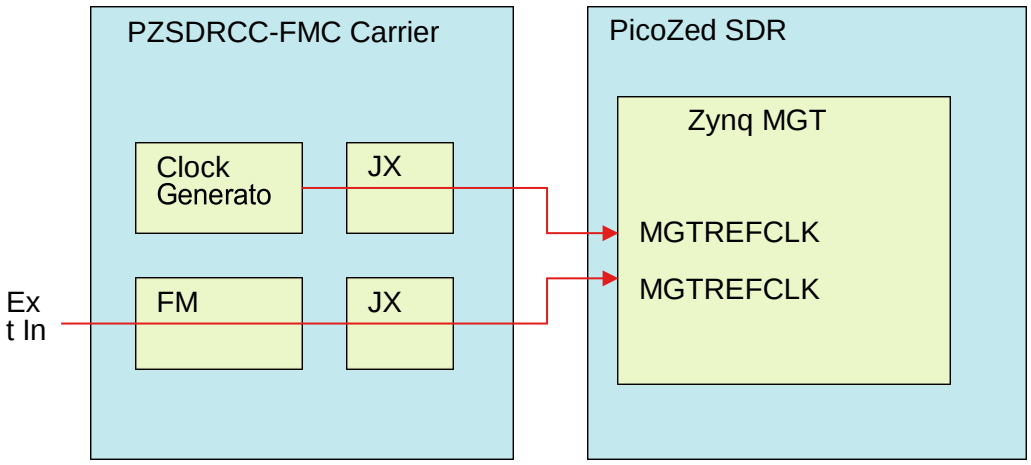


Figure 10 – Clock Source for MGT Transceivers

		Carrier I/O Connector		B2B Connector		SDR2x2 Rev C	SDR2x2 Rev D and later
GTX Name	Description	Reference Designator	Pin	Reference Designator	Pin	Bank 111 Pin	Bank 112 Pin
MGT0	FMC Rx+	P2	C6	JX1	88	AD8	AB4
	FMC Rx-	P2	C7		90	AD7	AB3
	FMC Tx+	P2	C2	JX3	8	AF8	AA2
	FMC Tx-	P2	C3		10	AF7	AA1
MGT1	SFP+ Rx +	P1	12	JX1	91	AE6	Y4
	SFP+ Rx -	P1	13		93	AC5	Y3
	SFP+ Tx +	P1	18	JX3	13	AF4	W2
	SFP+ Tx -	P1	19		15	AF3	W1
MGT2	SMA Rx+	J6		JX1	92	AC6	V4
	SMA Rx-	J5			94	AD3	V3
	SMA Tx+	J4		JX3	14	AE2	U2
	SMA Tx-	J3			16	AE1	U1
MGT3							
REFCLK 0	FMC Clk+	P2	D4	JX1	87	W6	R6
	FMC Clk-	P2	D5		89	W5	R5
REFCLK 1	Clock Gen +	U21	35	JX3	2	AA6	AB7
	Clock Gen -	U21	34		4	AA5	AB8

Table 17 – MGT Pin Connections

2.10.1 SMA Data TX/RX_P/N Pairs

The carrier card has four MGT Data SMA female connectors (J3, J4, J5, J6) for differential TX_P/N and RX_P/N data connections. The TX path includes capacitors for DC blocking. The RX path does not include capacitors for DC blocking. If DC blocking is required for your application, Avnet recommends using an inline capacitor (e.g., Fairview part). For more information, see:
http://www.fairviewmicrowave.com/inner-dc-block-5-mhz-18-ghz-sma-connectors-sd3241-p.aspx.

2.11 SMA Connectors and Functions

Multiple SMA connectors are available on the carrier to inject or export high frequency clock and data signals, as summarized in the table.

SMA Connector	Description	Direction	Refer to
J1	External AD9361 Reference Clock Input	Input	See External AD9361 Clock
J2	Clock Synthesizer Programmable Output	Output	See Clock Synthesizer IC
J3	SDR2x2 MGT TXN	Output	See SMA Data TX/RX_P/N Pairs
J4	SDR2x2 MGT TXP		
J5	SDR2x2 MGT RXN	Input	See SMA Data TX/RX_P/N Pairs
J6	SDR2x2 MGT RXP		
J7	External Reference Clock for Clock Synthesizer U21	Input	See Clock Synthesizer IC

Table 18 – SMA Connectors and Functions

FOR CONNECTOR LOCATIONS, REFER TO FIGURE 1: FEATURE LOCATIONS.

2.12 USB UART

The PicoZed SDR FMC Carrier Card implements a USB-to-UART bridge (P10) connected to a Zynq PS UART peripheral on the SOM. U4 is a Silicon Labs CP2103-GM USB-to-UART bridge device that allows connection to a host computer via USB. The CP2103 connects to the USB Micro AB connector, P10. Basic TXD/RXD connection is implemented. When the port is not in suspend mode, LED DS2 illuminates.

The USB UART interface is designed to operate in bus powered mode. In this mode, the UART is powered solely from the host PC's USB connection. This mode does not require the carrier to be turned on. Once enumeration is complete, the communication port with the PC remains persistent as long as the USB cable is plugged in. The carrier may be power cycled or reset without loss of the port connection. This is useful in the event where you want to monitor the UART outputs on a terminal window.

Silicon Labs provides royalty-free Virtual COM Port (VCP) drivers which permit the CP210x USB-to-UART bridge to appear as a COM port to host computer communications application software (e.g., HyperTerminal or Tera Term). Refer to the Silicon Labs CP210x USB-to-UART Setup Guide.

Visit http://zedboard.org/sites/default/files/documentations/CP210x_Setup_Guide_1_2_1.pdf for driver installation guide on PC.

The UART1 Zynq PS peripheral is accessed through MIO Bank 1/501 (1.8V).

Carrier Net Name	B2B Connector Pin	Zynq PL Pin	Zynq Bank	Bank Voltage
USB_UART_RXD	JX4 Pin 99	B21	501	1.8V
USB_UART_TXD	JX4 Pin 98	A18	501	1.8V

Table 19 – UART Connections

2.12.1 USB-UART Circuit Protection

USB data lines, D+/-, and Vbus lines are ESD protected with Littelfuse TVS diode, SESD0201X1UN-0020-09.

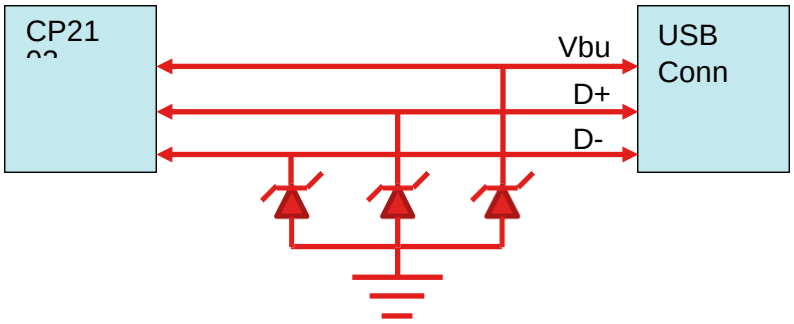


Figure 11 – USB-UART Circuit Protection

2.13 USB 2.0 OTG Interface

A USB Type A connector (P19) is routed to the PicoZed SDR SOM via header JX3 pins 63, 67, 68, 69, and 70. In USB OTG Host mode (default), this interface sources 5.0V power onto the USB_VBUS rail via power switch (U16) when an active high control signal is present on USB_OTG_CPEN (JX3.70).

The USB_OTG_ID signal is brought out to JX3.63 to allow the SOM to determine host or device selection. When grounded the interface is initially set to host mode, when floating the interface is in device mode. Once connected, the roles can change via the Host Negotiation Protocol (HNP).

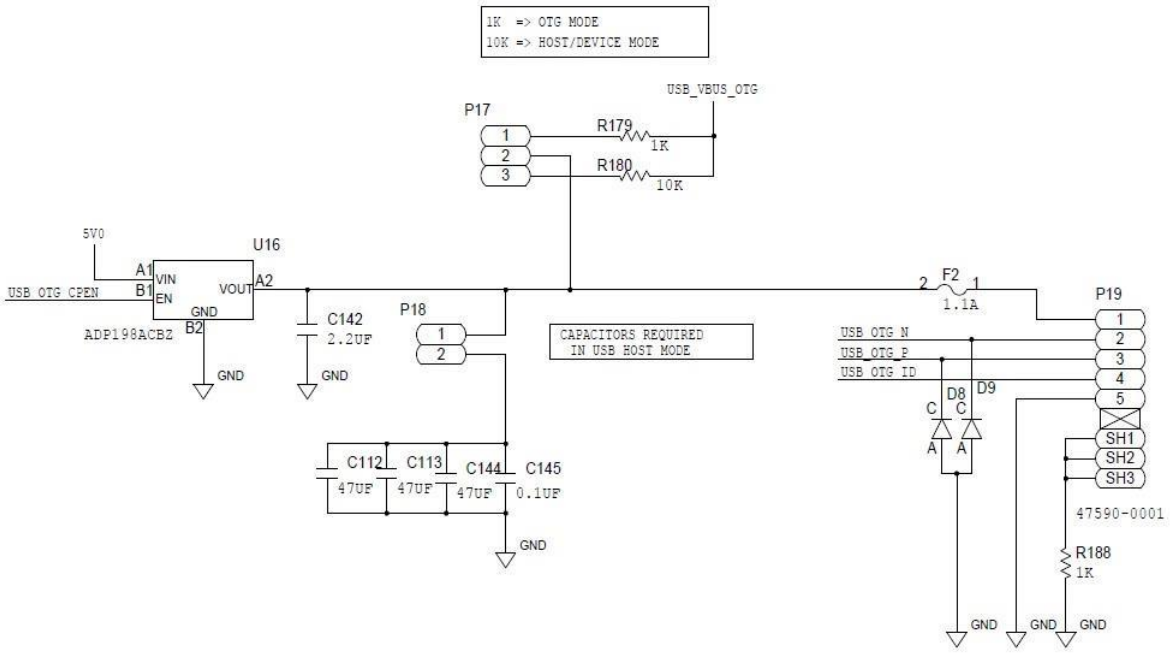


Figure 12 – USB OTG Circuit

The factory default for PicoZed SDR FMC Carrier Card is set to OTG mode with pin 1-2 shorted in P17. To change to USB Host mode, change the jumper to short pin 2-3.

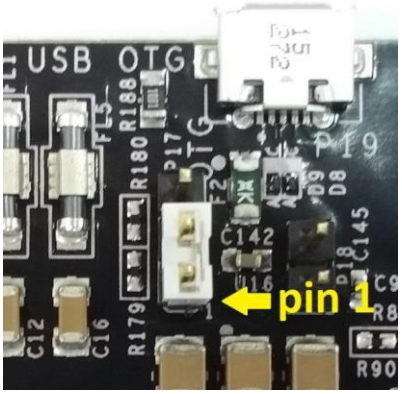


Figure 13 – Factory Default USB OTG Setting

2.13.1 USB 2.0 OTG Interface Protection

The USB 2.0 OTG interface is doubly protected – on the carrier card and on the SOM. On the carrier card, data lines (D+/-) are ESD protected using a Littelfuse TVS diode SESD0201X1UN-0020-09. Vbus is protected by a 1.1A fuse to prevent over current damages to power switch U16.

After the USB data signals propagate to the SOM side, they are further protected by ESD and EFT TVS diode U16.

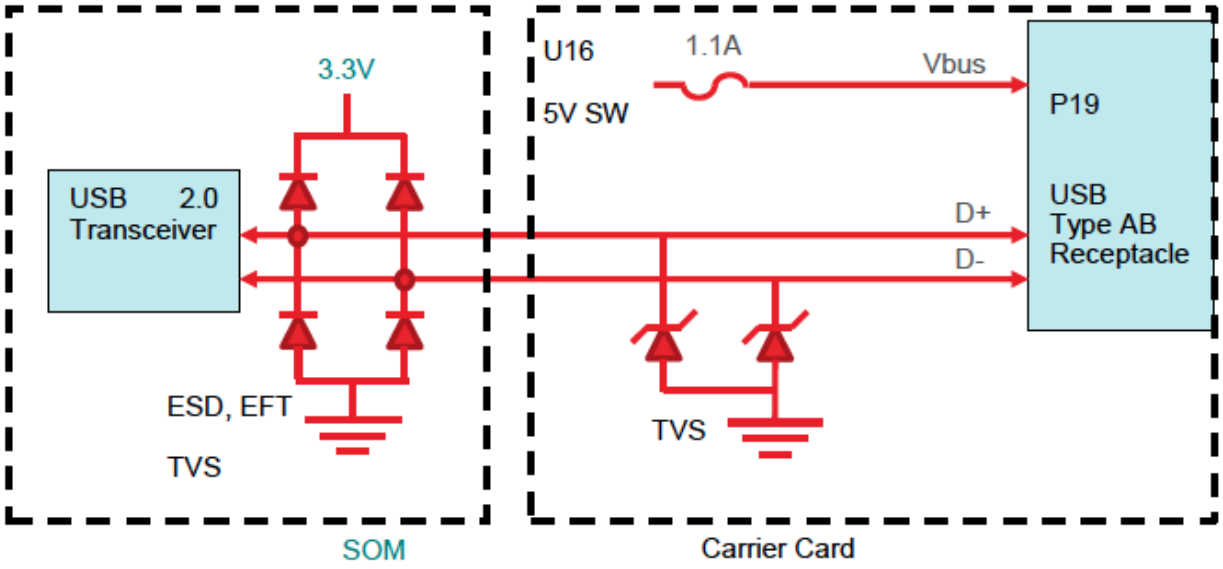


Figure 14 – USB 2.0 OTG Protection

SOM Net Name	Carrier Net Name	B2B Connector Pin
USB_ID	USB_OTG_ID	JX3 Pin 63
USB_VBUS_OTG	USB_VBUS_OTG	JX3 Pin 68
USB_OTG_CPEN	USB_OTG_CPEN	JX3 Pin 70
USB_OTG_P	USB_OTG_P	JX3 Pin 67
USB_OTG_N	USB_OTG_N	JX3 Pin 69

Table 20 – USB OTG Pin Connections

2.14 Ethernet Ports

There are two RJ45 connectors, M1 and M2, for 10/100/1000 Ethernet connectivity on the PicoZed SDR FMC Carrier Card. This figure gives a high level overview of the connection:

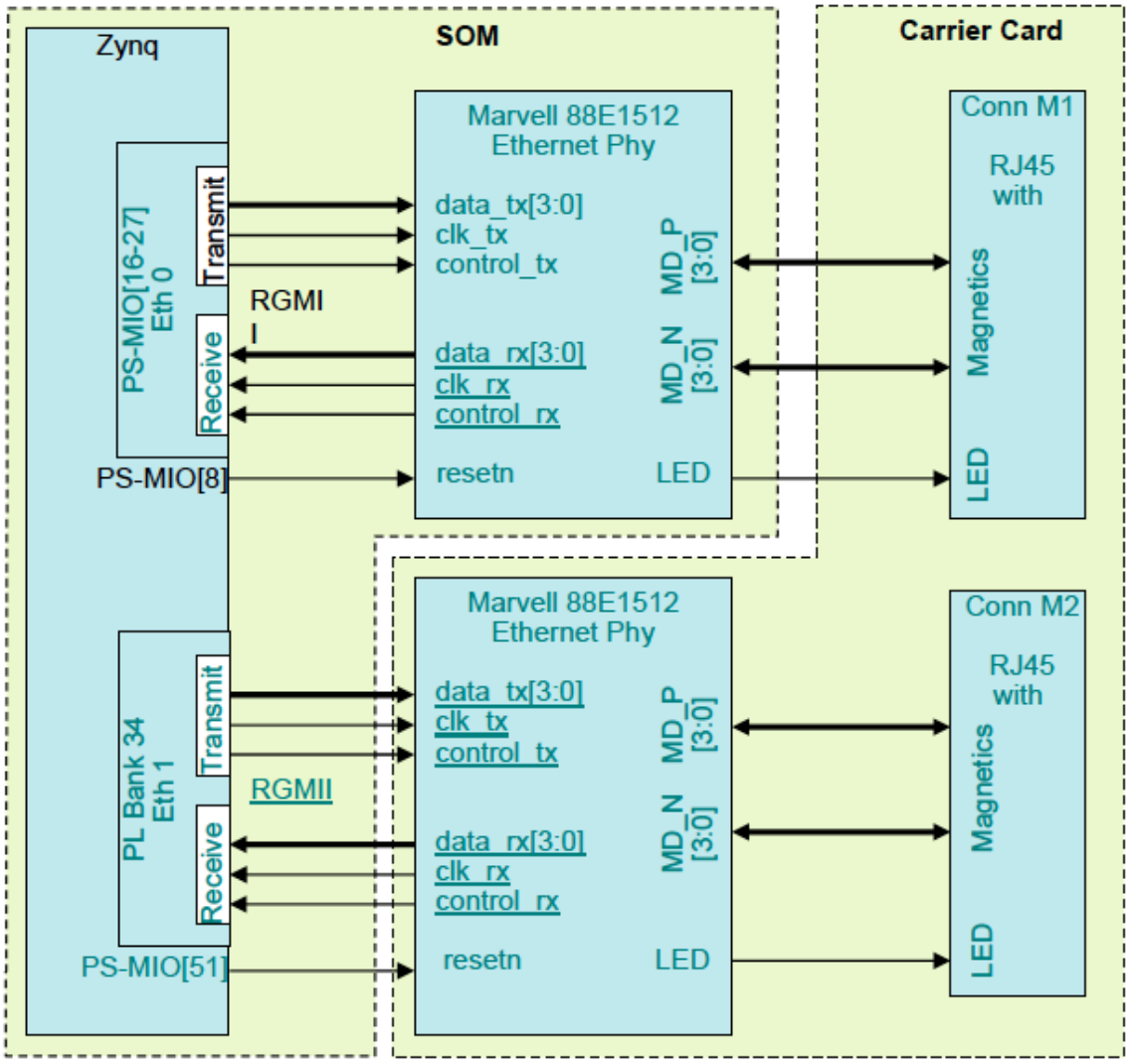


Figure 15 – Overview of Ethernet interface

2.14.1 Ethernet 1

The port labelled Ethernet 1 on the carrier (M1) implements a *copper* connection by providing a connector and integrated transformers, while using the 10/100/1000 Mbps Ethernet PHY on the SOM. The SOM has a label printed with a unique Ethernet MAC, which you can assign to this port in Linux.

The PHY differential pairs (RX/TX) connect to the Zynq PS Bank 501. The SOM and carrier use the same Marvell PHY device (88E1512-56QFN). The circuit design of the SOM PHY is also the same as the carrier card. The carrier Ethernet connector (M1) is the same MagJack L829-1J1T-43 used for connector M2.

Besides Ethernet signals, link status, and link speed, LED control signals are passed through B2B control signals to control LEDs on M1.

Carrier Net Name	B2B Connector Pin	Carrier Net Name
ETH0_MD1_P	JX3 Pin 51	ETH_MD1_P
ETH0_MD1_N	JX3 Pin 53	ETH_MD1_N
ETH0_MD2_P	JX3 Pin 52	ETH_MD2_P
ETH0_MD2_N	JX3 Pin 54	ETH_MD2_N
ETH0_MD3_P	JX3 Pin 57	ETH_MD3_P
ETH0_MD3_N	JX3 Pin 59	ETH_MD3_N
ETH0_MD4_P	JX3 Pin 58	ETH_MD4_P
ETH0_MD4_N	JX3 Pin 60	ETH_MD4_N
ETH0_PHY_LED0	JX3 Pin 47	ETH_PHY_LED0
ETH0_PHY_LED1	JX3 Pin 48	ETH_PHY_LED1

Table 21 – M1 Ethernet Connections

2.14.2 Ethernet 2

The port labelled Ethernet 2 on the carrier (M2) implements a *copper* connection by providing a connector, integrated transformers, and the physical layer device (PHY). The PHY differential pairs (RX/TX) connect to the Zynq PL I/O using an RGMII bus. This allows you to either use one of the Zynq PS Ethernet MACs, routed through the Zynq PL I/O using the Zynq EMIO interface, or use a Zynq PL-based Ethernet MAC IP. The carrier has a label printed with a unique Ethernet MAC, which you can assign to this port in Linux.

The carrier card PHY (U11) is a Marvell 88E1512-56QFN 10/100/1000 Ethernet PHY. The RGMII interface is connected to Zynq PL Bank 34 (1.8V) on the SOM. The PHY can be controlled via SMI bus (MDIO, MDC) which is also connected to Zynq PL Bank 34 (1.8V).

The M2 connector is a MagJack L829-1J1T-43 and contains integrated magnetics and two LEDs for connection indication.

At power up, the PHY is automatically reset by PG_MODULE signal. The PHY can also be reset by the Zynq PL I/O. The CONFIG pin of the PHY is pulled high.

Carrier Net Name	B2B Connector Pin	SDR2x2 Pin	Zynq Bank	Bank Voltage	SDR1x1 Net Name	SDR1x1 Pin
ETH1_TXD0	JX4 Pin 52	D6	34	1.8V	ETH0_TX_D0	E14
ETH1_TXD1	JX4 Pin 54	C6	34	1.8V	ETH0_TX_D1	D10
ETH1_TXD2	JX4 Pin 57	C9	34	1.8V	ETH0_TX_D2	B18
ETH1_TXD3	JX4 Pin 59	B9	34	1.8V	ETH0_TX_D3	A17
ETH1_TX_CLK	JX4 Pin 51	C8	34	1.8V	ETH0_TX_CLK	A19
ETH1_TX_CTRL	JX4 Pin 53	C7	34	1.8V	ETH0_TX_CTL	F14
ETH1_RXD0	JX4 Pin 42	E6	34	1.8V	ETH0_RX_D0	D11
ETH1_RXD1	JX4 Pin 44	D5	34	1.8V	ETH0_RX_D1	A16
ETH1_RXD2	JX4 Pin 45	F8	34	1.8V	ETH0_RX_D2	F15
ETH1_RXD3	JX4 Pin 47	E7	34	1.8V	ETH0_RX_D3	A15
ETH1_RX_CLK	JX4 Pin 46	G7	34	1.8V	ETH0_RX_CLK	B17
ETH1_RX_CTR	JX4 Pin 48	F7	34	1.8V	ETH0_RX_CTL	D13
ETH1_MDC	JX4 Pin 58	B10	34	1.8V	ETH0_MDC	C10
ETH1_MDIO	JX4 Pin 60	B9	34	1.8V	ETH0_MDIO	C11

Table 22 – M2 Ethernet Connections

2.15 EEPROM

The carrier card provides a 32kb I2C serial EEPROM (U6) for parameter storage. The part number is AT24C32D-SSHM-B. The EEPROM has three address pins (A0-A2) that can be used to modify its I2C address. These pins are all pulled down on the carrier card, so the I2C address for EEPROM is 0xA0. The EEPROM connects to the PicoZed SDR SOM through I2C MUX described in *I2C Address Space and Registers*.

The device has a write protect pin that inhibits writes if pulled high or automatically pulls down internally if left unconnected. The carrier card design left the pin floating, meaning write is ALLOWED. You can inhibit writes to the device by mounting R148 (4.7k).

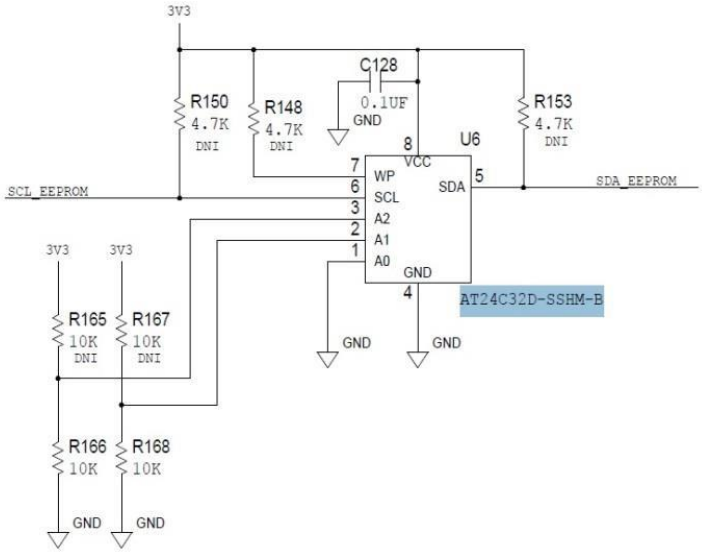


Figure 16 – EEPROM U6

2.16 HDMI Interface

The carrier has an HDMI V1.4 (DVI V1.0 compatible) video output port (P4). The data is configured for the YCbCr 4:2:2 format (16-bits). HDMI signals are driven by an HDMI transmitter (U1), the Analog Devices ADV7511 225MHz HDMI IC, capable of transmitting up to 1080p resolution video.

The carrier HDMI transmitter is only accessible with a PicoZed SDR 2x2 SOM (AES-Z7PZ-SDR2-G). Video data comes from Zynq PL Bank 33 through JX1 (see *Table 23 – HDMI Connections*).

The ADV7511 is configured via the I2C interface at address 0x72 and by pulling the PD pin low. You can assert PD pin high to change the I2C address to 0x7A.

LED DS1 is used to indicate a Hot Plug Detect signal when a valid HDMI connection is made. A carrier LED (DS1) turns on when this occurs.

To ensure low EMI emissions, all power pins are filtered using chip power filters and decoupling caps. High frequency signals between the transmitter and connector are filtered using DC chokes. Additionally, the data signals to P4 are ESD protected using ESD protection diodes. Varistor V1 is used to protect the CEC signal.

The functions and circuit implementation for ADV7511 are beyond the scope of this document. Refer to the Analog Devices ADV7511 datasheet, Hardware User's Guide, and Programming Guide at www.analog.com for detailed information. The Analog Devices Engineer Zone is a very useful source of information (https://ez.analog.com/welcome). Detailed information on the ADV7511, including a hardware user guide and example schematics/layout, can be found at http://ez.analog.com/docs/DOC-1740.

Carrier Net Name	B2B Connector Pin	Zynq PL Pin	Zynq Bank	Bank Voltage
HDMI_D35	JX1 Pin 75	G1	33	1.8V
HDMI_D34	JX1 Pin 73	H2	33	1.8V
HDMI_D33	JX1 Pin 70	K1	33	1.8V
HDMI_D32	JX1 Pin 68	K2	33	1.8V
HDMI_D31	JX1 Pin 69	H3	33	1.8V
HDMI_D30	JX1 Pin 67	H4	33	1.8V
HDMI_D29	JX1 Pin 64	H1	33	1.8V
HDMI_D28	JX1 Pin 62	J1	33	1.8V
HDMI_D27	JX1 Pin 63	E3	33	1.8V
HDMI_D26	JX1 Pin 61	F3	33	1.8V
HDMI_D25	JX1 Pin 56	E1	33	1.8V
HDMI_D24	JX1 Pin 54	E2	33	1.8V
HDMI_D23	JX1 Pin 49	C1	33	1.8V
HDMI_D22	JX1 Pin 47	D1	33	1.8V
HDMI_D21	JX1 Pin 44	F2	33	1.8V
HDMI_D20	JX1 Pin 42	G2	33	1.8V
HDMI_VSYNC	JX1 Pin 41	D4	33	1.8V
HDMI_HSYNC	JX1 Pin 43	F4	33	1.8V
HDMI_CLK	JX1 Pin 74	L3	33	1.8V
HDMI_DE	JX1 Pin 76	K3	33	1.8V
HDMI_INTN	JX1 Pin 10	L9	33	1.8V
HDMI_PD	JX1 Pin 9	N8	33	1.8V
HDMI_SPDIF	JX1 Pin 35	G4	33	1.8V
HDMI_SPDIF_OUT	JX1 Pin 37	F4	33	1.8V

Table 23 – HDMI Connections

2.17 SD Card Interface

The carrier has an SD Card interface (P13) that connects to the Zynq PS SD/SDIO peripheral. The SD card can be used for non-volatile external memory storage as well as booting the Zynq PS peripheral sd0 which is connected through Bank 1/501 MIO[40-45], including Card Detect.

The SD Card, a 3.3V interface, is connected through MIO Bank 1/501 which is set to 1.8V. Voltage translation is performed by a Texas Instrument TXS02612RTWR voltage level translator IC on board PicoZed SDR SOM. The translator also implements a switch that allows you to select between the microSD card on the PicoZed SDR SOM and the standard SD card on the carrier. The selection is done by a slider switch (S1) on the PicoZed SDR SOM. When S1 is set to short pin 1-2, the microSD card is selected to connect to the Zynq SOC and the SD card on the carrier card is isolated. When pin 2-3 is shorted, the reverse is true.

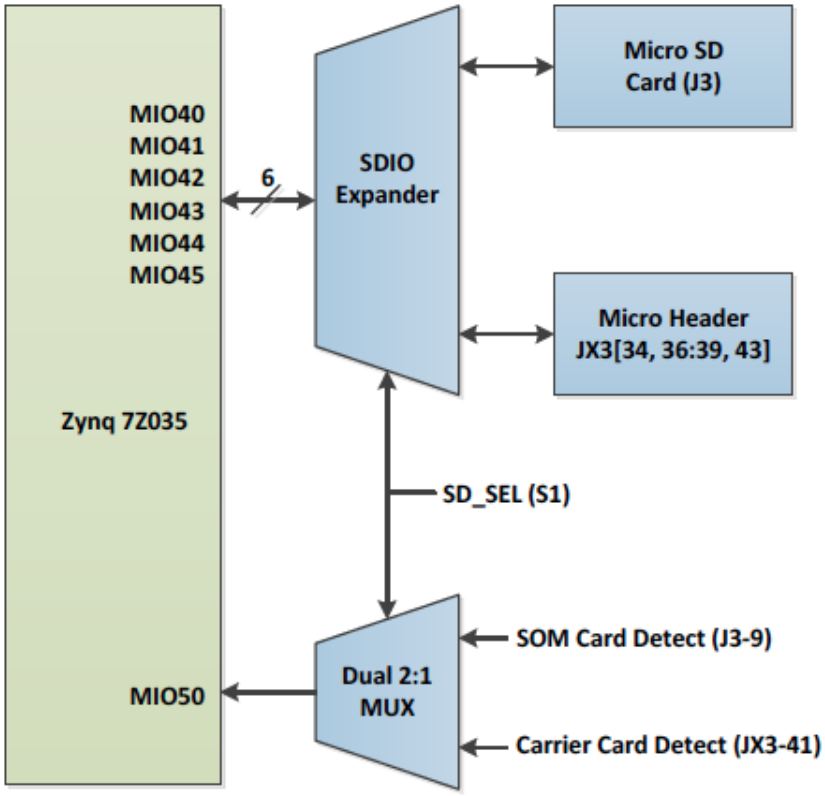


Figure 17 – SOM SD Card Switch Circuit

The SD card connector is a Molex 067840-8001. A class 10 card, or better, is recommended. Up to 32 GB is supported.

Carrier Net Name	B2B Connector Pin	SDR2x2 Pin (translated)	SDR2x2 Bank	Bank Voltage	SDR1x1 Net Name	SDR1x1 Pin
SD1_B_DAT0	JX3 Pin 37	F17	501	1.8V	SD0_DATA0	E12
SD1_B_DAT1	JX3 Pin 36	D18	501	1.8V	SD0_DATA1	A9
SD1_B_DAT2	JX3 Pin 39	E18	501	1.8V	SD0_DATA2	F13
SD1_B_DAT3	JX3 Pin 38	C18	501	1.8V	SD0_DATA3	B15
SD1_B_CLK	JX3 Pin 43	C22	501	1.8V	SD0_CLK	D14
SD1_B_CMD	JX3 Pin 34	C19	501	1.8V	SD0_CMD	C17
SD1_B_CDN	JX3 Pin 41	B22	501	1.8V	SD0_CD	B13

Table 24 – SD Card Connections

2.18 Fan Header

The carrier card provides a three pin 0.1” pitch fan header, Molex 22-23-2031, (P7) that allows you to add a cooling solution. The interface follows common 5V DC fan standard so you can purchase the fan easily from a third party vendor.

You may throttle FAN_PWM signal using PWM to control fan speed. The connector also provides a tachometer signal to the PizoZed SDR SOM.

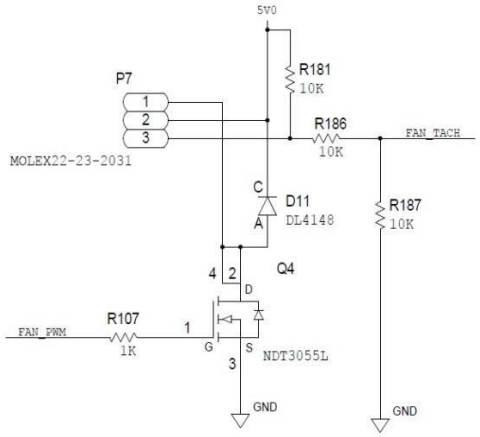


Figure 18 – Fan Circuit

Carrier Net Name	B2B Connector Pin	Zynq PL Pin (Translated)	Zynq Bank	Bank Voltage
FAN_TACH	JX4 Pin 70	A7	501	1.8V
FAN_PWM	JX3 Pin 68	B7	501	1.8V

Table 25 – Fan Signal Connections

2.19 JTAG

An auto-switching JTAG interface port (P15) is provided on the carrier card, a PC4 compliant connection. The PicoZed SDR SOM does not have a connector for its JTAG signals. All JTAG signals are routed to the carrier card connector. The JTAG chain design also automatically inserts the FMC JTAG interface into the JTAG chain when an FMC card is inserted. The detection is done using FMC_PRSNT signal.

A Xilinx JTAG platform cable (HW-USB-II-G) or a Digilent JTAG HS2 or HS3 programming cable should be used when programming via these ports.

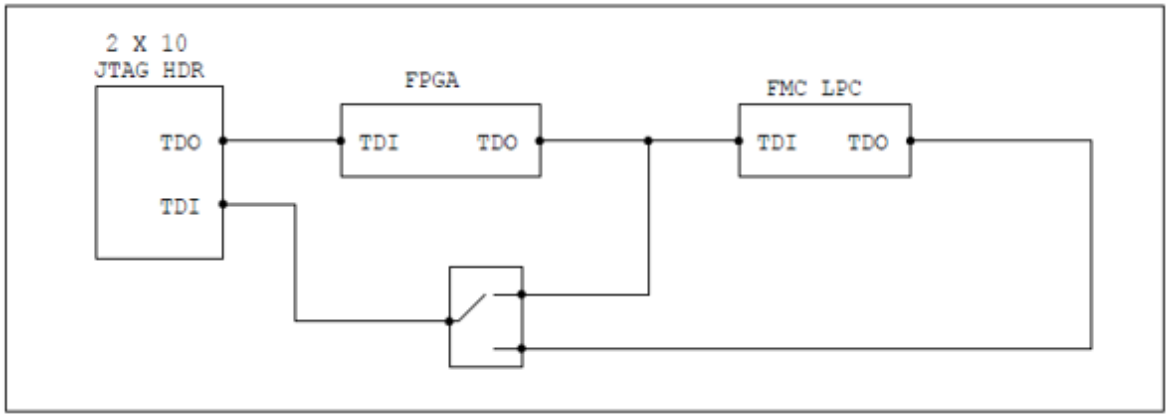


Figure 19 – JTAG Chain

A blue DONE LED (D4) is connected to the Zynq SOM via JX1.8, net name Zynq PL_DONE. When the Zynq PL is configured, this pin is driven high by the Zynq PL which turns the carrier's DONE LED on.

2.20 Audio

The carrier provides dual stereo input and output audio jacks (P5, P6), connected to a 96KHz sampling rate, 24-bit stereo audio codec (U3). The CODEC interfaces to Zynq PL Bank 34.

The codec can output two and input two audio streams simultaneously. The two output streams can select from a combination of differential or single-ended drivers. On the carrier card, single-ended left and right headphone drivers (LHP and RHP) are brought out to the connector P5-A 3.5mm jack. Single-ended line out drivers are also brought out to P5-B.

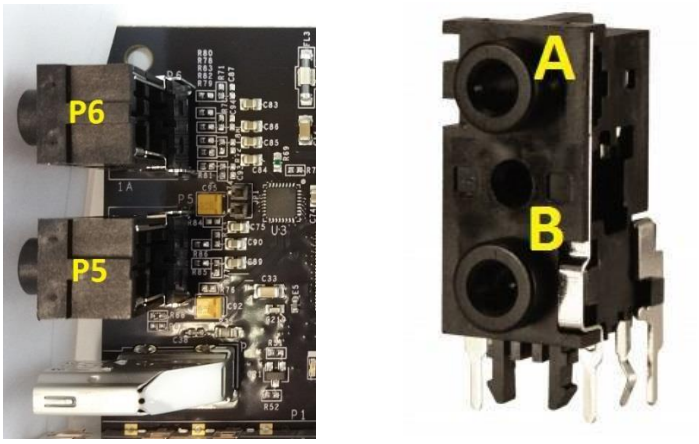


Figure 20 – Audio Jack P5 P6 Arrangement

All output drivers are AC coupled with large capacitors to ensure good frequency response throughout the audible range. However, you can experiment with DC coupling for headphone interface P5-A by modifying the circuit to provide virtual ground. To do so, solder R87, R84, and R76. Then de-solder R88, C95, and C92. It is also necessary to change codec control registers to enable DC coupling.

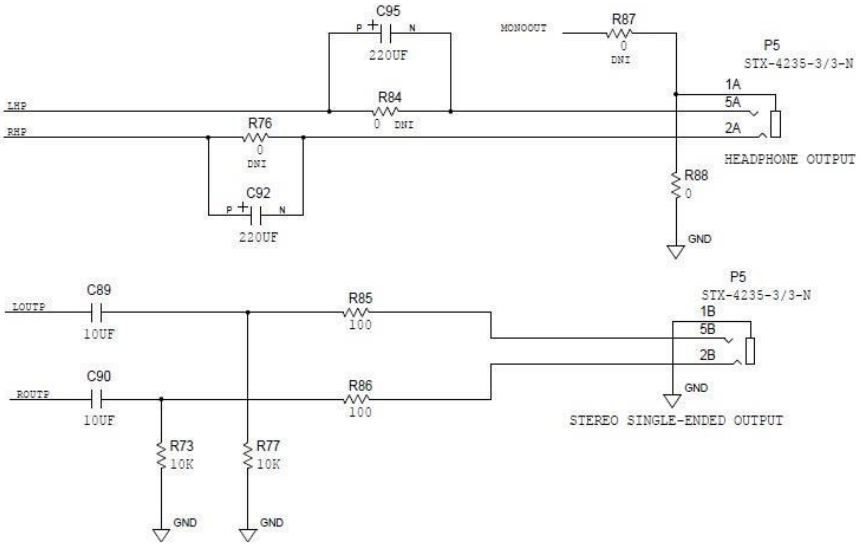


Figure 21 – Audio Output Coupling

The carrier card also wires up the codec to receive stereo input from two 3.5 mm jacks, P6-A and P6-B. Each jack can receive two channels of audio. Jack P6-A is suitable for connecting to a stereo microphone as it provides mic bias voltage to power electret microphones. P6-B is intended to receive line level signals.

The codec is controlled by I2C bus: net names SCL_ADAU1761_1V8 and SDA_ADAU1761_1V8. The I2C bus is connected to the PicoZed SDR SOM PL Bank 13 through an I2C MUX. The I2C MUX circuit is described in *I2C Address Space and Registers*.

2.21 Camera Connector

The carrier card provides a female edge connector (P9) for interfacing the SOM with Avnet's camera modules. These modules present a standard PCI Express x4 male edge connector; therefore the carrier uses the female mating connector. No interoperability with the PCI Express electrical or signaling specification is supported.

An example of an Avnet camera module is the ON PYTHON-1300-C Camera Module. Information about the module and the interface are posted on the product website at http://picozed.org/product/python-1300-c-camera-module.

The carrier camera interface adheres to Avnet's interface pinout. The following signals are available as single-ended or differential:

- Camera data (8 bits)
- Camera clock
- Camera reference clock
- Camera Sync

The following control signals are single-ended:

- I2C signals (SCL, SDA)
- Camera SPI (MOSI, MISO, EN, CLK)
- GPIO (9 bits)

The interface also provides 1.8V and 5.0V power. By moving the R268 0 ohm resistor to R269 (DNI), it routes 3.3V instead of 1.8V to the connector.

2.22 RF Connector

RF Personality cards specially designed for PicoZed SDR can boost the transmitter output using a power amplifier (PA) and increase the dynamic range of the receiver input with a low-noise amplifier (LNA) or other functionalities such as up/down conversion outside the range of the AD936x.

These cards are attached to the carrier at connector (P3).

An example of an RF Personality card is the Analog Devices AD-PZSDR2400TDD-EB. You can find more information at:
http://www.analog.com/en/design-center/evaluation-hardware-and-software/evaluation-boards-kits/ad-pzsdr2400tdd-eb.html#eb-overview

Control and monitor signals are passed between the RF card and carrier using carrier connector (P3), which is a 40-pin vertical SMD component. RF signals are connected between the SOM and RF card using 35mm U.FL coaxial cables, providing access to the transmit and receive inputs of the AD936x. The carrier also includes mounting holes that can be used to secure the RF card to the carrier.

Figure 22 shows the AD-PZSDR2400TDD-EB RF Personality card between the antenna and the PicoZed SDR 2x2 SOM; all connected to the FMC Carrier.

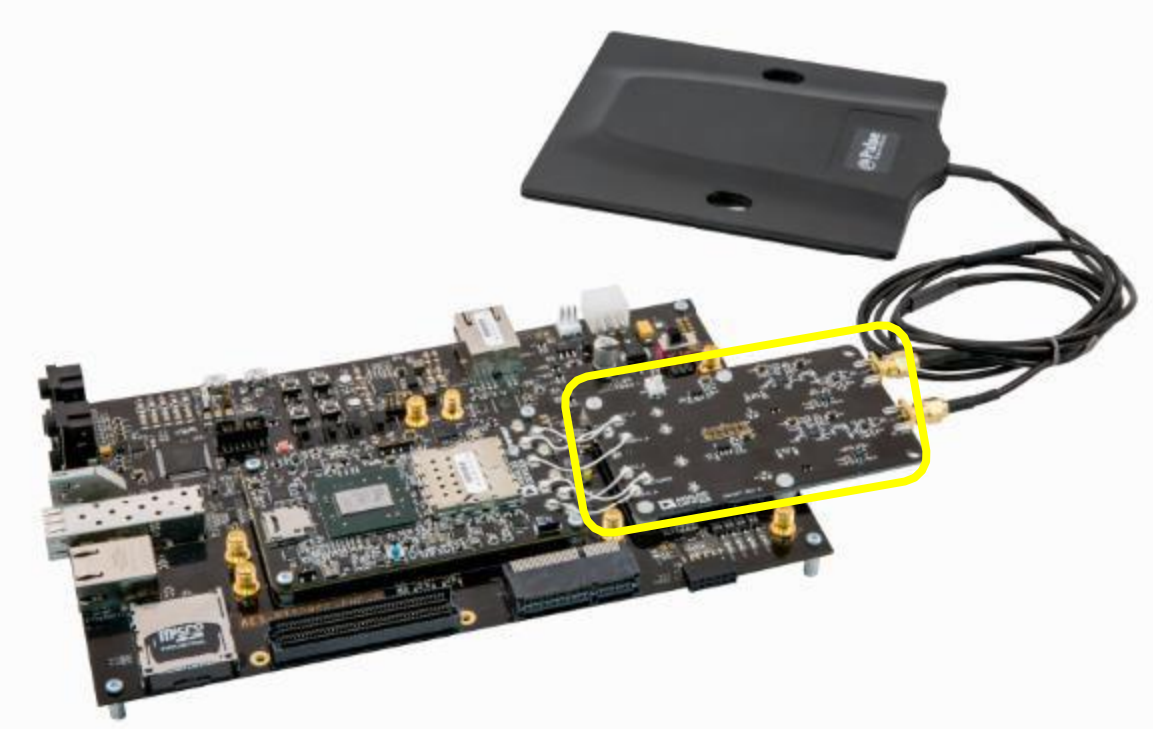


Figure 22 – RF Personality Card Connection

The signals defined by the RF Personality card connector are summarized in the following table:

Signal Name	Description	SDR2x2 Zynq Pins	SDR1x1 Zynq Pins
AD9361_GPO[0:3]	General purpose outputs from AD936x on the SOM.	N/A	N/A
AD9361_AUXADC[0:1]	Auxiliary ADC input to AD936x on the SOM.	N/A	N/A
MEAS_RF1_8V MEAS_RF2_8V	Analog signals from the RF card sampled by the carrier AD7291 (U7), which communicates to the SOM over I2C. Connected to the AD7291at VIN6 and VIN7, respectively.	N/A	N/A
AD9361_CLK	Clock input to carrier at SMA (J1), routed the AD936x on the SOM and the RF card.	N/A	N/A
SCL_RF SDA_RF	I2C signals for the RF card, routed to the SOM through the carrier I2C mux (U9).	AF24 AF25	TBD
AD9361_GPO_VDD	Optional supply for the AD936x GPO signals. Output @ 2.5V from the SOM. Apply a higher voltage if higher GPO voltage is required.	N/A	N/A
RF_GPIO_0_BANK13 RF_GPIO_1_BANK13 RF_GPIO_2_BANK12 RF_GPIO_3_BANK34 RF_GPIO_4_BANK34 RF_GPIO_5_BANK34	General purpose I/O between the Zynq PL, at the bank specified, and the RF card.	AA20 AB20 AA14 J9 K10 A9	TBD
VIN_SW	12V supply from the carrier.	N/A	N/A
VADJ	Adjustable I/O supply from the carrier.	N/A	N/A
5V0, 3V3, 1V8	Supplied from the carrier.	N/A	N/A

Table 26 – RF Personality Card Signals

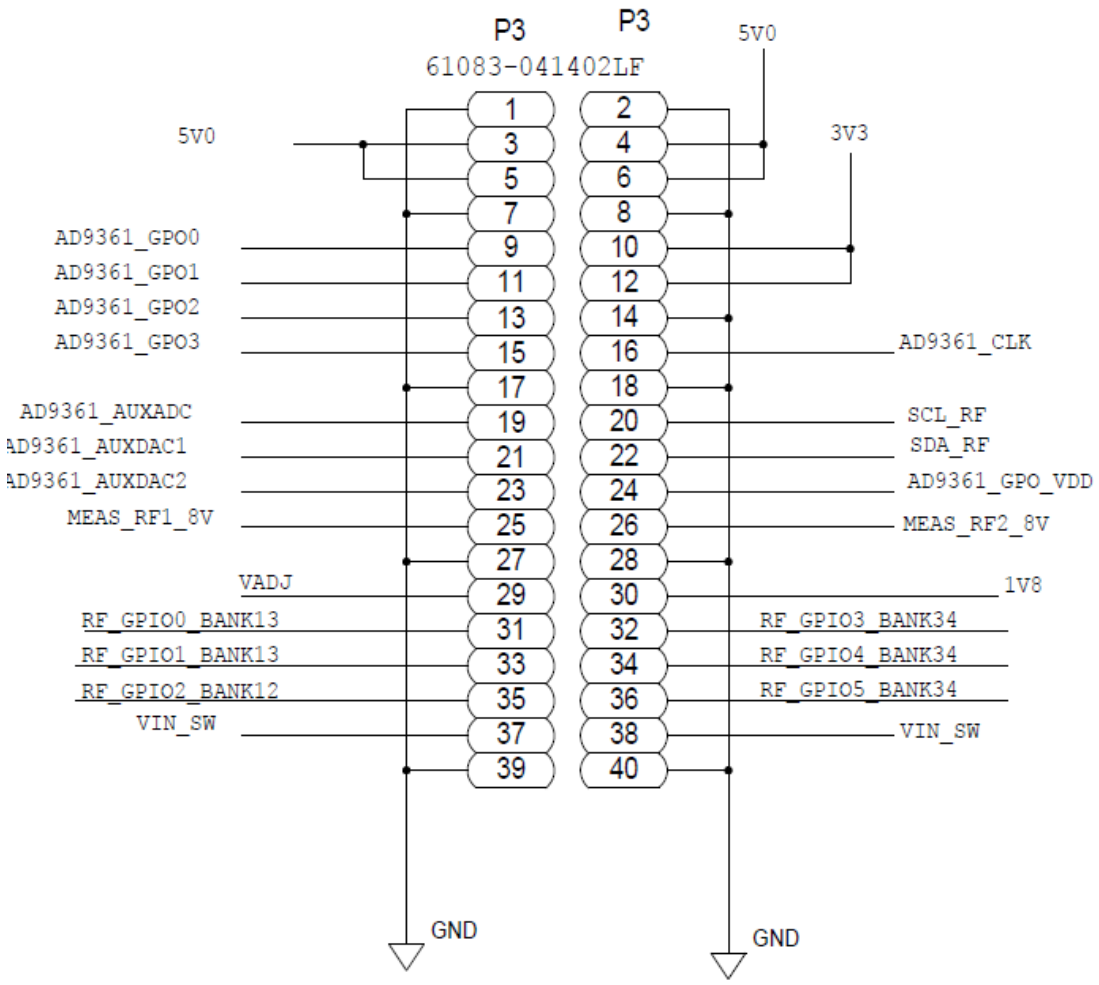


Figure 23 – RF Personality Connector

3 Power

The carrier requires an external power input (included with the kit). The carrier regulates all voltage rails required for its peripherals and those required for the SOM.

3.1 Power Input

The carrier is powered from a DC 12V supply (P20). P20 is a 2x3 6-pin right angle power connector which is NOT ATX-compatible. The connector is from Molex Mini-Fit Jr series; part number 0039301060.

CAUTION: Do not connect ATX power supplies to the carrier card in place of the supplied power adapter. The pin configuration is NOT compatible to ATX power pins.

The 12V power input is switched by S5 between OFF and ON positions. The ON/OFF positions are clearly labelled on the carrier card. In the OFF position, the 12V supply actively drives the PWR_ENABLE signal low on both the carrier card and the Picozed SDR SOM to actively shut down power ICs. When in the ON position, the 12V power input is connected to downstream power ICs.

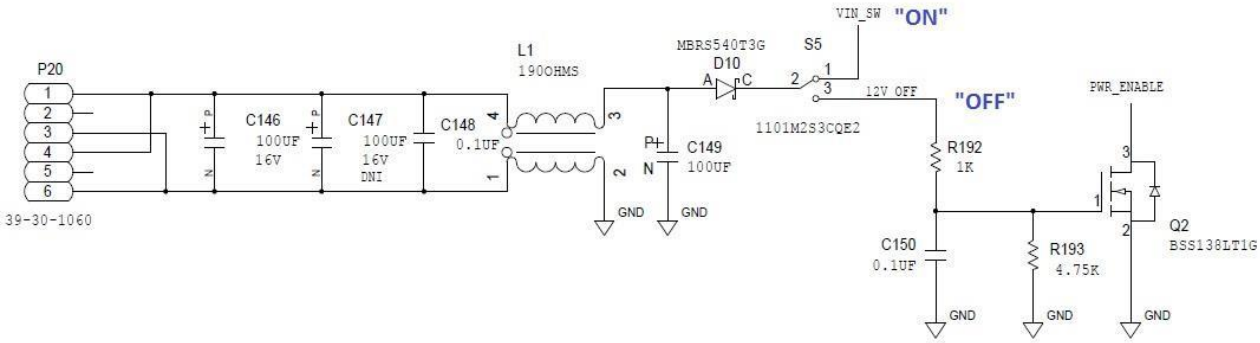


Figure 24 – Power Switch S5

The maximum input current from P20 is 5.0A. Any current exceeding this value will damage the filter network. The power supply shipped with the AES-Z7PZ-SDR2-DEV-G Kit is rated at 12V, 5.0 Amps and is recommended for use with the PicoZed SDR FMC Carrier Card.

3.2 Power Rails

The table below lists the voltage rails, currents, and tolerances.

Voltage	Tolerance (%)	IC	Max DC Current	Functional Area
12V Input	5	Wall adapter	5.0A	All Power
5V	5	U17, ADP2386ACPZN	5.0A	SOM: System Power Carrier: Clock Synthesizer U21 LDO
3.3V	5	U15, ADP2386ACPZN	5.0A	Carrier: FMC
3.3V_AD9517	1	U19, ADM7150ACPZ-3.3	800mA	Carrier: Clock Synthesizer U21
VADJ 1.8V, 2.5V or 3.3 *See VADJ Selection*	5	U8, ADP5052ACPZ	3.5A	SOM: VCCO Bank 12, 13 Carrier: RF conn P3, FMC VCCIO
1.8V	5	U8, ADP5052ACPZ	1.1A	SOM: VCCO Bank 33, 34 Carrier: VCC I2C Mux RF conn P3 HDMI Transmitter U1 Ethernet Phy U11 PMOD P14 Camera Conn P9
Audio 1.8V	5	U8, ADP5052ACPZ LDO	200mA	Carrier: Audio Codec U3
1.2V_AVTT	3	U8, ADP5052ACPZ	1.1A	SOM: MGT
1.0V_AVCC	3	U8, ADP5052ACPZ	3.5A	SOM: MGT, Core

Table 27 – Power Rail with Current Estimate

3.3 VADJ Selection

VADJ rail is configurable via P8. VADJ is an independent rail supplying power to the Zynq PL I/O banks. VADJ powers Zynq Banks 12 and 13, which are both High Range (1.2V – 3.3V) banks on the Zynq SoC in PicoZed SDR 1x1 and PicoZed SDR 2x2. The VADJ rail is also connected to the FMC interface.

P8 Jumper Position	VADJ
Open (Default)	1.8V
Short 1-2	2.5V
Short 2-3	3.3V

Table 28 – VADJ Selection

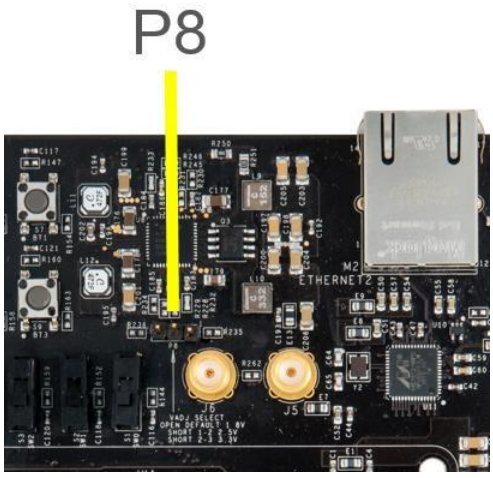


Figure 25 – Jumper Location P8

3.4 Sequencing

The carrier provides all sequencing functions required to properly bring up PicoZed SDR 1x1 and PicoZed 2x2 modules.

The PWR_EN signal, active high, JX1.5, allows the carrier to turn on or off the PicoZed power supplies. When switch S5 is set to OFF, PWR_EN is actively driven low to shut down power ICs on the PicoZed SDR SOM. The components R192, R193, and C150 have been placed to adjust the timing of this signal during power off conditions. This signal should not be de-asserted until VCCIO_EN is de-asserted.

When the power switch (S5) is turned on, 5V is first powered and the PicoZed SDR SOM powers up from this 5V. The VCCIO_EN signal, active high, JX2.10, originates on the SOM and is the output of the1.8V regulator, PG_1V8. This signal enables the carrier's 1V0_AVCC and 3V3 simultaneously. 1V0_AVCC enables 1V2_AVTT. 1V2_AVTT then enables 1.8V and VADJ simultaneously. 3.3V also enables audio 1.8V.

When the carrier is turned off (power switch turned off or power plug removed) or the PicoZed's PG_1V8 signal is de-asserted, VCCI_EN is driven low which turns off the FMC-CC supplies. 5V continues to be supplied unless the power switch S5 is set to OFF.

PG_MODULE signal, active high, JX2.11, is pulled up by the PicoZed SDR SOM to 5V. This signal can be pulled low by the carrier board power ICs, the FMC board, or the PicoZed when the board's power circuitry is not *Good* yet.

The following diagram illustrates the carrier power supply sequencing on power up.

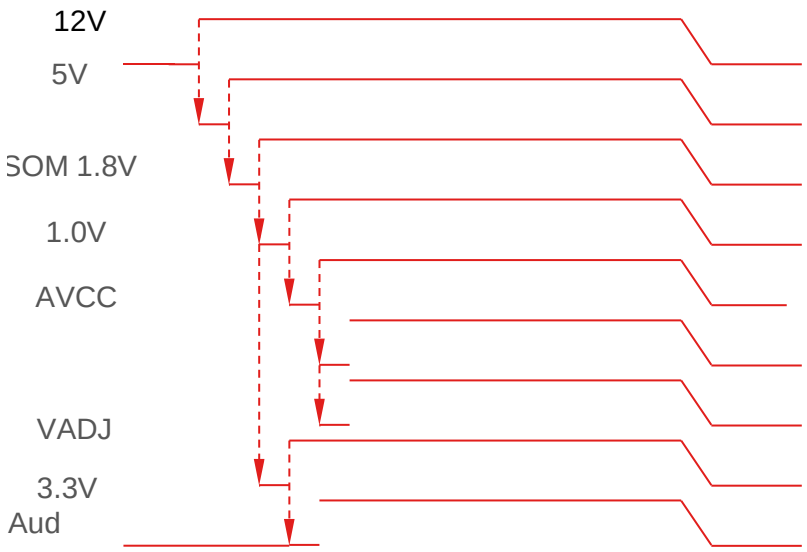


Figure 26 – Power Sequence

3.5 Power Good LEDs

The carrier uses the follow LEDs to indicate successful power up conditions:

- Red LED, DS8, illuminates when 5V is powered up.
- Green LED, D3, on the PicoZed SDR SOM illuminates when the PG_MODULE signal is asserted.

See Figure 27 below for a picture of a successfully configured system.

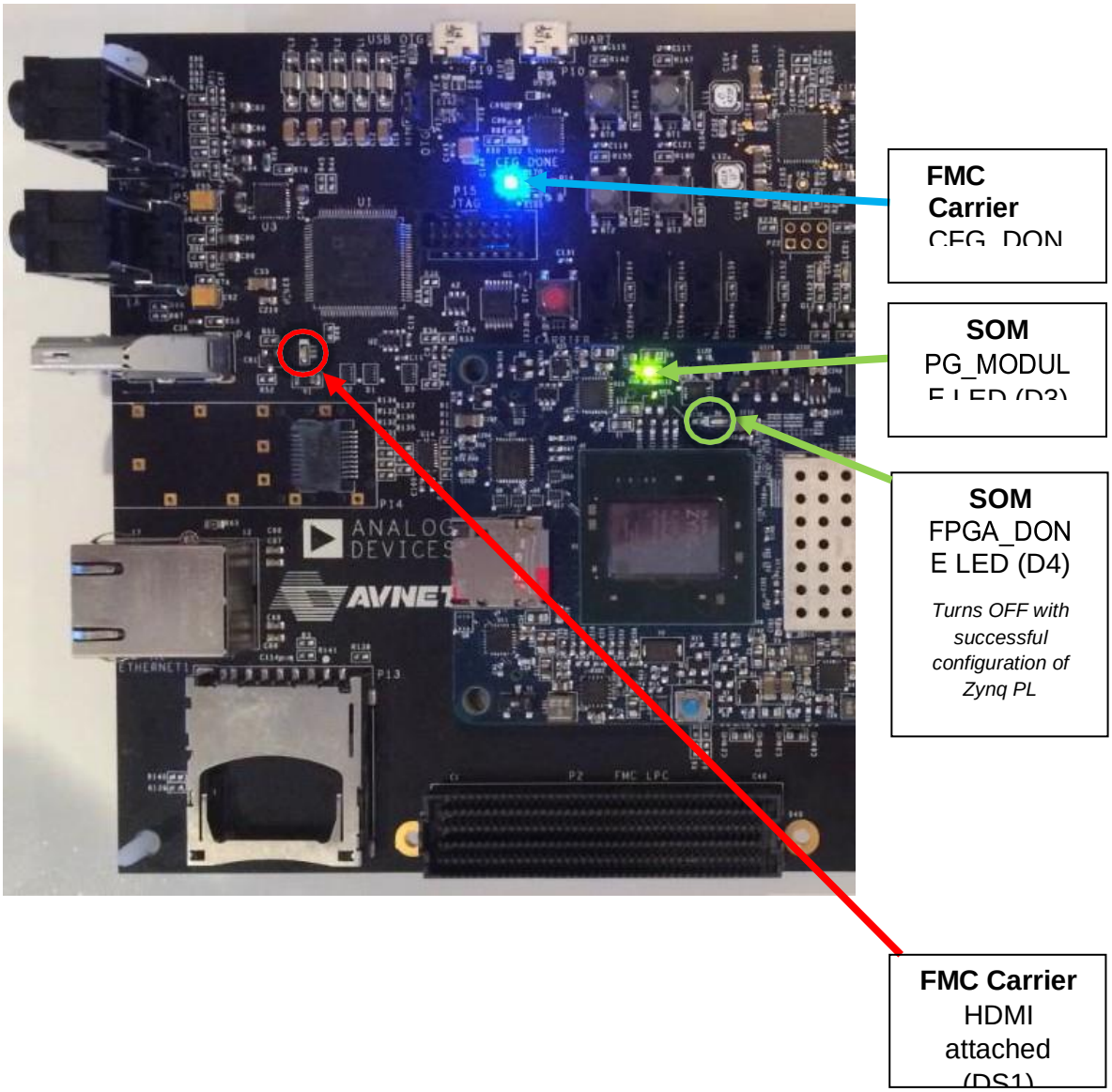


Figure 27 – Power Good LEDs

4 Jumpers, Configuration Settings, and Test Points

This table is a quick reference to all the jumpers, configuration settings, and test points on the FMC. For detailed information, refer to the appropriate sections in this document. To locate them on the carrier, refer to Figure 1, Figure 28, and Figure 29.

Reference Designator	Name	Footprint/ Connector	Notes
J1	AD9361_CLK	SMA	Clock input to AD9361 on PicoZed SDR SOM. Also fed to RF Connector.
J2	Clock Generator Test Output	SMA	Test clock out from U21 Clock Generator.
P16	Zynq PL_VBATT_TEST	2x1 0.1" header, not assembled	Connected to VCCBATT_0 pin on PicoZed SDR Zynq SOC through JX1 B2B connector. Carefully read the *SOM User Guide* regarding this feature before connecting a VBATT voltage source.
P23	Voltage Monitor Plug	3x2 0.1" header, not assembled	For probing power supply voltages **Pin** **Net** **Description** 1 VIN_SW Voltage after power switch 2 VIN_HDR 5V supply 3 1V0_AVCC 1V supply to MGT 4 1V8 1.8V supply 5 3V3 3.3V supply 6 1V2_AVTT 1.2V to MGT
TP1	PG_MODULE	Test_pad	Global power good from power IC U8.
TP2	AD9361_GPO_VDD	Raised loops, for clips, Yellow	Connected to I/O voltage for GPO pins of AD9361 on SOM through B2B connector.
TP7, TP10	Clock Generator U21 Clk in	Raised loops, for clips, Yellow	Allows you to inject custom reference clock frequencies.
TP9	Clock Generator U21 Sync in	Raised loops, for clips, Yellow	Allows you to assert clock generator U21 sync. Refer to *AD9517-3 Datasheet*.
TP12	Clock Generator U21 reference monitor	Raised loops, for clips, Yellow	Allows you to monitor health of clock source selected as reference frequency.

Table 29 – Test Points

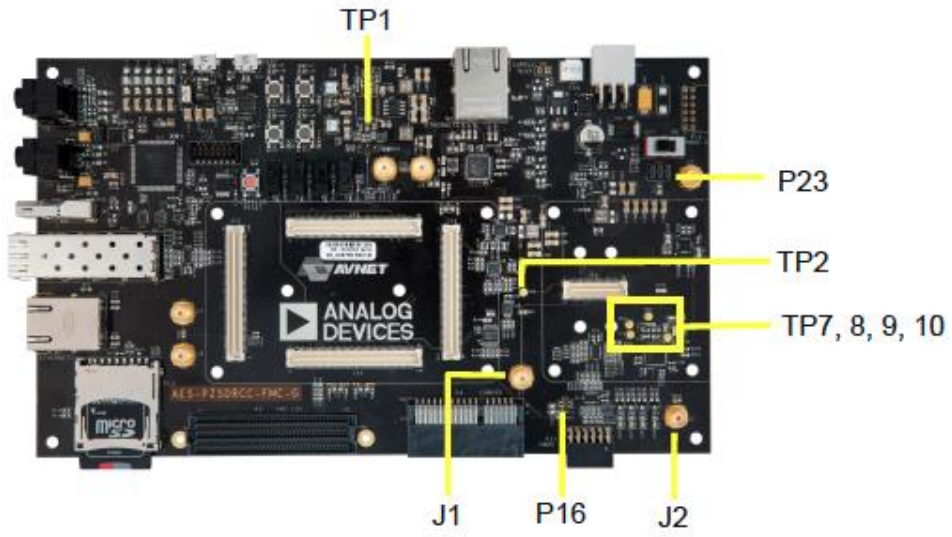


Figure 28 – Test Point Locations

Reference Designator	Name	Footprint/ Connector	Default	Notes	
JP1	Stereo Mic Bias Enable	2x1 0.1" Header	Open	If shorted, passes MICBIAS voltage to right-side microphone of 3.5mm audio jack P6-A. Mono mic is not affected by this jumper and is always connected to MICBIAS voltage.	
P17	USB OTG/ Host_Device Mode Select	3x1 0.1" Header	Pin 1-2 Shorted	Selects between USB OTG or Host/Device mode.	
				1-2	USB OTG
				2-3	USB Host/Device
P8	VADJ Select	3x1 0.1" Header	Open	Select VADJ voltage to power PicoZed SDR Banks 12 and 13.	
				Open	1.8V
				Short 1-2	2.5V
				Short 2-3	3.3V
P18	Enable extra capacitors for USB Host	2x1 0.1" Header	Open	If shorted, P19 USB_VBUS is decoupled with extra bulk caps. Must be shorted if P19 is configured for USB Host mode.	
				Open	No bulk caps
				Short	Bulk caps added

Table 30 – Jumper Settings

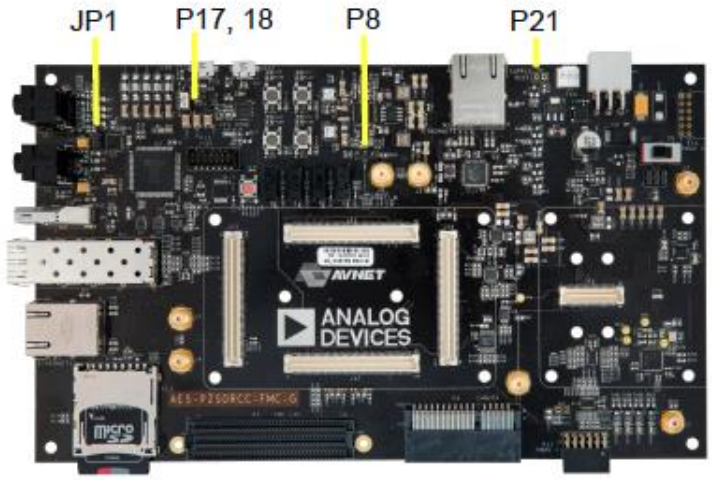


Figure 29 – Jumper Locations

5 Reference Designs

The PicoZed SDR FMC Carrier supports a sophisticated reference design developed and maintained by Analog Devices. A pre-compiled, bootable image of this design is included on an SD card. To learn how to run the reference design, download the *PicoZed SDR FMC Quick Start Card* and *PicoZed SDR FMC Carrier Getting Start Guide* at www.picozed.org/product/picozed-sdr-development-kit.

To quickly explore the reference design, here are some additional resources:

- The SD card image used to boot the reference design.
- The Analog Devices PicoZed SDR Wiki provides details about reference designs.
- The HDL, no-OS and Linux sources are hosted on GitHub.
- For HDL, we recommend cloning from the latest official tag (released twice per year) rather than the development branch. (https://github.com/analogdevicesinc/hdl/releases) For example, choose branch **hdl_2015_r2** to get the second release of 2015.

Figure 30 – ADI GitHub HDL Repository

- The TCL scripts to build the Vivado project for this carrier are in **/projects/pzsdr/ccfmc**.
- The ADI Reference Designs HDL User Guide explains how to rebuild the Zynq PL project.

NOTE: The reference design is based on the HDL code maintained by Analog Devices. To manage dependencies in the build process for Vivado projects, Analog Devices provides Linux-based *makefiles*. We recommend Windows users build Vivado projects using *make* under CYGWIN. Instructions to install a minimal version of CYGWIN that provides a Linux-like environment under Windows are available here.

6 Glossary of Terms

Term	Definition
B2B	Board-to-Board (SOM-Carrier Connector)
FMC	Zynq PL Mezzanine Card
HDMI	High-Definition Multimedia Interface
HNP	Host Negotiation Protocol
HP	High Performance I/O bank
HR	High Range I/O bank
LDO	Low Drop Out voltage regulator
LPC	Low Pin Count, refers to FMC connector
MGT	Multi Gigabit Transceiver
MIO	Multiplexed Input Output (the dedicated I/O available on the Zynq PS)
PL	Zynq Programmable Logic
PMOD	Digilent Pmod™
POR	Power On Reset
PS	Zynq Processing System
RS	Rate Select
SDR1x1	PicoZed SDR 1x1 with Zynq Z7020 and AD9364
SDR2x2	PicoZed SDR 2x2 with Zynq Z7035 and AD9361
SFP+	Enhanced Small Form-factor Pluggable
SMA	SubMiniature version A (a RF coaxial connector)
SMPS	Switch Mode Power Supply
SoC	System On Chip
SOM	System On Module (used collectively to refer to SDR2x2 and SDR1x1)
VCP	Virtual COM Port