AS5013

Data Sheet

Low Power Integrated Hall IC for Human Interface Applications

1 General Description

The AS5013 is a complete Hall Sensor IC for smart navigation key applications to meet the low power requirements and host SW integration challenges for products such as cell phones and smart handheld devices.

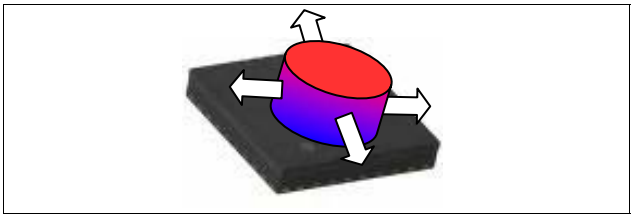
Due to the on chip processing engine, system designers are not tasked with integrating complex SW algorithms on their host processor thus leading to rapid development cycles.

The AS5013 single-chip IC includes 5 integrated Hall sensing elements for detecting up to ±2mm lateral displacement, high resolution ADC, XY coordinate and motion detection engine combined with a smart power management controller.

The X and Y positions coordinates and magnetic field information for each Hall sensor element is transmitted over a 2-wire I²C compliant interface to the host processor.

The AS5013 is available in a small 16-pin 4x4x0.55mm QFN package and specified over an operating temperature of
-20 to +80°C.

Figure 1 Typical Arrangement of AS5013 and Axial Magnet



Benefits

- Complete system-on-chip
- High reliability due to non-contact sensing
- Low power consumption

Key Features

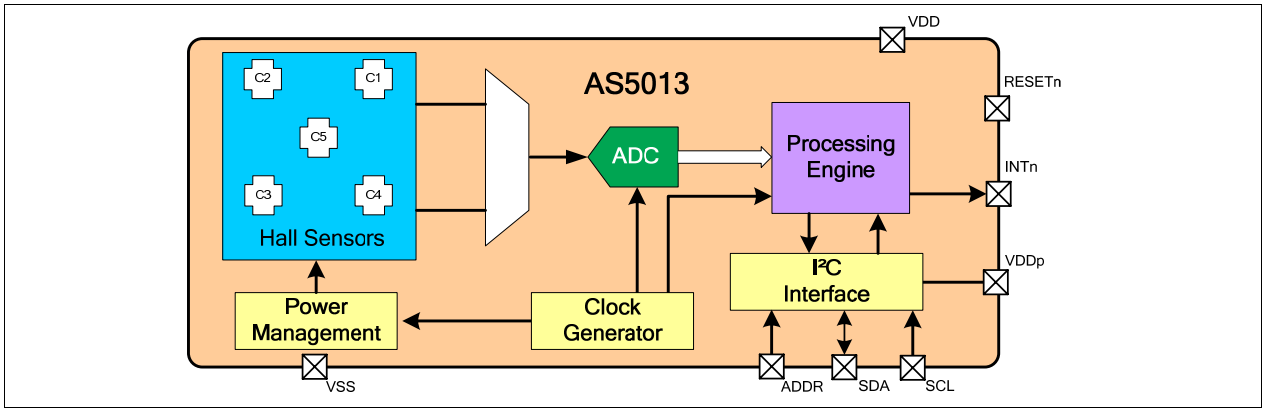
- 2.7 to 3.6V operating voltage
- Down to 1.7V peripheral supply voltage
- Two operating modes:
  - Idle mode
  - Low Power mode
- Less than 3µA current consumption in Idle mode
- Low power mode with selectable readout rate
- Two interrupt modes
  - Motion detect
  - Data ready
- Lateral magnet movement radius up to 2mm
- High-speed I²C interface

Applications

The AS5013 is ideal for small factor manual input devices in battery operated equipment, such as

- Mobile phones
- MP3 players
- PDA's
- GPS receivers
- Gaming consoles

Figure 2 AS5013 Block Diagram



2 Package and pinout

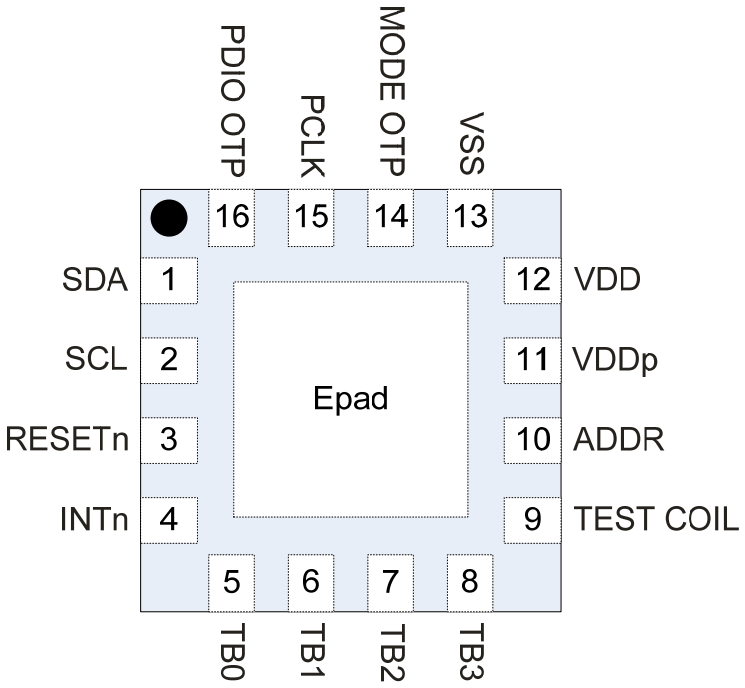


Figure 3: QFN-16 package and pinout (TOP view)

Die Pad	Pin Name	Pin Typ	ESD	Requirement/ Comment
1	SDA	DIO_OD	2kV	I²C Data line, open drain
2	SCL	DI	2kV	I²C Clock line
3	RESETn	DI	2kV	General Reset input: 0: Reset, 1: Normal mode
4	INTn	DO_OD	2kV	Interrupt line, open drain, active low
5	TB0	AIO	2kV	test pin, leave unconnected
6	TB1	AIO	2kV	test pin, leave unconnected
7	TB2	AIO	2kV	test pin, leave unconnected
8	TB3	AIO	2kV	test pin, leave unconnected
9	TEST COIL	special	2kV	test pin, leave unconnected or connect to VSS
10	ADDR	DI_ST	2kV	I²C address selection input. Read in at each reset
11	VDDp	S	2kV	1.7 ~ 3.6V IO power supply
12	VDD	S	2kV	2.7 ~ 3.6V Core power supply
13	VSS	S	2kV	Power supply ground
14	MODE OTP	DIO	2kV	test pin, leave unconnected
15	PCLK	DIO	2kV	test pin, leave unconnected
16	PDIO OTP	DIO	2kV	test pin, leave unconnected
EPAD	Exposure Pad	-	-	Internally not connected. Leave open or connect to VSS

PIN Types:
S ... supply pad
DI : digital input
DIO_OD ... digital I/O / open drain
AIO ... analog I/O
DI_ST : digital input with Schmitt trigger functionality
DO_OD ... digital output open drain

2.1 Ordering Information

Model	Delivery Form	Package
AS5013-IQFT	Tape & Reel	QFN 4x4x0.55mm

3 Operating the AS5013

3.1 Typical application

The AS5013 requires only a few external components in order to operate immediately when connected to the host microcontroller.
Only 4 wires are needed for a simple application using a single power supply: two wires for power and two wires for the I²C communication. A fifth connection can be added in order to send an interrupt to the host CPU when the magnet is moving away from the center and to inform that a new valid coordinate can be read.

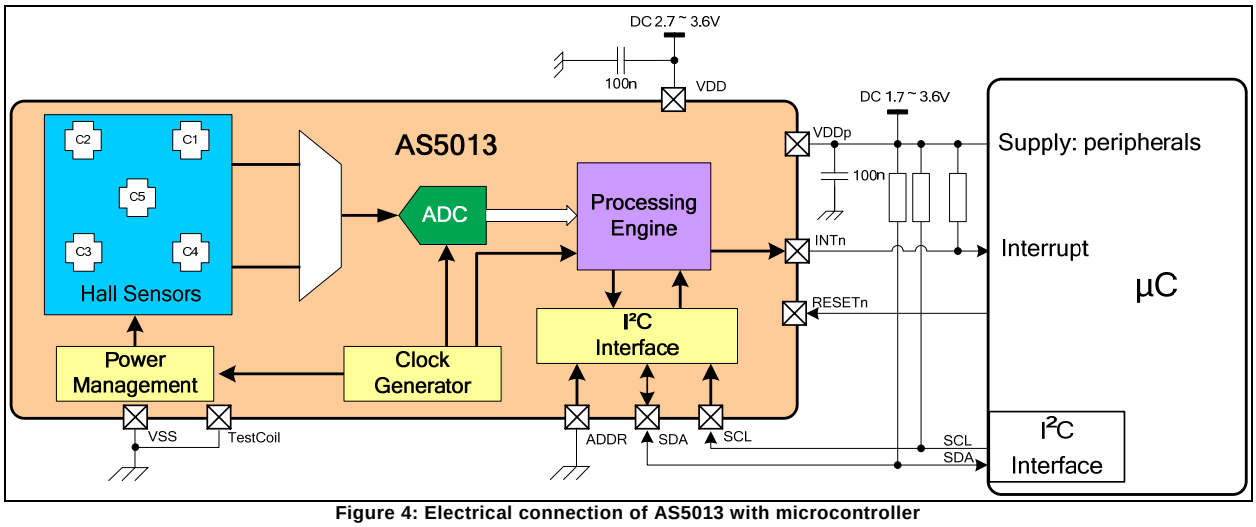


Figure 4: Electrical connection of AS5013 with microcontroller

3.2 XY coordinates interpretation

The movement of the magnet over the Hall elements causes response which is geometrically distributed like a bell-shaped curve.
The maximum magnet travel is a circle of 2mm radius around the center of the AS5013. The hall elements C1..C4 are placed on a circle centered on the middle of the package. The hall element C5, placed exactly in the middle is used for better linearity response with magnet displacement larger than +-1.0mm.

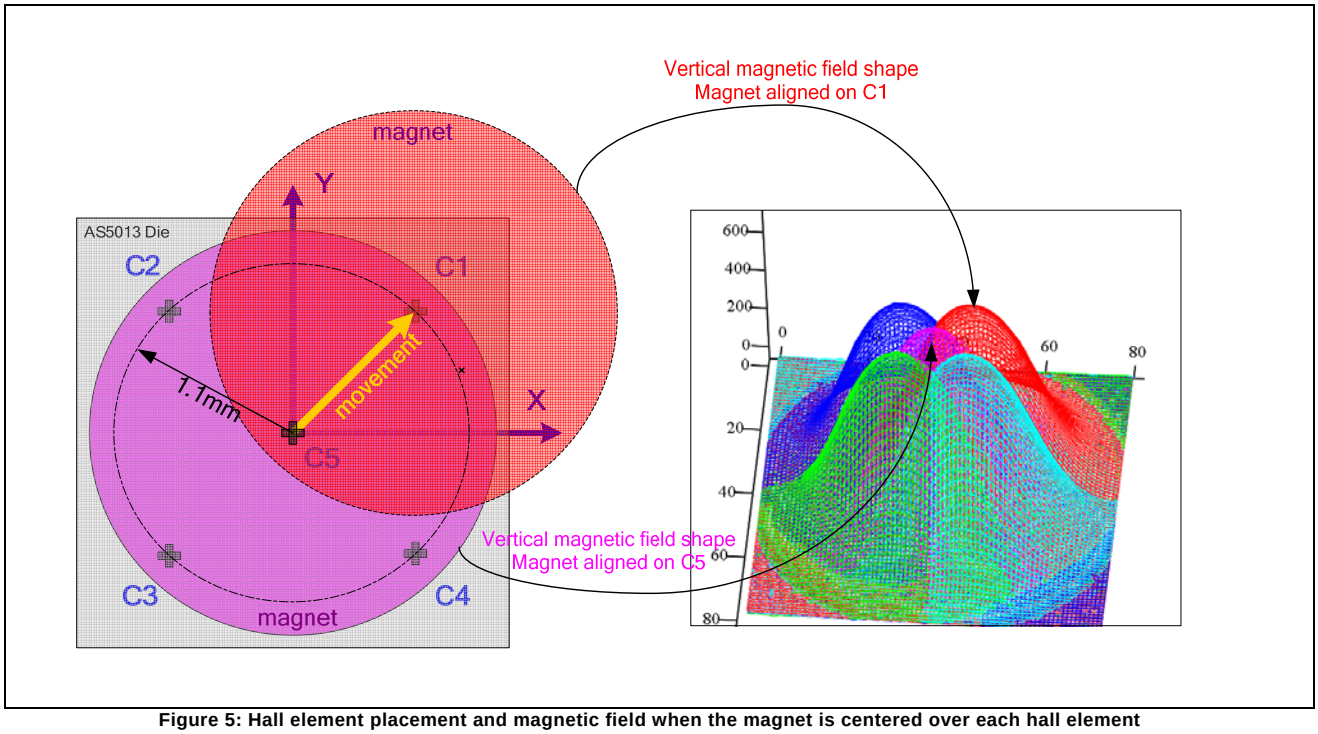


Figure 5: Hall element placement and magnetic field when the magnet is centered over each hall element

3.3 Transfer function

AS5013 has the possibility to adjust the transfer function for the used magnet and a specific range to optimize the linearity and resolution. The value will be provided from austriamicrosystems AG and has to be written in the algorithm related registers *M_ctrl [0x2B]*, *J_ctrl [0x2C*], *T_ctrl [0x2D]* during the initialization phase.
Please contact austriamicrosystems for parameter settings.

Below is the optimal setup for a range of +- 0.6 mm to obtain the best dynamic range from XY registers -128~+127 with one given magnet airgap, with d2x0.8mm axial magnet.

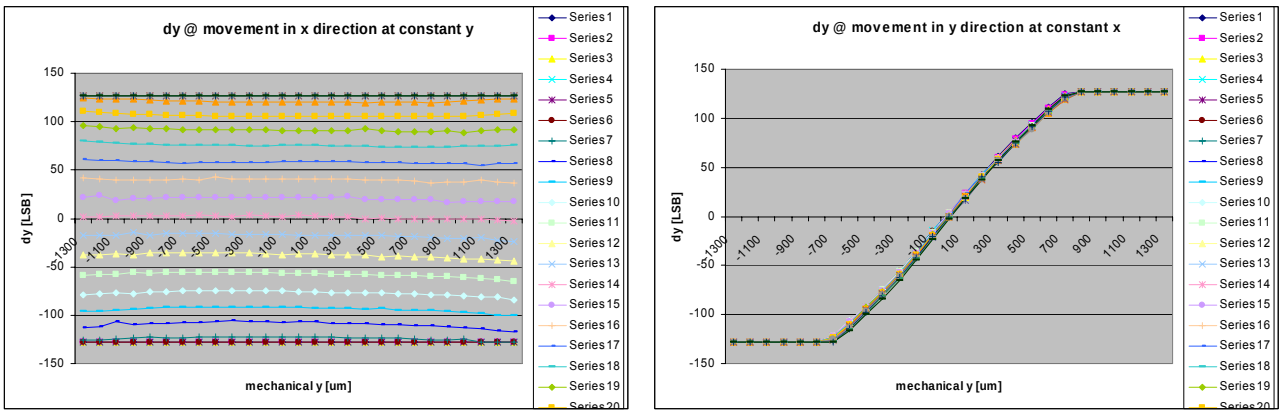


Figure 6: Example of transfer function Y_displacement vs. Y_register, optimized for 0.6mm travel radius

3.4 Power modes

The AS5013 can operate in two different power modes, depending on the power consumption requirements of the whole system.

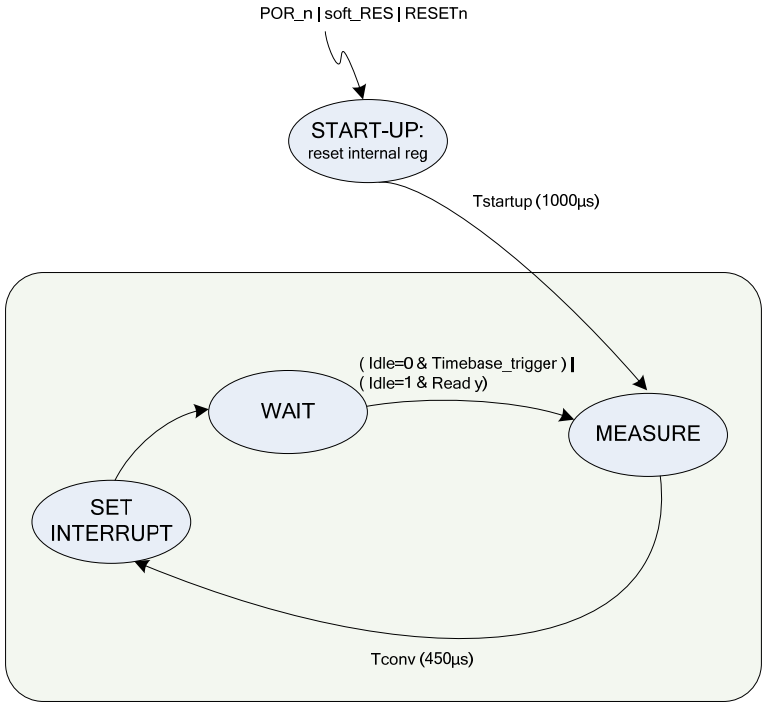


Figure 7: Readout cycle depending on power mode (idle bit)

START-UP:
After power up and after applying a soft reset (Reg 0Fh [1]) or hardware reset (RESETn input, LOW pulse >100ns), AS5013 enters the START-UP state. During this state the internal registers are loaded with their reset values. After min. Tstartup = 1000µs, the AS5013 will perform one measurement and switches automatically into the WAIT state.

MEASURE:
The hall element data are measured, x/y coordinates are calculated and available in registers 10h and 11h after Tconv = 450µs max.

SET INTERRUPT:
The INTn ouput is set, depending on the interrupt mode configured in the control register Reg 0Fh [2] and Reg 0Fh [3].

WAIT
The module is now in waiting status. A new measurement will occur depending on the power mode used (Reg 0Fh [7] Idle = 0 or 1) and the Timebase Reg 0Fh [6:4]

4 I²C Registers

4.1 Control Register 1 (0Fh)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Idle	Time base bit[2]	Time base bit[1]	Time base bit[0]	INT_disable	INT_function	Soft_rst	Data_valid
R/W	*R/W*	*R/W*	*R/W*	*R/W*	*R/W*	*R/W*	*R*

Reset value: 1111 0000

- **Bit7: Idle**

→ **Idle = 0**: Low Power Mode
The measurements are triggered with an internal low power oscillator – the user can select between 8 different timings by setting the low power timebase (Control Register 1 [6:4])
→ **Idle = 1**: Idle mode (default)
A new measurement cycle is started after the I²C ACK bit following the read out of the Y_res_int register 11h. The readout rate and thus the power consumption is externally controlled by the host MCU.

- **Bit6-4: Low Power timebase**

Configure the time base of the automatic wakeup in Low Power Mode

Low Power time base CONFIG_REG1 0Fh [6:4]	$\Delta t_{timbase}$ (ms)	Average core current IDD (µA)
000b	20	190
001b	40	97
010b	80	50
011b	100	40
100b	140	30
101b	200	22
110b	260	17
111b (default)	320	15

- **Bit3: INT_disable**

→ **INT_disable = 0**: Interrupt output INTn is enabled (default)
→ **INT_disable = 1**: Interrupt output INTn is disabled and is fixed to '1'

- **Bit2: INT_function**

→ **INT_function = 0**: Interrupt output INTn is active '0' after each measurement (default):
- Automatically triggered in Low Power mode, depending on the time base chosen
- 450µs after Y readout in Idle mode

The interrupt is cleared by the I²C ACK bit after reading the Y-register 11h. In block read mode, the several other bytes could be transferred before the interrupt is cleared.
→ **INT_function = 1**: Interrupt output INTn is active '0' when the movement of the magnet exceeds the Dead Zone area.
The Dead Zone area is set by registers Xp (Reg 12h), Xn (Reg 13h), Yp (Reg 14h), Yn (Reg 15h).
The interrupt is cleared by the I²C ACK bit after reading the Y_res_int register 11h, and will be active '0' at the next measurement if the magnet is still in the Detection Area.
In block read mode, several other bytes could be transferred before the interrupt is cleared when the Y_res_int register is read.
It is recommended to use this mode with the Low Power mode (Idle = 0), in order to wake up automatically a system when the magnet has been moved away from the center. The polling time is the Low Power time base bit [6:4].

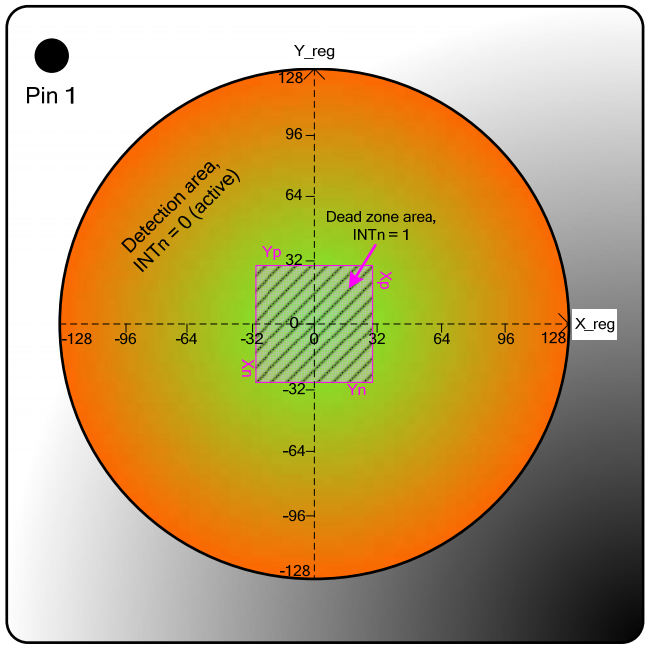


Figure 8: Dead Zone representation with INT_function = 1

- **Bit1: Soft_rst**

→ **Soft_rst = 0**: Normal mode (default).
→ **Soft_rst = 1**: Reset mode. All the internal registers are loaded with their reset value. The Control Register 1 is loaded as well with the value 1111 0000, then the Soft_rst bit goes back to 0 (Normal mode) once the internal reset sequence is finished.

- **Bit0: Data_valid**

→ **Data_valid = 0**: No valid coordinate is present in the X and Y_res_int registers. Reading those registers in this state will give the last valid coordinates.
→ **Data_valid = 1**: New coordinate values are ready in X and Y_res_int registers. Reading the register Y_res_int resets this bit.

4.2 X_Register (10h)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
X[7]	X[6]	X[5]	X[4]	X[3]	X[2]	X[1]	X[0]
R	*R*	*R*	*R*	*R*	*R*	*R*	*R*

Reset value: 0000 0000

- **Bit7-0: X coordinate**

X coordinate, 2'complement format (signed -128~+127)

4.3 Y_res_int Register (11h)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Y[7]	Y[6]	Y[5]	Y[4]	Y[3]	Y[2]	Y[1]	Y[0]
R	*R*	*R*	*R*	*R*	*R*	*R*	*R*

Reset value: 0000 0000

- **Bit7-0: Y_res_int coordinate**

Y coordinate, 2'complement format (signed -128~+127).
Reading this register will reset the INTn output to '1' if enabled, and reset the Data_valid bit of the Control Register 1 (0Fh), after the ACK bit of Y_res_int register readback.

4.4 Xp Register (12h)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Xp [7]	Xp [6]	Xp [5]	Xp [4]	Xp [3]	Xp [2]	Xp [1]	Xp [0]
R/W	*R/W*	*R/W*	*R/W*	*R/W*	*R/W*	*R/W*	*R/W*

Reset value: 0000 0101 (5d)

- **Bit7-0: Xp range register**

Xp range value, 2'complement (signed: -128~+127).
Determines the RIGHT threshold for the activation of INTn output (if output enabled), when bit INT_function = 1 (see Control Register 1(0Fh)).

4.5 Xn Register (13h)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Xn [7]	Xn [6]	Xn [5]	Xn [4]	Xn [3]	Xn [2]	Xn [1]	Xn [0]
R/W	*R/W*	*R/W*	*R/W*	*R/W*	*R/W*	*R/W*	*R/W*

Reset value: 1111 1011 (-5d)

- **Bit7-0: Xn range register**

Xn range value, 2'complement (signed: -128~+127).
Determines the LEFT threshold for the activation of INTn output (if output enabled), when bit INT_function = 1 (see Control Register 1 (0Fh)).

4.6 Yp Register (14h)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Yp [7]	Yp [6]	Yp [5]	Yp [4]	Yp [3]	Yp [2]	Yp [1]	Yp [0]
R/W	*R/W*	*R/W*	*R/W*	*R/W*	*R/W*	*R/W*	*R/W*

Reset value: 0000 0101 (5d)

- **Bit7-0: Yp range register**

Yp range value, 2'complement (signed: -128~+127).
Determines the TOP threshold for the activation of INTn output (if output enabled), when bit INT_function = 1 (see Control Register (0Fh)).

4.7 Yn Register (15h)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Yn [7]	Yn [6]	Yn [5]	Yn [4]	Yn [3]	Yn [2]	Yn [1]	Yn [0]
R/W	*R/W*	*R/W*	*R/W*	*R/W*	*R/W*	*R/W*	*R/W*

Reset value: 1111 1011 (-5d)

- **Bit7-0: Yn range register**

Yn range value, 2'complement (signed: -128~+127).
Determines the BOTTOM threshold for the activation of INTn output (if output enabled), when bit INT_function = 1 (see Control Register (0Fh)).

4.8 M_ctrl Register (2Bh)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
M_ctrl [7]	M_ctrl [6]	M_ctrl [5]	M_ctrl [4]	M_ctrl [3]	M_ctrl [2]	M_ctrl [1]	M_ctrl [0]
R/W	*R/W*	*R/W*	*R/W*	*R/W*	*R/W*	*R/W*	*R/W*

Reset value: 0000 0000 (00h)

- **Bit7-0: M_ctrl register**

Middle hall element C5 control register.
For more information how to configure this parameter, please contact austriamicrosystems.

4.9 J_ctrl Register (2Ch)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
J_ctrl [7]	J_ctrl [6]	J_ctrl [5]	J_ctrl [4]	J_ctrl [3]	J_ctrl [2]	J_ctrl [1]	J_ctrl [0]
R/W	*R/W*	*R/W*	*R/W*	*R/W*	*R/W*	*R/W*	*R/W*

Reset value: 0000 0110 (6d)

- **Bit7-0: J_ctrl register**

Sector dependent attenuation of the outer Hall elements C1..C4.
For more information how to configure this parameter, please contact austriamicrosystems.

4.10 T_ctrl Register (2Dh)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
T_ctrl [7]	T_ctrl [6]	T_ctrl [5]	T_ctrl [4]	T_ctrl [3]	T_ctrl [2]	T_ctrl [1]	T_ctrl [0]
R/W	*R/W*	*R/W*	*R/W*	*R/W*	*R/W*	*R/W*	*R/W*

Reset value: 0000 1001 (9d)

- **Bit7-0: T_ctrl register**

Scaling control register.
This register controls the scaling factor of the XY coordinates to fit to the 8-bit X and Y_res_int register (full dynamic range).
For more information how to configure this parameter, please contact austriamicrosystems.

4.11 Control Register 2 (2Eh)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Test	Test	Test	ext_clk_en	use_static_offset	EN_offset_comp	inv_spinning	pptrim_en
R/W	*R/W*	*R/W*	*R/W*	*R/W*	*R/W*	*R/W*	*R/W*

Reset value: 1000 0100

- **Bit7: Test**

Test bit. Must be configured to ‘1’.

- **Bit[6:4]: Test**

Test bit. Must be configured to ‘000’.

- **Bit3: use_static_offset**

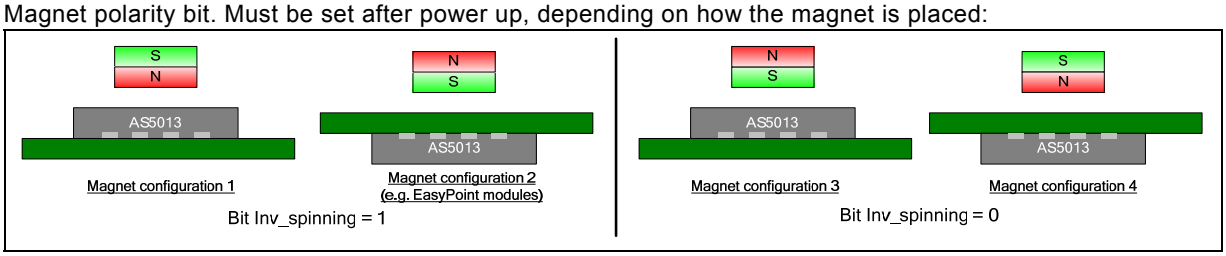
Test bit. Must be configured to ‘0’.

- **Bit2: EN_offset_comp**

Test bit. Must be configured to ‘1’.

- **Bit1: inv_spinning**

Magnet polarity bit. Must be set after power up, depending on how the magnet is placed:



Note: In case the registers X and Y_res_int values take only the two values -128 and +127 for any position of the magnet, one cause is the magnet polarity which must be inverted by changing this bit.

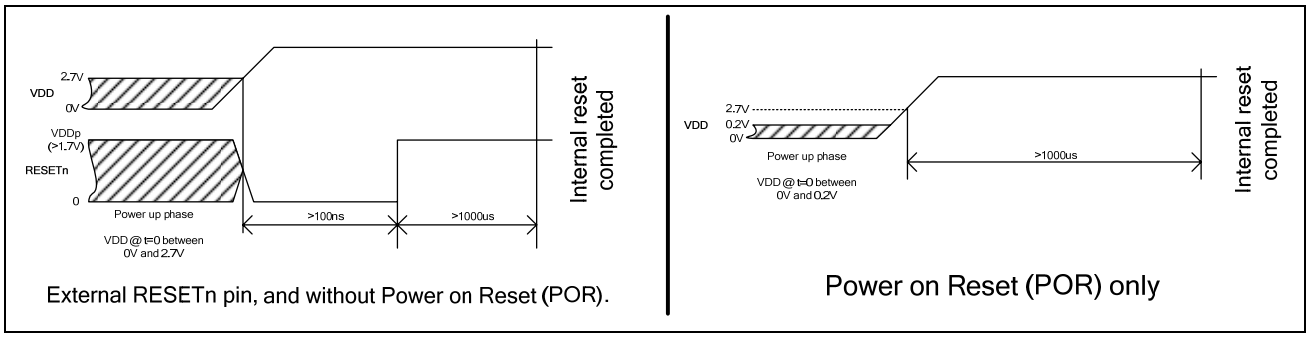
- **Bit0: pptrim_en**

Test bit. Must be configured to '0'.

4.12 Power ON

The AS5013 has a Power ON Reset (POR) cell to monitor the VDD voltage at startup and reset all the internal registers.

After the internal reset is completed, the POR cell is disabled in order to save current during normal operation.
If VDD drops below 2.7V down to 0.2V, the POR cell will not be enabled back, and the registers will not be correctly reseted or can get random values.
It is **highly recommended to control the external RESETn** signal by applying a LOW pulse of >100ns once VDD reached 2.7V and VDDp reached 1.7V.



4.13 Registers Initialization

After Power Up, the following sequence must be performed:

1. VDD and VDDp Power up, and reached their nominal values (VDD>2.7V, VDDp>1.7V).
2. RESETn LOW during >100ns
3. Delay 1000µs
4. Loop check register [0Fh] until the value F0h or F1h is present (reset finished, registers to their default values)
5. Optional: Write value 86h into register [2Eh] → Invert magnet polarity (if needed, e.g. for EasyPoint modules)
6. Configure register [2Bh] → Configure M_ctrl middle hall element control
7. Configure register [2Ch] → Configure J_ctrl attenuation factor
8. Configure register [2Dh] → Configure T_ctrl scaling factor
9. Configure the wanted Power Mode into register [0Fh] (Idle mode or Low Power Mode with Timebase configuration)
10. X Y coordinates are ready to be read.

Note: In case the registers X and Y_res_int values take only the two values -128 and +127 for any position of the magnet, one cause is the magnet polarity which must be inverted by changing the bit *inv_spinning* of Control_register_2 (2Eh).

4.14 I²C Registers

The following registers / functions are accessible over the serial I²C interface.

Register	#bits	Access	Address	Format	Reset Value	Bit	Description
IC Identification							
ID Code	8	R	0C		0Ch	<7:0>	8 bit Manufacture ID Code
ID Version	8	R	0D		0Dh	<7:0>	8 bit Component ID Version
Silicon Revision	8	R	0E		00h	<7:0>	8 bit Silicon Revision
Control_register_1							
Idle	1	R/W	0Fh		1b	<7>	1 : Idle mode 0 : Low Power mode
Low_power_timebase	3	R/W	0Fh		111b	<6:4>	Low Power readout time base register
INT_disable	1	R/W	0Fh		0b	<3>	Disables the interrupt functionality. 1 : Interrupt disabled 0 : Interrupt enabled
INT_function	1	R/W	0Fh		0b	<2>	Interrupt control register 0 : interrupt goes low with every new calculated x/y coordinates 1 : interrupt pin goes low in when new x/y coordinates are calculated and the magnet has exited the xp, xn, yp yn threshold values
soft_rst	1	R/W	0Fh		0b	<1>	Soft Reset 0: Normal mode 1: all registers return to their respective reset value
data_valid	1	R	0Fh		0b	<0>	Data valid indicator 0: X/Y calculation ongoing 1: X/Y calculation finished , coordinates ready
X/Y coordinate registers							
x	8	R	10h	two's comp.	00h	<7:0>	Result
y_res_int	8	R	11h	two's comp.	00h	<7:0>	Result, resets the interrupt flag at the value ACK
Range settings							
xp	8	R/W	12h	two's comp.	5h (5 dec)	<7:0>	wake up threshold @ positive X -direction
xn	8	R/W	13h	two's comp.	FBh (-5 dec)	<7:0>	wake up threshold @ negative X -direction
yp	8	R/W	14h	two's comp.	5h (5 dec)	<7:0>	wake up threshold @ positive Y -direction
yn	8	R/W	15h	two's comp.	FBh (-5 dec)	<7:0>	wake up threshold @ negative Y –direction

Register	#bits	Access	Address	Format	Reset Value	Bit	Description
Channel voltages (3)							
c4_neg <11:8>	4	R	16h	two's comp	00h	<3:0> <7:4>	voltage @ channel 4, neg. current spinning sign extended to 8 bit
c4_neg <7:0>	8	R	17h	two's comp	00h	<7:0>	voltage @ channel 4, neg. current spinning
c4_pos <11:8>	4	R	18h	two's comp	00h	<3:0> <7:4>	voltage @ channel 4, pos. current spinning sign extended to 8 bit
c4_pos <7:0>	8	R	19h	two's comp	00h	<7:0>	voltage @ channel 4, pos. current spinning
c3_neg <11:8>	4	R	1Ah	two's comp	00h	<3:0> <7:4>	voltage @ channel 3, neg. current spinning sign extended to 8 bit
c3_neg <7:0>	8	R	1Bh	two's comp	00h	<7:0>	voltage @ channel 3, neg. current spinning
c3_pos <11:8>	4	R	1Ch	two's comp	00h	<3:0> <7:4>	voltage @ channel 3, pos. current spinning sign extended to 8 bit
c3_pos <7:0>	8	R	1Dh	two's comp	00h	<7:0>	voltage @ channel 3, pos. current spinning
c2_neg <11:8>	4	R	1Eh	two's comp	00h	<3:0> <7:4>	voltage @ channel 2, neg. current spinning sign extended to 8 bit
c2_neg <7:0>	8	R	1Fh	two's comp	00h	<7:0>	voltage @ channel 2, neg. current spinning
c2_pos <11:8>	4	R	20h	two's comp	00h	<3:0> <7:4>	voltage @ channel 2, pos. current spinning sign extended to 8 bit
c2_pos <7:0>	8	R	21h	two's comp	00h	<7:0>	voltage @ channel 2, pos. current spinning
c1_neg <11:8>	4	R	22h	two's comp	00h	<3:0> <7:4>	voltage @ channel 1, neg. current spinning sign extended to 8 bit
c1_neg <7:0>	8	R	23h	two's comp	00h	<7:0>	voltage @ channel 1, neg. current spinning
c1_pos <11:8>	4	R	24h	two's comp	00h	<3:0> <7:4>	voltage @ channel 1, pos. current spinning sign extended to 8 bit
c1_pos <7:0>	8	R	25h	two's comp	00h	<7:0>	voltage @ channel 1, pos. current spinning
c5_neg <11:8>	4	R	26h	two's comp	00h	<3:0> <7:4>	voltage @ channel 5, neg. current spinning sign extended to 8 bit
c5_neg <7:0>	8	R	27h	two's comp	00h	<7:0>	voltage @ channel 5, neg. current spinning
c5_pos <11:8>	4	R	28h	two's comp	00h	<3:0> <7:4>	voltage @ channel 5, pos. current spinning sign extended to 8 bit
c5_pos <7:0>	8	R	29h	two's comp	00h	<7:0>	voltage @ channel 5, pos. current spinning
hall bias currents							
AGC	8	R/W	2Ah		00b 20h	<7:6> <5:0>	not implemented (read 00b) 6 bit AGC value (if an AGC algorithm implemented in the µC)

Register	#bits	Access	Address	Format	Reset Value	Bit	Description
Control register for the algorithm							
M_ctrl	8	R/W	2Bh		00h	<7:0>	Control register for the middle Hall element C5. If the register is zero the middle Hall element is used for the XY calculation
J_ctrl	8	R/W	2Ch		06h	<7:0>	Control register for the sector dependent attenuation of the outer Hall elements
T_ctrl	8	R/W	2Dh		09h	<7:0>	Scale input to fit to the 8 Bit result register
Control_register_2							
Test	1	R/W	2Eh		1b	<7>	Test only, must be 1’
Test	1	R/W	2Eh		0b	<6>	Test only, must be ‘0’
Test	1	R/W	2Eh		0b	<5>	Test only, must be ‘0’
ext_clk_en	1	R/W	2Eh		0b	<4>	Test only, must be ‘0’
use_static_offset	1	R/W	2Eh		0b	<3>	Test only, must be ‘0’
EN_offset_comp	1	R/W	2Eh		1b	<2>	Test only, must be ‘1’
inv_spinning	1	R/W	2Eh		0b	<1>	Invert the channel voltage. Set to invert the magnet polarity
pptrim_en	1	R/W	2Eh		0b	<0>	Factory only, must be ‘0’

5 I²C interface

The AS5013 supports the 2-wire high-speed I²C protocol in device mode, according to the NXP specification UM10204.
The host MCU (master) has to initiate the data transfers. The 7-bit device address of the AS5013 depends on the state at the pin ADDR.

- ADDR = 0 → Slave address =‘1000 000’ (40h)
- ADDR = 1 → Slave address =‘1000 001’ (41h)

For other I²C addresses, please contact austriamicrosystems.

Supported modes:
Random/Sequential Read
Byte/Page Write

Standard (slave mode)
Fast Mode (slave mode)
High Speed (slave mode)

The SDA signal is bidirectional and is used to read and write the serial data. The SCL signal is the clock generated by the host MCU, to synchronize the SDA data in read and write mode. The maximum I²C clock frequency is 3.4MHz, data are triggered on the rising edge of SCL.

5.1 Interface operation

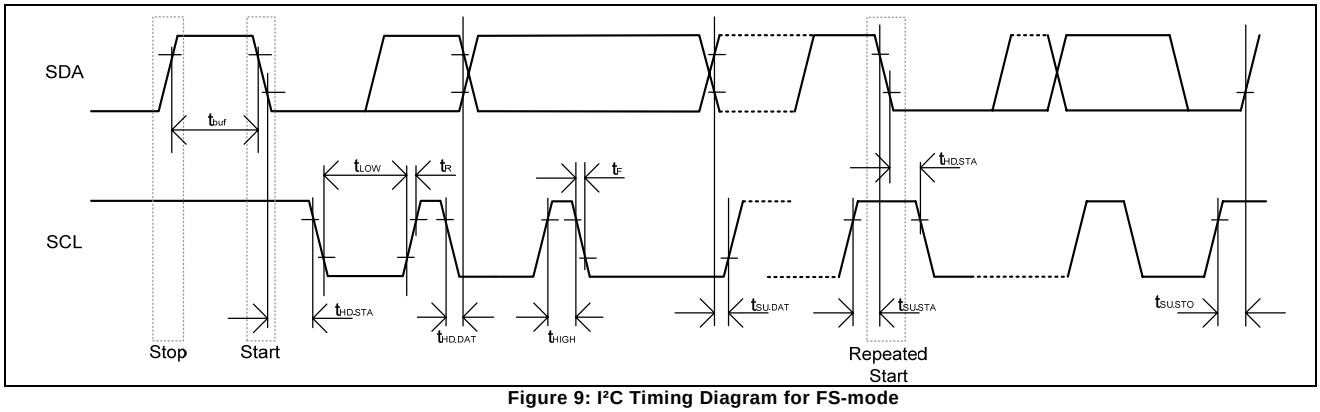


Figure 9: I²C Timing Diagram for FS-mode

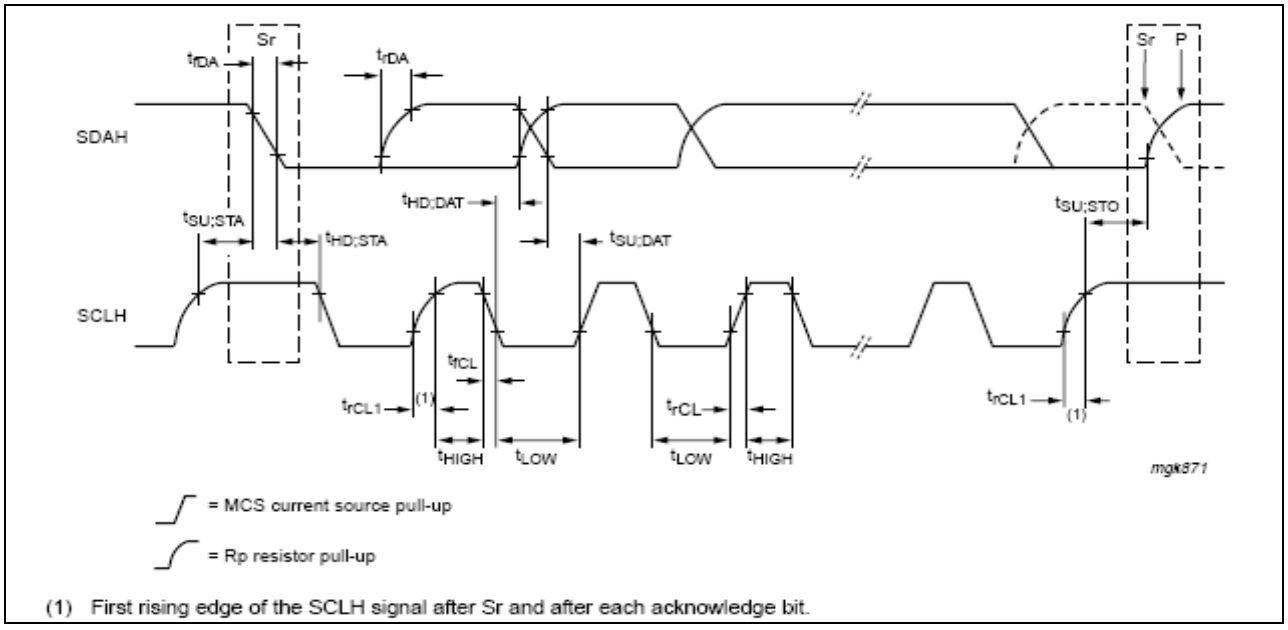


Figure 10: Timing Diagram for HS-mode

5.2 I²C Electrical Specification

			FS-mode+		HS-mode C_B=100pF		HS-mode C_B=400pF		
Symbol	**Parameter**	**Condition**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
V_{IL}	LOW-Level Input Voltage		-0.5	$0.3V_{DDp}$	-0.5	0.3VDDp	-0.5	$0.3V_{DDp}$	V
V_{IH}	HIGH-Level Input Voltage		$0.7V_{DDp}$	V_{DDp} + 0.5 (1)	$0.7V_{DDp}$	VDDp + 0.5 (1)	0.7VDDp	V_{DDp} + 0.5 (1)	V
V_{hys}	Hysteresis of Schmitt Trigger Inputs	V_{DDp} < 2V	$0.1V_{DDp}$	--	$0.1V_{DDp}$	--	0.1VDDp	--	V
V_{OL}	LOW-Level Output Voltage (open-drain or open-collector) at 3mA Sink Current	V_{DDp} < 2V	--	$0.2V_{DDp}$	--	0.2VDDp	--	$0.2V_{DDp}$	V
I_{OL}	LOW-Level Output Current	V_{OL} = 0.4V	20		--	--	--	--	mA
I_{CS}	Pull-up current of SCLH current source	SCLH output levels between 0.3 V_{DDp} and 0.7 V_{DDp}	--	--	3	12	3	12	mA
t_{SP}	Pulse Width of Spikes that must be suppressed by the Input Filter		--	50 (2)	--	10	--	10	ns
I_i	Input Current at each I/O Pin	Input Voltage between $0.1V_{DDp}$ and $0.9V_{DDp}$	-10	+10 (3)	--	10	--	10	µA
C_B	Total Capacitive Load for each Bus Line		--	550	--	100	--	400	pF
$C_{I/O}$	I/O Capacitance (SDA, SCL) (5)		--	10	--	10	--	10	pF

(1) Maximum V_{IH} = V_{DDpmax} +0.5V or 5.5V, which ever is lower.
(2) Input filters on the SDA and SCL inputs suppress noise spikes of less than 50 ns.
(3) I/O pins of Fast-mode and Fast-mode Plus devices must not obstruct the SDA and SCL lines if VDDp is switched off.

5.3 I²C Timing

			FS-mode+		HS-mode C_B=100pF		HS-mode C_B=400pF (5)		
Symbol	**Parameter**	**Condition**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
f_{SCLK}	SCL clock Frequency		--	1000	--	3400	--	1700	kHz
t_{BUF}	Bus Free Time; time between STOP and START Condition		500	--	500	--	500	--	ns
$t_{HD;STA}$	Hold Time; (Repeated) START Condition (1)		260	--	160	--	160	--	ns
t_{LOW}	LOW Period of SCL Clock		500	--	160	--	320	--	ns
t_{HIGH}	HIGH Period of SCL Clock		260	--	60	--	120	--	ns
$t_{SU;STA}$	Setup Time for a Repeated START condition		260	--	160	--	160	--	ns
$t_{HD;DAT}$	Data Hold Time (2)		0	450	0	70	0	150	ns
$t_{SU;DAT}$	Data Setup Time (3)		50	--	10	--	10	--	ns
t_R	Rise Time of SDA and SCL Signals		20+0.1C$_b$	120	--	--	--	--	ns
t_F	Fall time of SDA and SCL signals		20+0.1C$_b$	120 (4)	--	--	--	--	ns

			FS-mode+		HS-mode C_B=100pF		HS-mode C_B=400pF (5)		
Symbol	**Parameter**	**Condition**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
t_{rCL}	Rise time of SCLH signal	Ext. pull-up source of 3mA	--	--	10	40	20	80	ns
t_{rCL1}	Rise time of SCLH signal after repeated START condition and after an acknowledge bit	Ext. pull-up source of 3mA	--	--	10	80	20	160	ns
tf_{CL}	Output rise time of SCLH signal	Ext. pull-up source of 3mA	--	--	10	40	20	80	ns
t_{rDA}	Output rise time of SDAH signal		--	--	10	80	20	160	ns
t_{fDA}	Output rise time of SDAH signal		--	--	10	80	20	160	ns
$t_{SU;STO}$	Setup Time for STOP Condition		260	--	160	--	160	--	Ns
V_{nL}	Noise margin at LOW level	For each connected device (including hysteresis)	$0.1V_{DDp}$	--	$0.1V_{DDp}$	--	$0.1V_{DDp}$	--	V
V_{nH}	Noise margin at HIGH level		$0.2V_{DDp}$	--	$0.2V_{DDp}$	--	$0.2V_{DDp}$	--	V

(1) after this time the first clock is generated
(2) A device must internally provide a minimum hold time (120ns / max 250ns for Fast-mode Plus, 80ns / max 150ns for High-speed mode) for the SDA signal (referred to the V_{IHmin} of the SCL) to bridge the undefined region of the falling edge of SCL.
(3) A fast-mode device can be used in standard-mode system, but the requeirement $t_{SU;DAT}$ = 250ns must then e met. This is automatically the case if the device does not stretch the LOW period of the SCL signal. If such a device does strech the LOW period of the SCL signal, it must output the next data bit to the SDA line $t_{Rmax} + T_{SU;DAT}$ = 1000 + 250 = 1250ns before the SCL line is released.
(4) In Fast-mode Plus, fall time is specified the same for both output stage and bus timing. If series resistors are used this has to be considered for bus timing
(5) For capacitive bus loads between 100pF and 400pF, the timing parameters must be linearly interpolated

5.4 I²C modes

The AS5013 supports the I2C bus protocol. A device that sends data onto the bus is defined as a transmitter and a device receiving data as a receiver. The device that controls the message is called a master. The devices that are controlled by the master are referred to as slaves. A master device that generates the serial clock (SCL), controls the bus access, and generates the START and STOP conditions must control the bus. The AS5013 operates as a slave on the I²C bus. Connections to the bus are made through the open-drain I/O lines SDA and the input SCL. Clock stretching is not included.

Automatical increment of address pointer:
The AS5013 slave automatically increments the address pointer after each byte transferred. The increase of the address pointer is independent from the address being valid or not.

Invalid Addresses:
If the user sets the address pointer to an invalid address, the address byte is not acknowledged. Nevertheless a read or write cycle is possible. The address pointer is increased after each byte.

Reading:
When reading from a wrong address, the AS5013 slave data returns all zero. The address pointer is increased after each byte. Sequential read over the whole address range is possible including address overflow.

Writing:
A write to a wrong address is not acknowledged by the AS5013 slave, although the address pointer is increased. When the address pointer points to a valid address again, a successful write accessed is acknowledged. Page write over the whole address range is possible including address overflow.

The following bus protocol has been defined:

- Data transfer may be initiated only when the bus is not busy.
- During data transfer, the data line must remain stable whenever the clock line is HIGH. Changes in the data line while the clock line is HIGH are interpreted as start or stop signals.

Accordingly, the following bus conditions have been defined:

Bus Not Busy
Both data and clock lines remain HIGH.

Start Data Transfer
A change in the state of the data line, from HIGH to LOW, while the clock is HIGH, defines a START condition.

Stop Data Transfer
A change in the state of the data line, from LOW to HIGH, while the clock line is HIGH, defines the STOP condition.

Data Valid
The state of the data line represents valid data when, after a START condition, the data line is stable for the duration of the HIGH period of the clock signal. The data on the line must be changed during the LOW period of the clock signal. There is one clock pulse per bit of data.
Each data transfer is initiated with a START condition and terminated with a STOP condition. The number of data bytes transferred between START and STOP conditions are not limited, and are determined by the master device. The information is transferred byte-wise and each receiver acknowledges with a ninth bit.

Acknowledge
Each receiving device, when addressed, is obliged to generate an acknowledge after the reception of each byte. The master device must generate an extra clock pulse that is associated with this acknowledge bit.
A device that acknowledges must pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is stable LOW during the HIGH period of the acknowledge-related clock pulse. Of course, setup and hold times must be taken into account. A master must signal an end of READ access to the slave by not generating an acknowledge bit on the last byte that has been clocked out of the slave. In this case, the slave must leave the data line HIGH to enable the master to generate the STOP condition.

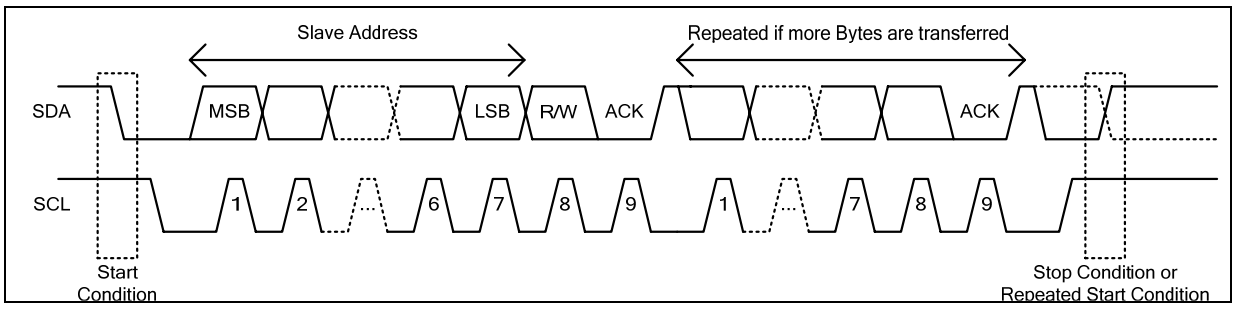


Figure 11: Data Read (Write Pointer, Then Read) - Slave Receive and Transmit

Depending upon the state of the R/W bit, two types of data transfer are possible:

- **Data transfer from a master transmitter to a slave receiver.**
  The first byte transmitted by the master is the slave address, followed by R/W = 0. Next follows a number of data bytes. The slave returns an acknowledge bit after each received byte. If the slave does not understand the command or data it sends a “not acknowledge”. Data is transferred with the most significant bit (MSB) first.
- **Data transfer from a slave transmitter to a master receiver.**
  The master transmits the first byte (the slave address). The slave then returns an acknowledge bit, followed by the slave transmitting a number of data bytes. The master returns an acknowledge bit after all received bytes other than the last byte. At the end of the last received byte, a “not acknowledge” is returned. The master device generates all of the serial clock pulses and the START and STOP conditions. A transfer is ended with a STOP condition or with a repeated START condition. Since a repeated START condition is also the beginning of the next serial transfer, the bus is not released. Data is transferred with the most significant bit (MSB) first.

The AS5013 can operate in the following two modes:

- **Slave Receiver Mode (Write Mode):**
  Serial data and clock are received through SDA and SCL. Each byte is followed by an acknowledge bit (or by a not acknowledge depending on the address-pointer pointing to a valid position). START and STOP conditions are recognized as the beginning and end of a serial transfer. Address recognition is performed by hardware after reception of the slave address and direction bit (see Figure). The slave address byte is the first byte received after the START condition. The slave address byte contains the 7-bit AS5013 address, which is stored in the OTP memory.
  The 7-bit slave address is followed by the direction bit (R/W), which, for a write, is 0. After receiving and decoding the slave address byte the device outputs an acknowledge on the SDA. After the AS5013 acknowledges the slave address + write bit, the master transmits a register address to the AS5013. This sets the address pointer on the AS5013. If the address is a valid readable address the AS5013 answers by sending an acknowledge. If the address-pointer points to an invalid position a “not acknowledge” is sent. The master may then transmit zero or more bytes of data. In case of the address pointer pointing to an invalid address the received data are not stored. The address pointer will increment after each byte transferred independent from the address being valid. If the address-pointer reaches a valid position again, the AS5013 answers with an acknowledge and stores the data. The master generates a STOP condition to terminate the data write.

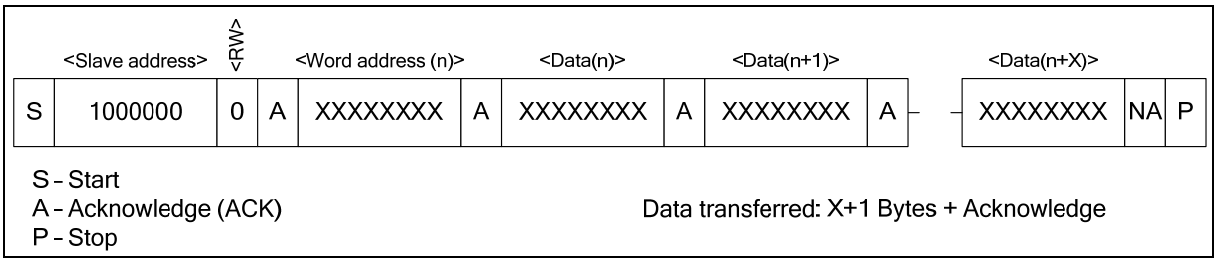


Figure 12: Data Write - Slave Receiver Mode

- **Slave Transmitter Mode (Read Mode):**
  The first byte is received and handled as in the slave receiver mode. However, in this mode, the direction bit indicates that the transfer direction is reversed. Serial data is transmitted on SDA by the AS5013 while the serial clock is input on SCL. START and STOP conditions are recognized as the beginning and end of a serial transfer. The slave address byte is the first byte received after the master generates a START

condition. The slave address byte contains the 7-bit AS5013 address. The default address is 80h. The 7-bit slave address is followed by the direction bit (R/W), which, for a read, is 1. After receiving and decoding the slave address byte the device outputs an acknowledge on the SDA line. The AS5013 then begins to transmit data starting with the register address pointed to by the register pointer. If the register pointer is not written to before the initiation of a read mode the first address that is read is the last one stored in the register pointer. The AS5013 must receive a “not acknowledge” to end a read.

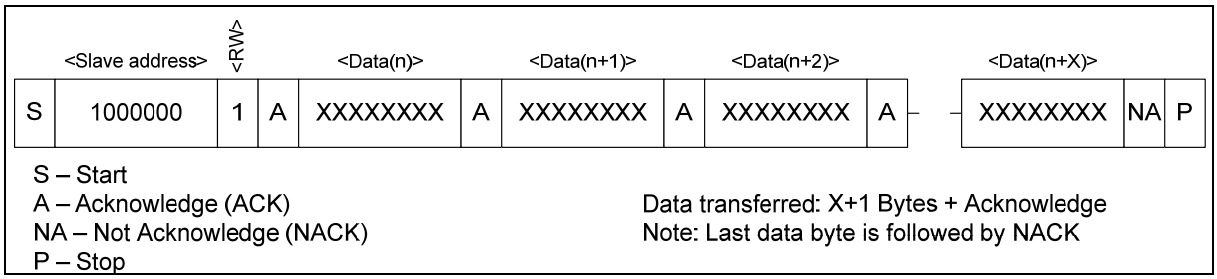


Figure 13: Data Read (from Current Pointer Location) - Slave Transmitter Mode

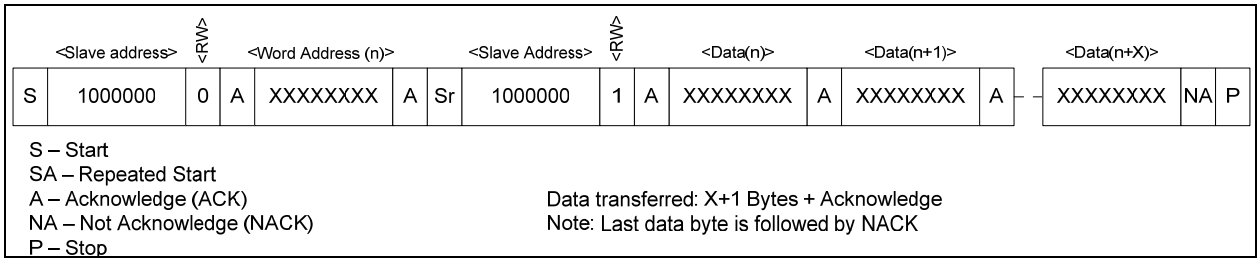


Figure 14: Data Read (from New Pointer Location) - Slave Transmitter Mode

High Speed Mode:
The AS5013 is capable to work in HS-mode.

For switching to HS-mode the Master has to send the sequence: START, MASTER CODE, NACK. This sequence is sent in FS-mode. As no device is allowed to acknowledge the master code, the master code is followed by a not-acknowledge. After a device receives the master code it has to switch from FS-settings to HS-settings within tSU.STA which is 160ns for HS-mode. The device stays in HS-mode as long as it does not receive a STOP command. After receiving a STOP command it has to switch back form HS-settings to FS-settings, which has to be competed within the minimum bus free time tBUF which is 500ns.

When switching to HS-mode the slave has to

- Adapt the SDAH and SCLH input filters according to the spike suppression requirement required in HS-mode. In HS-mode spikes up to 10ns, in FS-mode spikes up to 50ns have to be suppressed.
- Adapt the setup and hold times according to the HS-mode requirement. In HS-mode an internal hold time for SDA for START/STOP detection of 80ns (max. 150ns), in FS-mode an internal hold time of 160ns (max. 250ns) has to be provided.
- Adapt the slope control for SDAH output stage

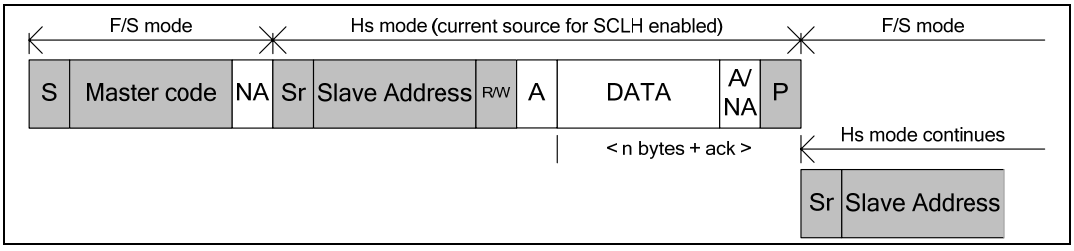


Figure 15: Data transfer format in HS-mode

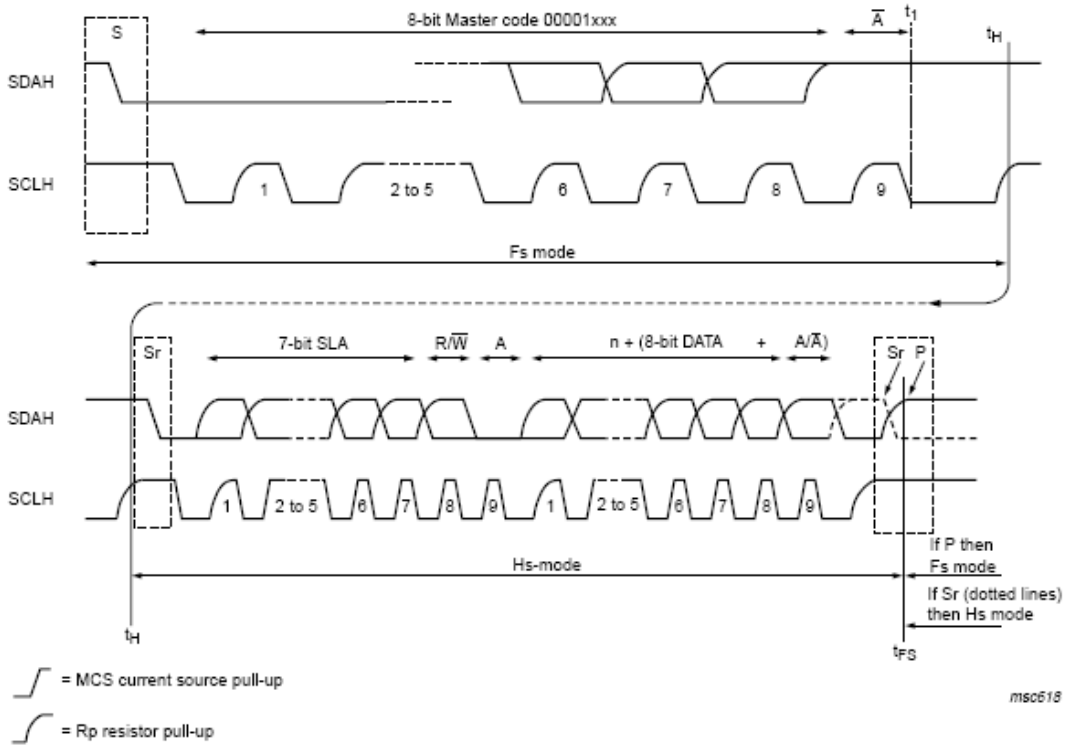


Figure 16: A complete HS-mode transfer

Automatical increment of address pointer:
The AS5013 slave automatically increments the address pointer after each byte transferred. The increase of the address pointer is independent from the address being valid or not.

Invalid Addresses:
If the user sets the address pointer to an invalid address, the address byte is not acknowledged. Nevertheless a read or write cycle is possible. The address pointer is increased after each byte.

Reading:
When reading from a wrong address, the AS5013 slave returns all zero. The address pointer is increased after each byte. Sequential read over the whole address range is possible including address overflow.

Writing:
A write to a wrong address is not acknowledged by the AS5013 slave, although the address pointer is increased. When the address pointer points to a valid address again, a successful write accessed is acknowledged. Page write over the whole address range is possible including address overflow.

5.5 SDA, SCL Input Filters

Input filters for SDA and SCL inputs are included to suppress noise spikes of less than 50ns. Furthermore the SDA line is delayed by 120ns to provide an internal hold time for Start/Stop detection to bridge the undefined region of the falling edge of SCL. The delay needs to be smaller than $t_{HD.STA}$ 260ns.

6 Device specifications

6.1 Absolute maximum ratings (non operating)

Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated under “Operating Conditions” is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Parameter	Symbol	Min	Max	Unit	Note
DC supply voltage	VDD	-0.3	5	V	
Peripheral supply voltage	VDDp	-0.3	5 VDD +0.3	V	
Input pin voltage	Vin	-0.3	VDDp +0.3	V	
Input pin voltage	Vin	-	3.6	V	
Input current (latchup immunity)	I_{scr}	-100	100	mA	Norm: JEDEC 78
Electrostatic discharge	ESD	-	±2	kV	Norm: MIL 883 E method 3015, direct pad contact
Package Thermal Resistance	Θ_{JA}	-	32	K/W	Velocity=0, Multi Layer PCB; JEDEC Standard Testboard
Storage temperature	T_{strg}	-55	125	°C	
Package body temperature	T_{body}		260	°C	Norm: IPC/JEDEC J-STD-020 (1) (2)
Humidity non-condensing		5	85	%	

Notes:
(1) The reflow peak soldering temperature (body temperature) is specified according IPC/JEDEC J-STD-020 “Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices”.
(2) The lead finish for Pb-free leaded packages is “Matte Tin” (100% Sn)

6.2 Operating conditions

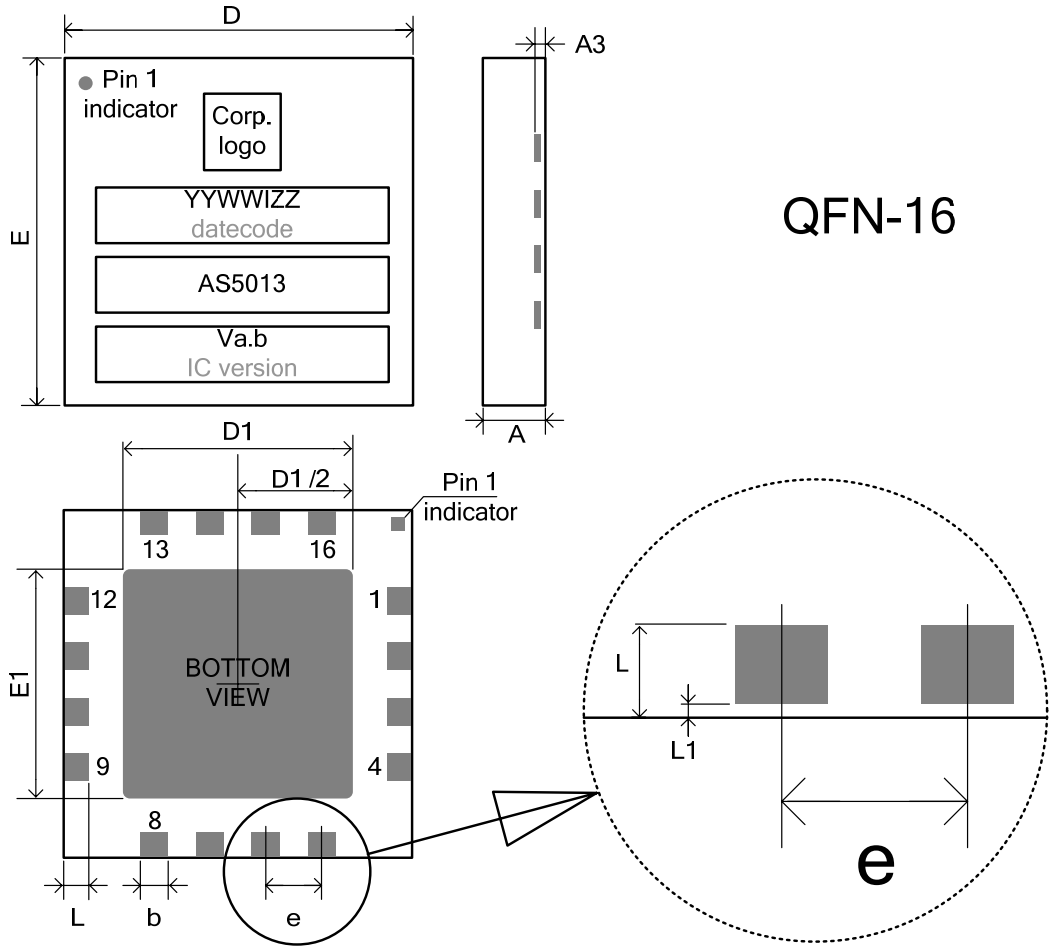
(operating conditions: T_{amb} = -20 to +80°C, VDD = 3.3V, RESETn = HIGH)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Core Supply voltage	VDD	2.7		3.6	V	
Peripheral Supply voltage	VDDp	1.7		VDD	V	Input: RESETn Open drain outputs: SCL, SDA, INTn. External I2C pull up resistor to be connected to VDDp.
Maximal average current consumption on VDD depends on the sampling time ts[ms]	IDD_s	3+3760/ts [ms]			µA	Sampling time ts[ms] Pulsed peaks IDDf
Current consumption on core supply, Idle mode, no readout	IDD_I			3	µA	no sampling (ts = infinite)
Current consumption on core supply, Idle mode, continuous readout	IDD_f			10	mA	continuous current pin VDD Maximum sampling ts = 450µs
Power up time analog	Tpua			1000	us	Step on VDD to Data_Ready
Conversion time	Tconv			450	us	Read X/Y coordinate I²C Y_res_int ACK bit of to Data_Ready
Nominal wakeup time	$t_{P,W}$	20		320	ms	see to the chapter power modes
lateral movement radius	dx dy			2	mm	The range depends on the magnet and the distance to the surface, $dx^2+dy^2 <= 4$ mm
type of magnet	d	2		3	mm	cylindrical; axial magnetized
Hall array diameter	RH		2.2		mm	
magnetic field strength	B_Z	30		120	mT	vertical magnetic field at magnet center; measured at chip surface
Ambient temperature range	T_{amb}	-20		+80	°C	
Resolution of XY displacement			8		bit	over 2*dx and 2*dy axis
Noise (RMS)				100	µT	C1..C5 channel data (result from two measurement – pos and neg current spinning)
PSRR Power Supply Rejection Ratio				0.2	%/100mV	conditions : VDD=3.3V; Temp = 25°C dVDD= 100 mVpp @ 10..30 kHz
IC package		QFN16 4x4x0.55mm				
Power supply filtering capacitors		100			nF	Ceramic capacitor VDD - VSS
		100			nF	Ceramic capacitor VDDp - VSS

6.3 Digital IO pads DC/AC characteristics

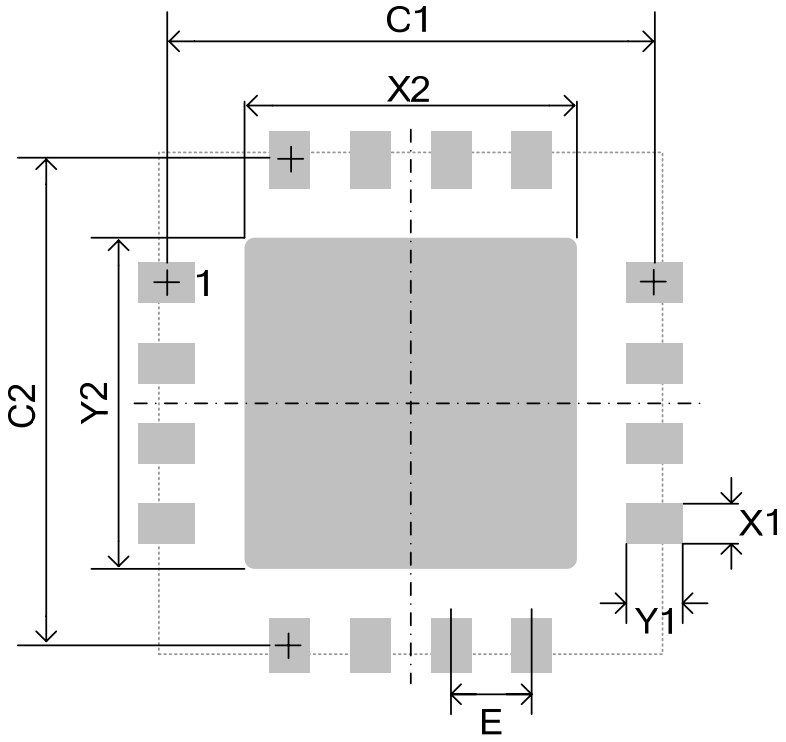
Parameter	Symbol	Min	Max	Unit	Note
Inputs: SCL, SDA					
High level input voltage	V_{IH}	0.7 * VDDp		V	IIC
Low level input voltage	VIL		0.3 * VDDp	V	IIC
Input leakage current	I_{LEAK}		1	µA	VDDp = 3.6V
Inputs: ADDR,RESETn (JEDEC76)					
High level input voltage	V_{IH}	0.65 * VDDp		V	JEDEC
Low level input voltage	VIL		0.35 * VDDp	V	JEDEC
Input leakage current	I_{LEAK}		1	µA	VDDp = 3.6V
Outputs: SDA					
High level output voltage	V_{OH}	Open drain		Leakage current 1 µA	High level output voltage
Low level output voltage	V_{OL1}		VSS + 0.4	V	-6mA; VDDP > 2V; fast mode
Low level output voltage	V_{OL3}		VDDP*0.2	V	-6mA; VDDP <= 2V; fast mode
Low level output voltage	V_{OL1}		VSS + 0.4	V	-3mA; VDDP > 2V; high speed
Low level output voltage	V_{OL3}		VDDP*0.2	V	-3mA; VDDP <= 2V; high speed
Capacitive load	C_L		400	pF	standard mode (100 kHz)
Capacitive load	C_L		400	pF	fast mode (400 kHz)
Capacitive load	C_L		100	pF	high speed mode (3.4 MHz)
Outputs: INTn (JEDEC76)					
High level output voltage	V_{OH}	Open drain		Leakage current 1 µA	High level output voltage
Low level output voltage	V_{OL}		VSS + 0.2	V	-100uA;
Low level output voltage	V_{OL}		VSS + 0.45	V	-2mA;
Capacitive load	C_L		30	pF	standard mode (100 kHz)

7 Package Drawings



DIM (mm)	MIN	NOM	MAX
A	0.50	0.55	0.60
A3		0.152 REF	
b	0.18	0.23	0.28
D		4.00 BSC	
E		4.00 BSC	
D1	2.60	2.70	2.80
E1	2.60	2.70	2.80
e		0.65 BSC	
L	0.35	0.40	0.45
L1	0.00		0.10

8 Recommended footprint



DIM (mm)	Typ
C1	3.7
C2	3.7
E	0.65
X1	0.40
Y1	0.7
X2	2.6
Y2	2.6

9 Recommended mounting

The typical mounting configuration of the AS5013 with the mechanics is on both sides of the PCB:
- Mechanics + Magnet on the top side
- AS5013 IC on the bottom side

A thickness of 0.6mm to 1.0mm for the PCB is recommended.

A dome switch for push button function can be added as well.

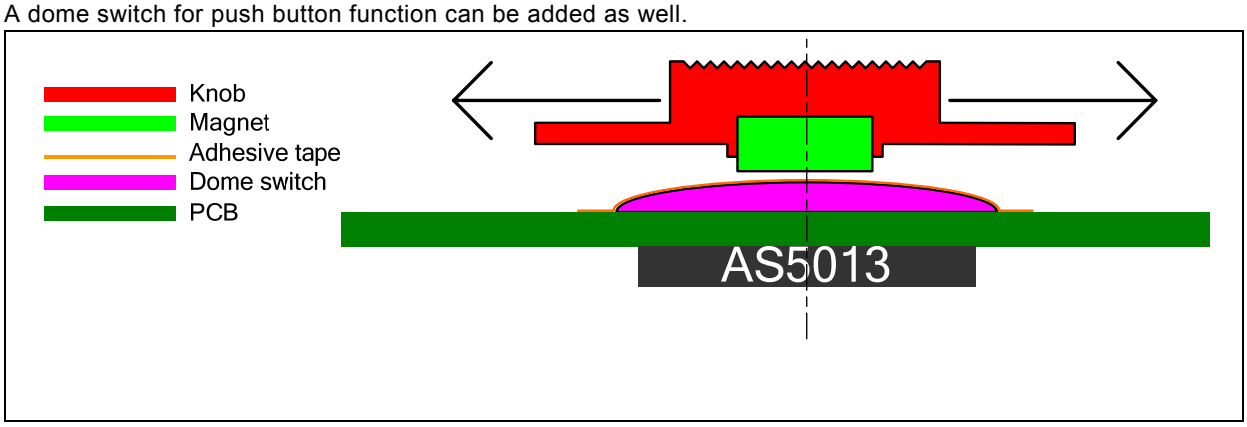


Figure 17: AS5013 mounting example for low profile joystick.

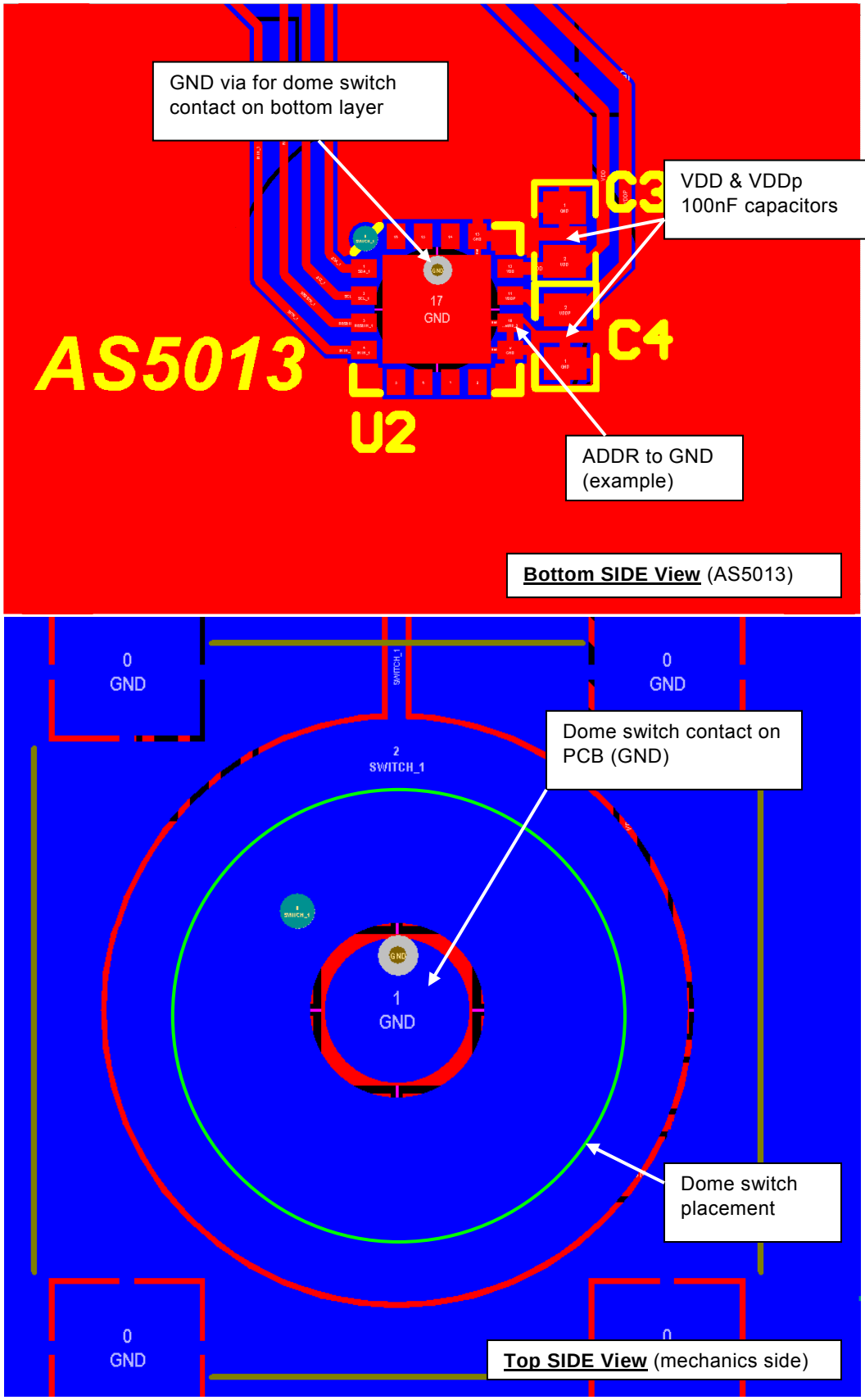


Figure 18: Layout example for low profile joystick

Table of contents

Revision History

Revision	Date	Description
0.02	06.04.2010	• Preliminary
1.00	15.06.2010	• Y_res_int ACK resets INTn, not STOP bit • Bit Soft_rst description inverted (soft_rst = Normal mode) • Control register 2 bit 7: always 1 and Test bits fixed to '0' • Added PSSR and Noise values
1.01	02.07.2010	• Chapter 4.13, step 5: Write 86h to Control register 2, for magnet polarity inversion
1.02	19.07.2010	• Chapter 5, I²C address inverted (40h and 41h for 1000 000 and 1000 001)
1.03	22.07.2010	• Chapter 4.12: Power ON Sequence added
1.04	16.08.2010	• Chapter 2 & 6.1: ESD direct pad contact +-2kV
1.05	20.09.2010	• I²C Timings diagrams: improved pictures resolution
1.06	16.12.2010	• Chapter 5.2: Changed VDD to VDDp references for I²C levels

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