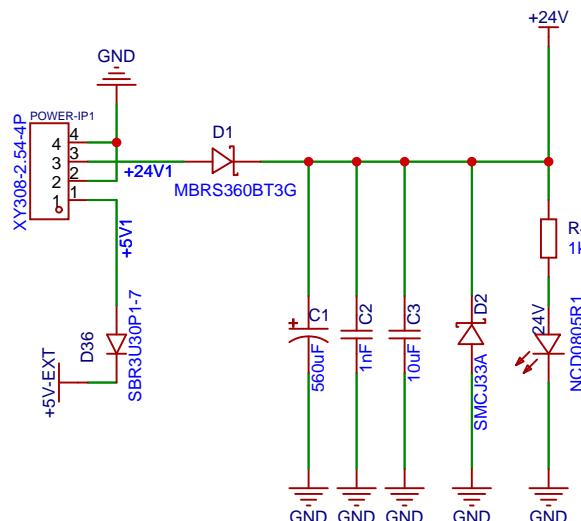


# DC 24V PROTECTION



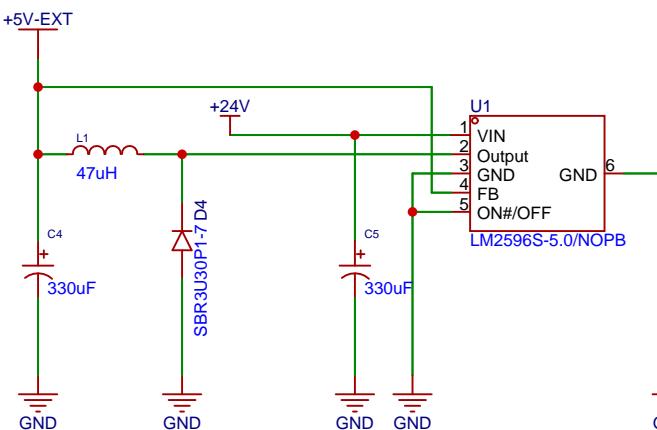
Schematic	Main-Controller-Schem_3			Update Date	2025-08-22
Create Date	2025-08-21			Part Number	JLCPCB-002
Page	24V-Power-Protection			Drawn	EasyEDA
Reviewed	EasyEDA			Reviewed	EasyEDA
	DAC-Main-controller			VER	SIZE
				PAGE	1 OF 9
 EasyEDA			V0.1	A4	EasyEDA.com

**NOTES**

CHANGE 1: Got rid of the BJT 5V Protection  
 CHANGE 2: Replaced inductor L1 (C16726S) which saturated at 2.5A with (C149599) which saturates at 3A.  
 CHANGE 3: Got rid of 12V power protection and added 24V power protection.

1 2 3 4 5 6

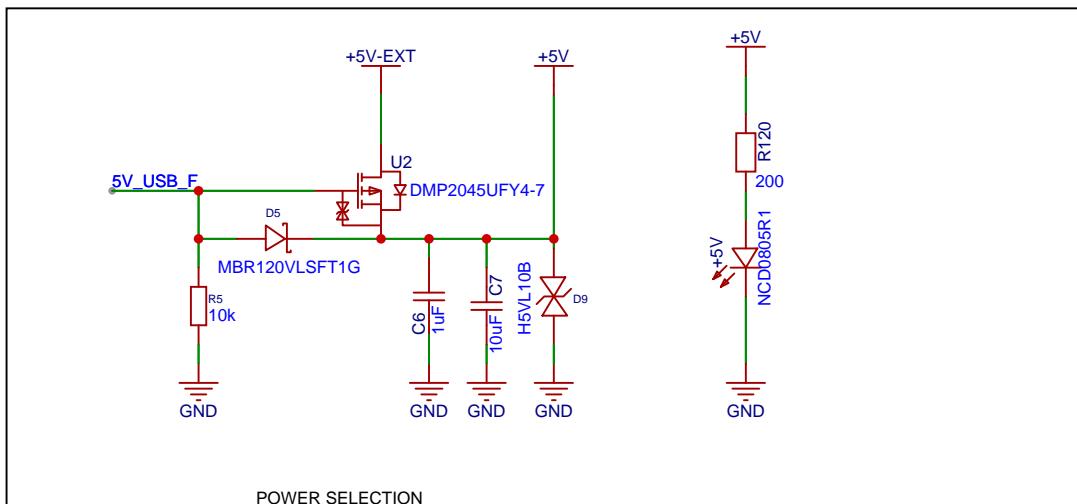
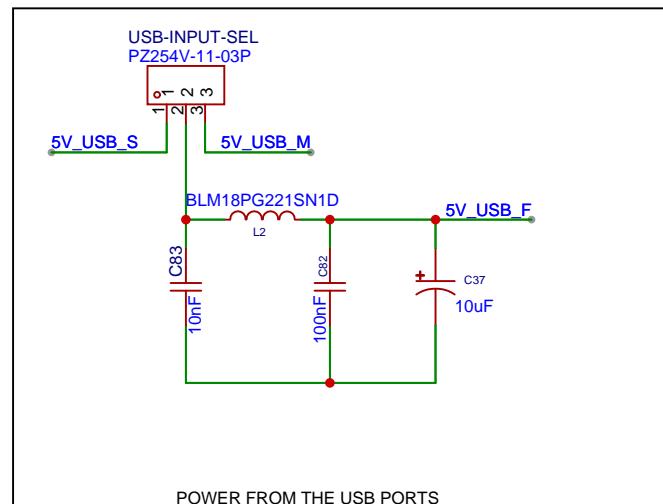
## BUCK 12V - 5V OUTPUT



Schematic	Main-Controller-Schem_3			Update Date	2025-08-21
Create Date	2025-08-21			Part Number	JLCPCB-002
Page	5V-Power			Drawn	EasyEDA
Reviewed	EasyEDA			Reviewed	EasyEDA
	DAC-Main-controller			VER	SIZE
				PAGE	2 OF 9
 EasyEDA.com		V0.1	A4		

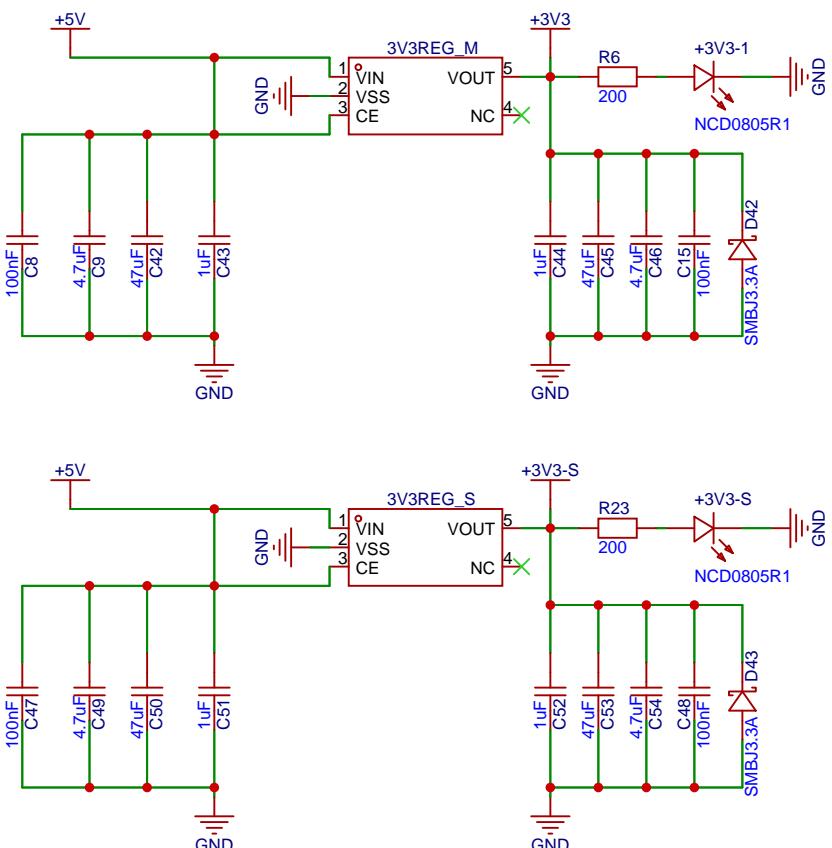
1 2 3 4 5 6

# POWER SUPPLY SELECTION

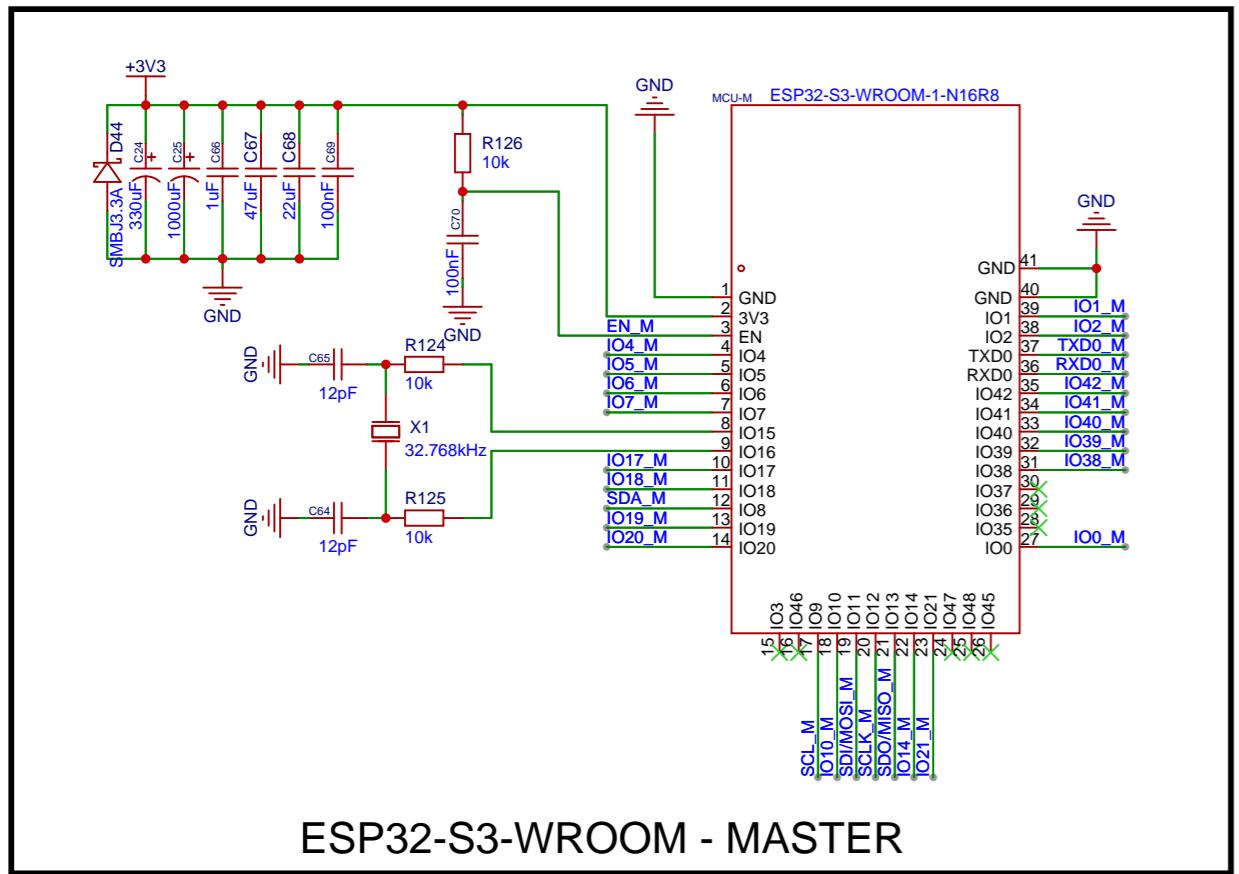


Schematic	Main-Controller-Schem_3			Update Date	2025-10-16
Create Date	2025-08-21			Part Number	JLCPCB-002
Page	Power-Selection			Drawn	EasyEDA
Reviewed	EasyEDA			Reviewed	EasyEDA
	DAC-Main-controller			VER	SIZE
				PAGE	3 OF 9
				V0.1	A4
				EasyEDA.com	

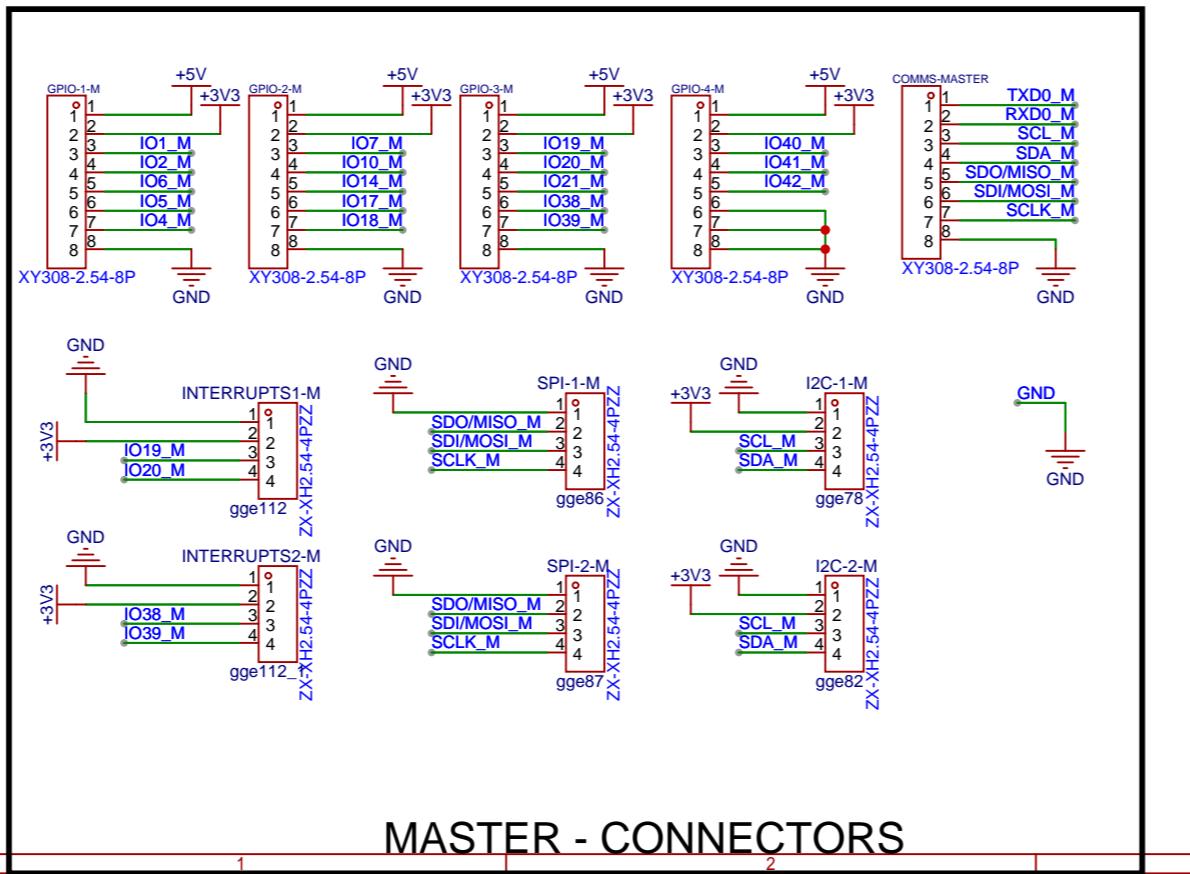
## DC 5V TO DC 3V3



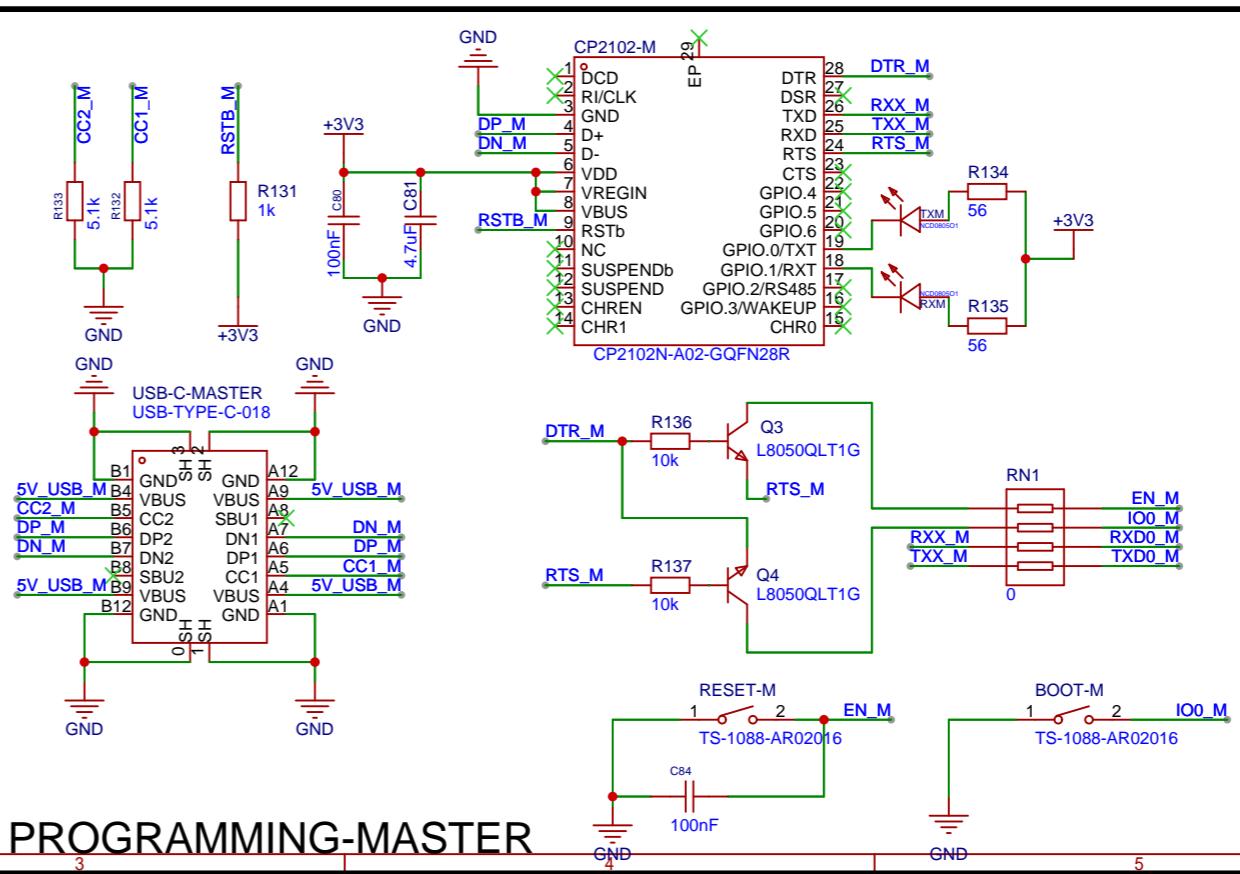
Schematic	Main-Controller-Schem_3			Update Date	2025-09-08	
Page	3V3-Power			Create Date	2025-08-21	
Drawn	EasyEDA	DAC-Main-controller			Part Number	JLCPCB-002
Reviewed	EasyEDA					
		VER	SIZE	PAGE	4 OF 9	
 EasyEDA		V0.1	A4	EasyEDA.com		



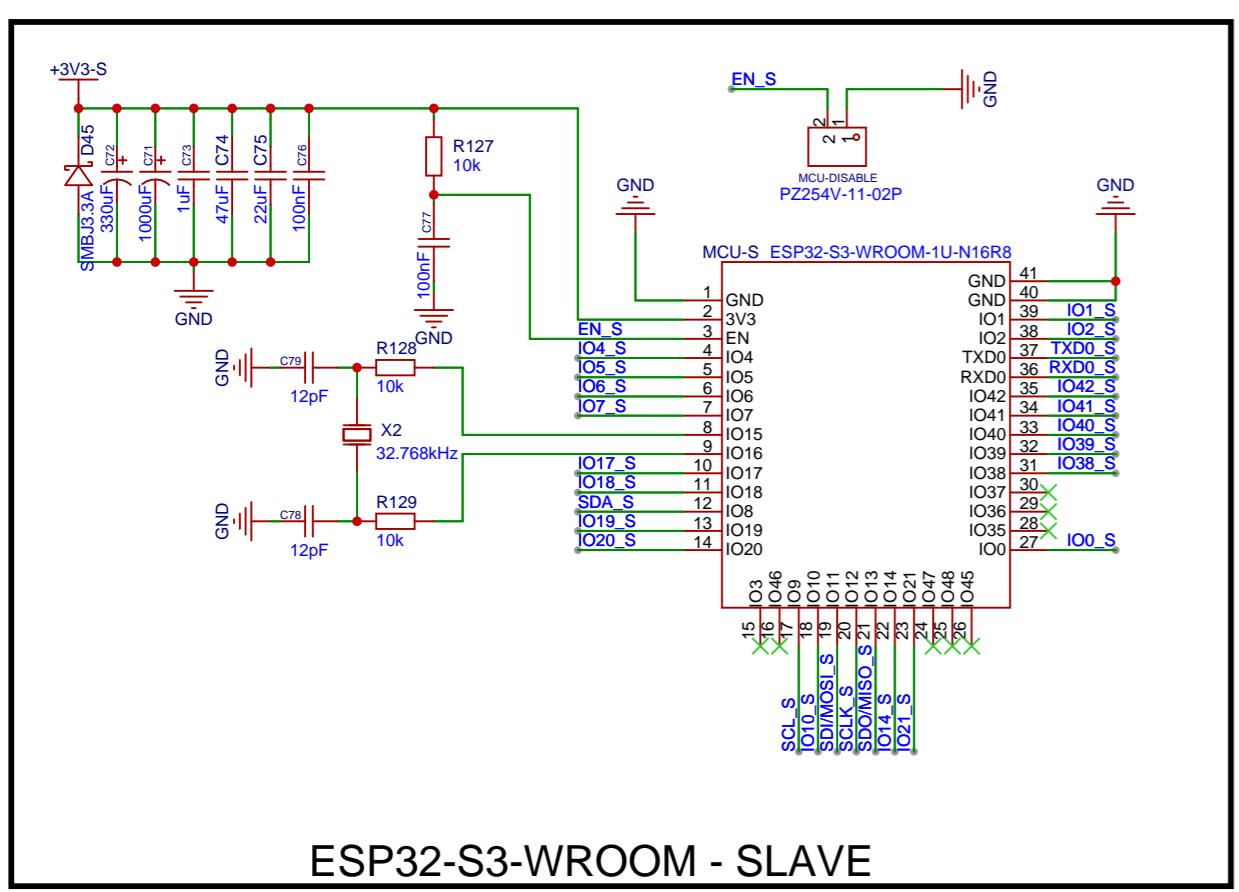
ESP32-S3-WROOM - MASTER



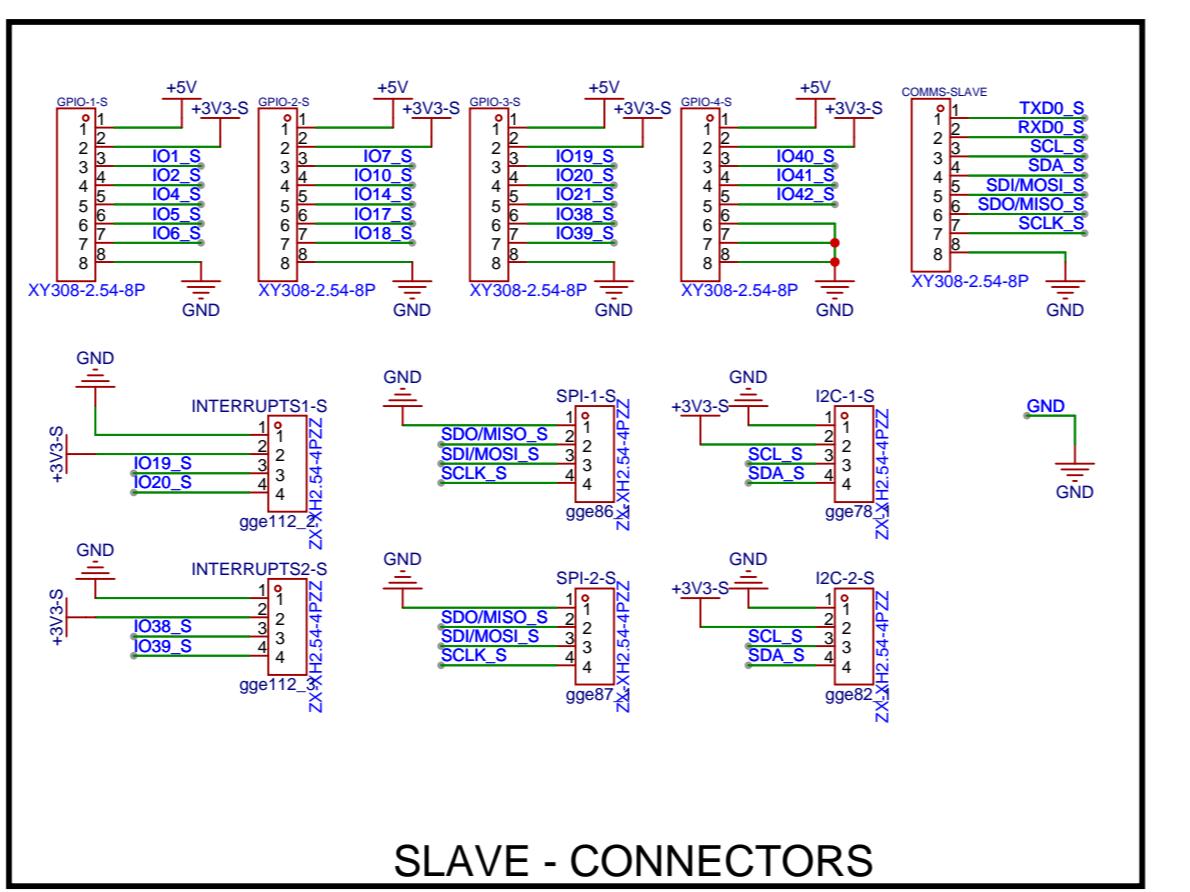
## MASTER - CONNECTORS



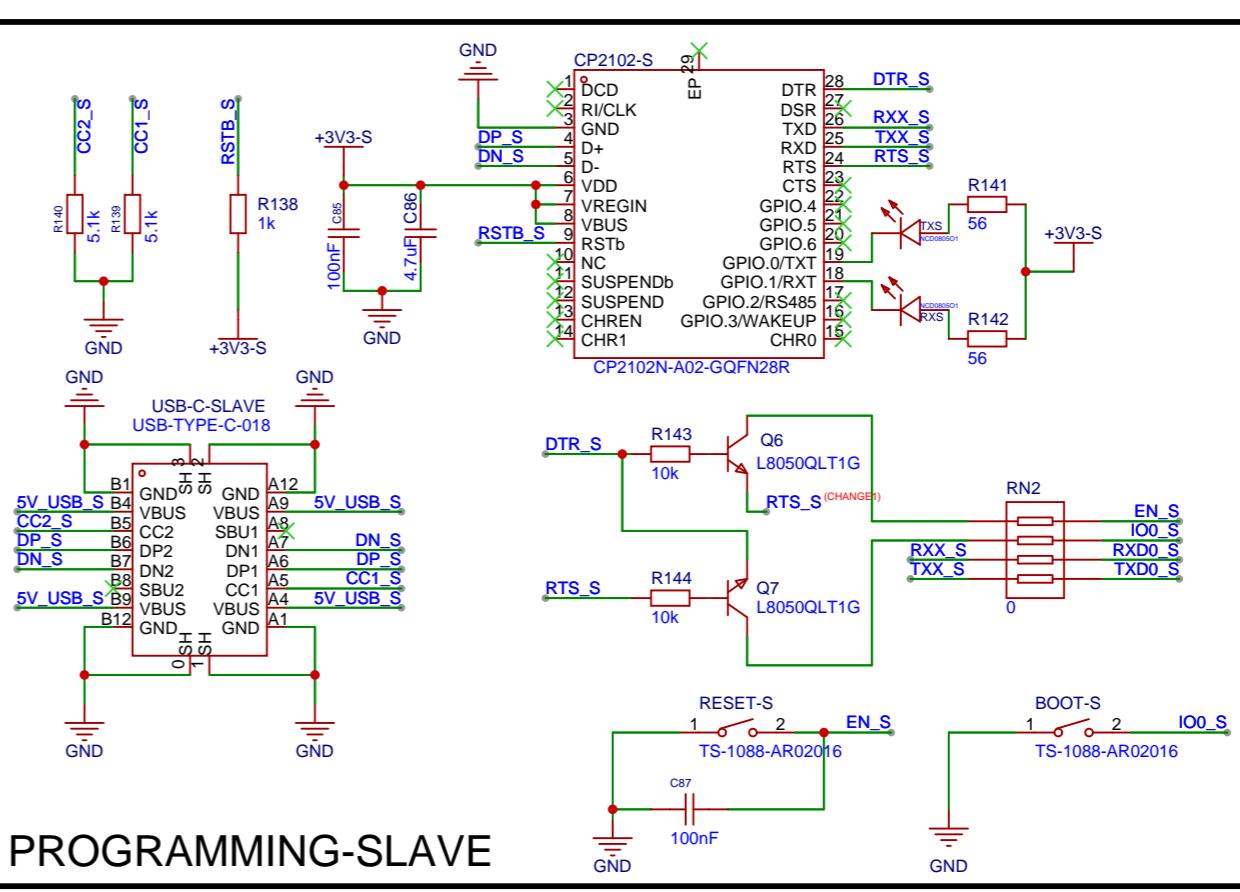
PROGRAMMING-MASTER



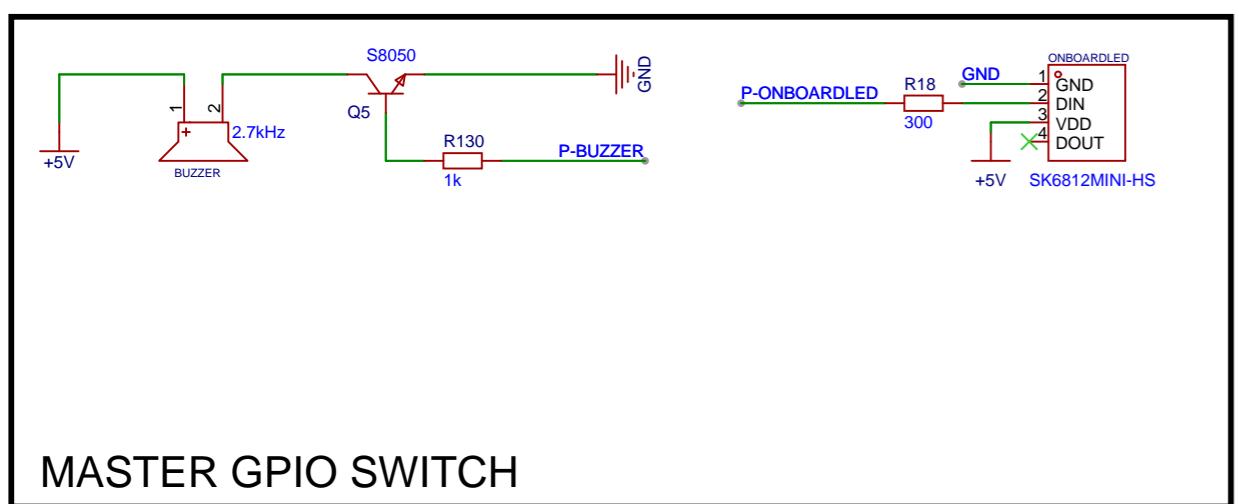
ESP32-S3-WROOM - SLAVE



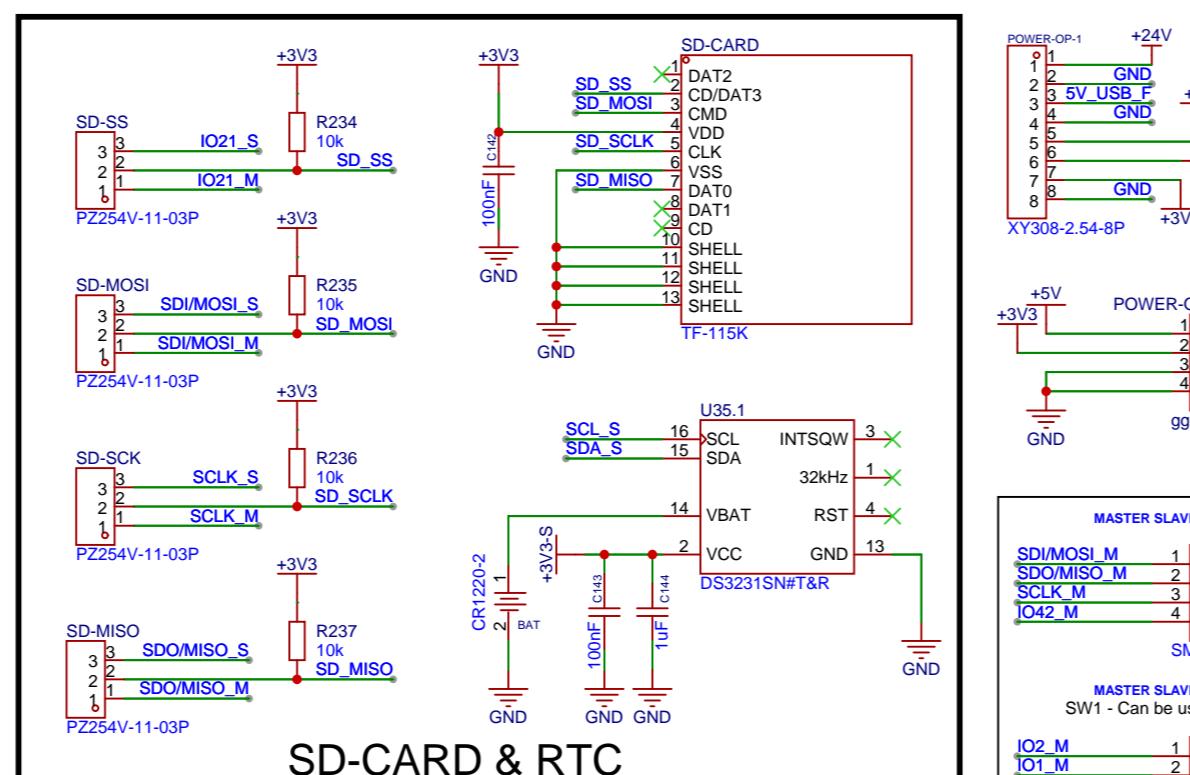
## SLAVE - CONNECTORS



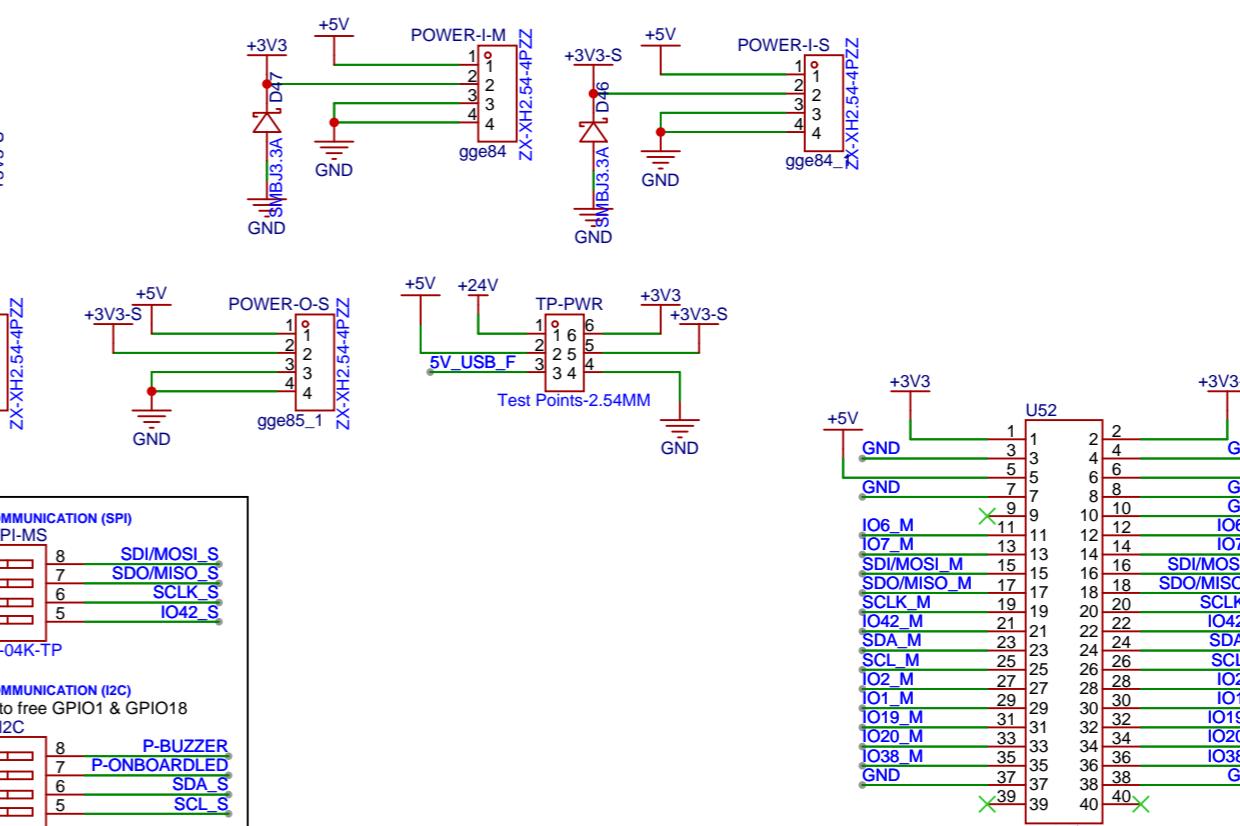
# PROGRAMMING-SLAVE



## MASTER GPIO SWITCH



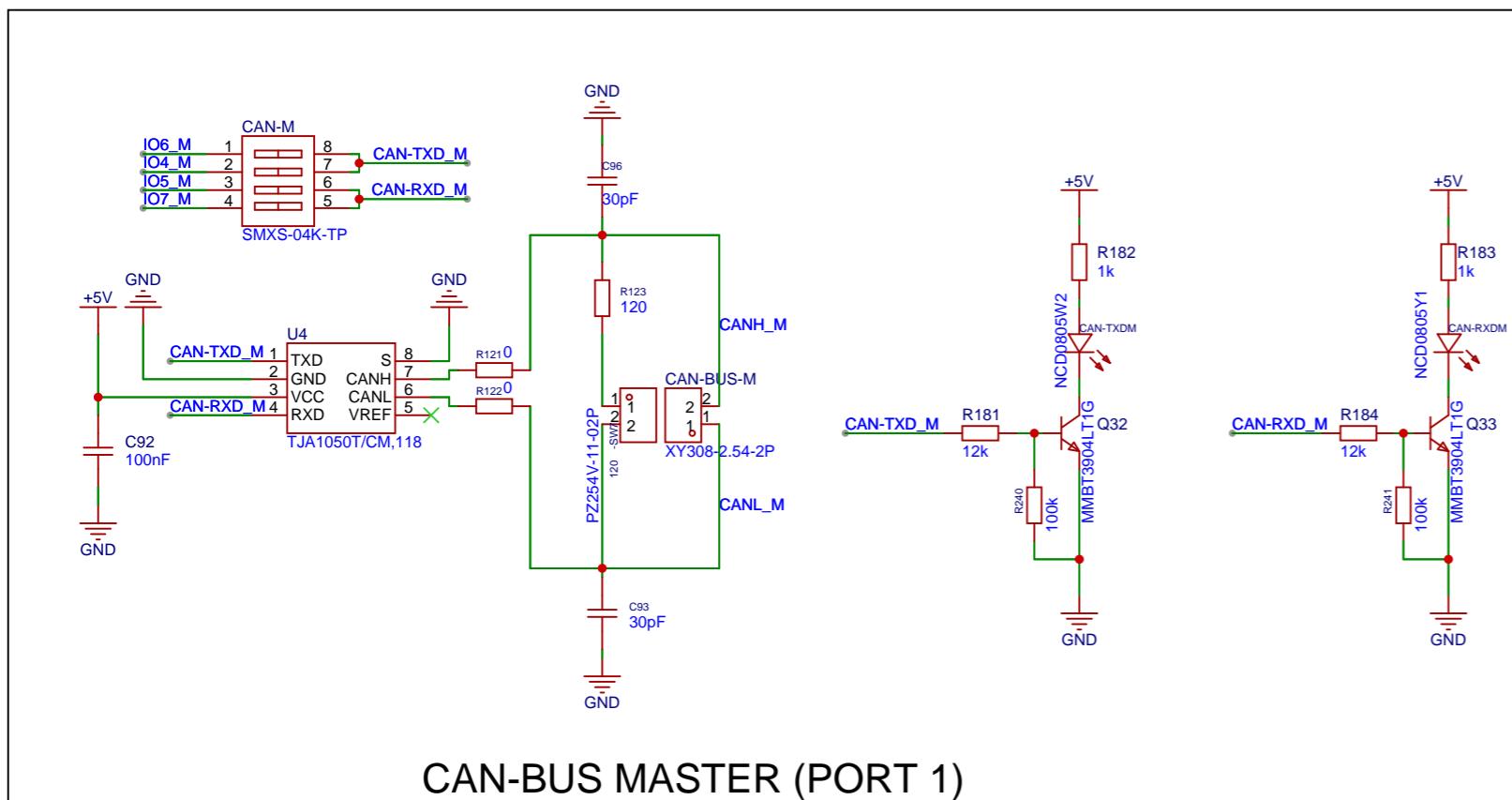
GND GM



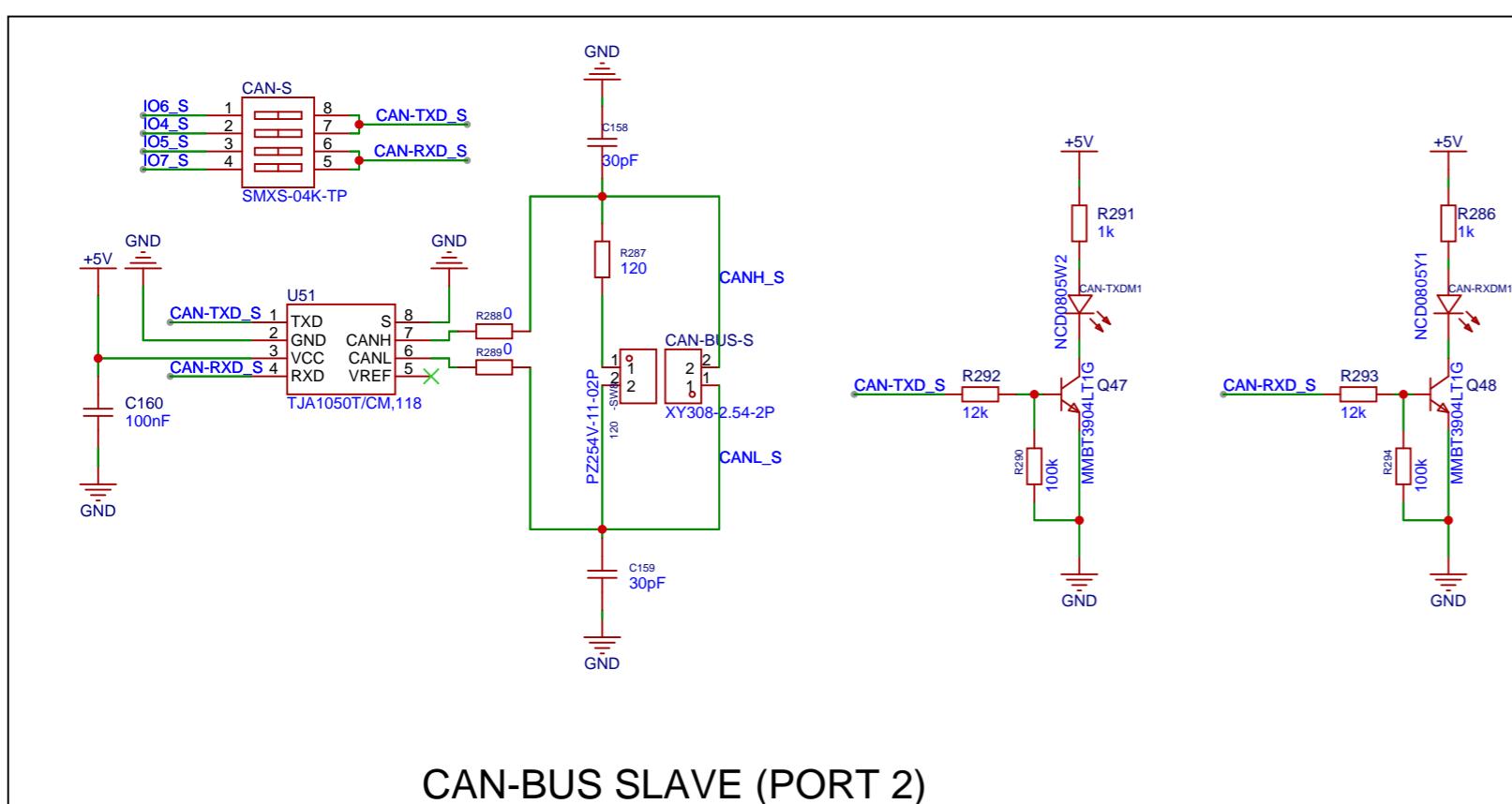
Main Controller Schem. 3

Schematic	Main-Controller-Schem_3	Update Date	2025-10-16
		Create Date	2025-08-21
Page	ESP32-Module	Part Number	001

DAC-Main-controller

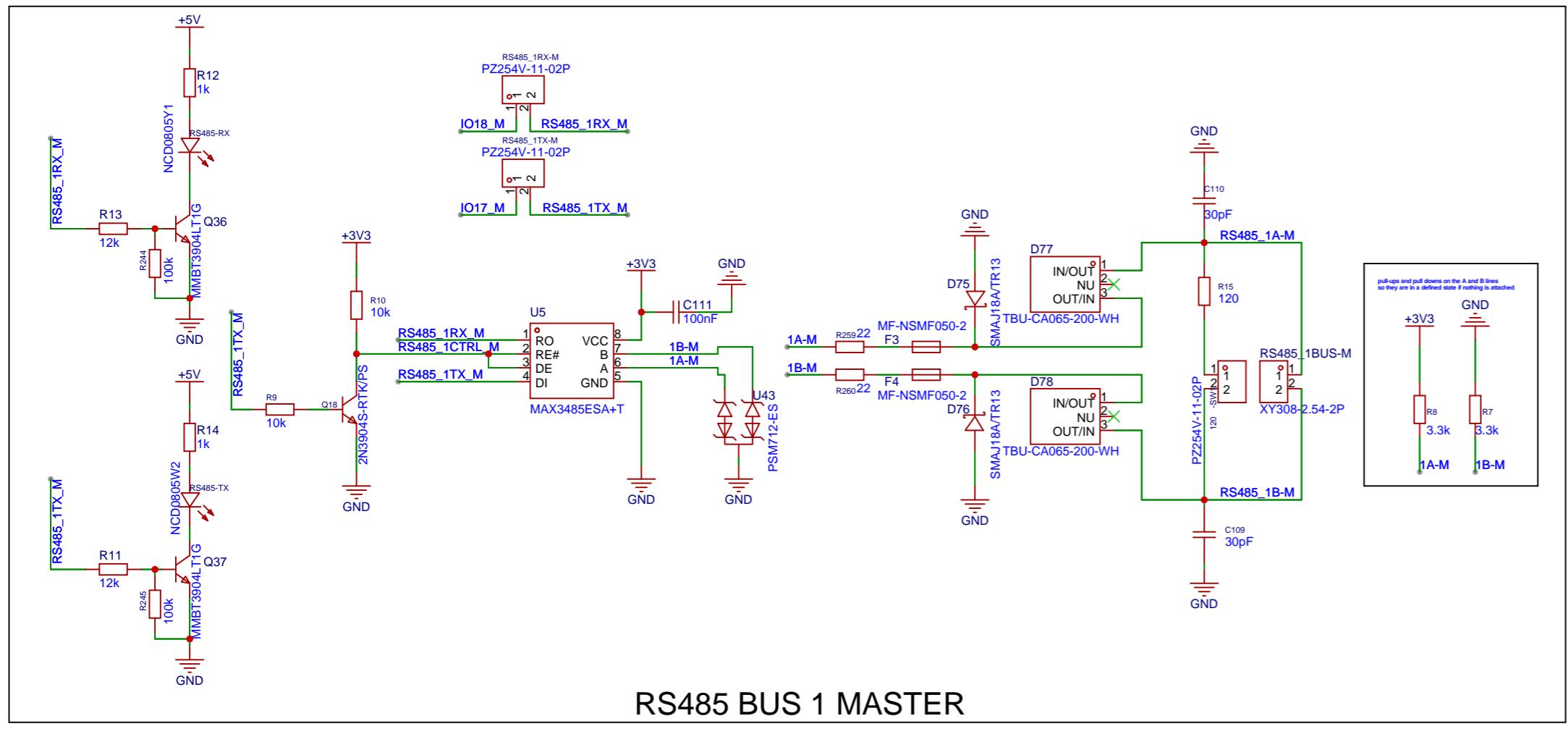


CAN-BUS MASTER (PORT 1)

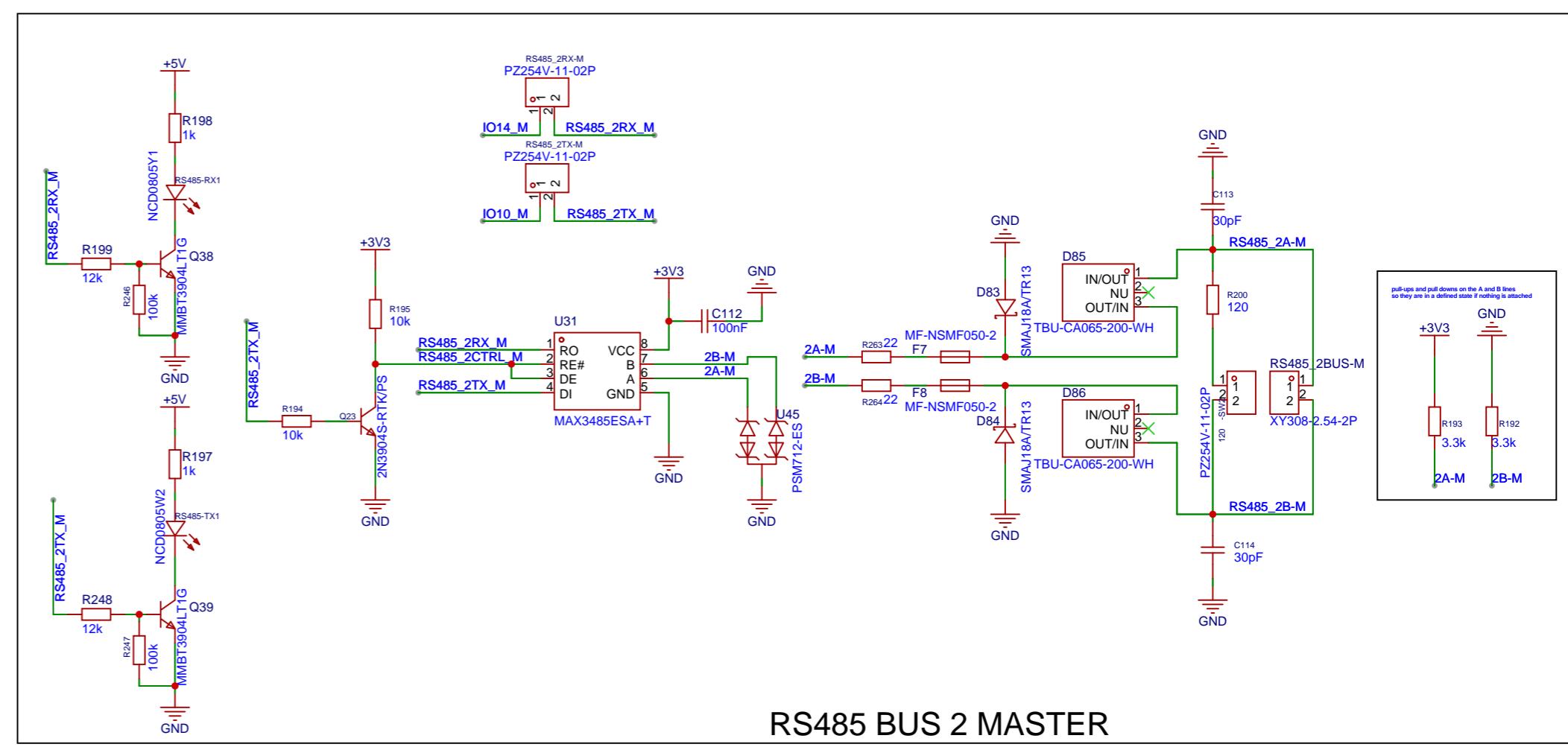


CAN-BUS SLAVE (PORT 2)

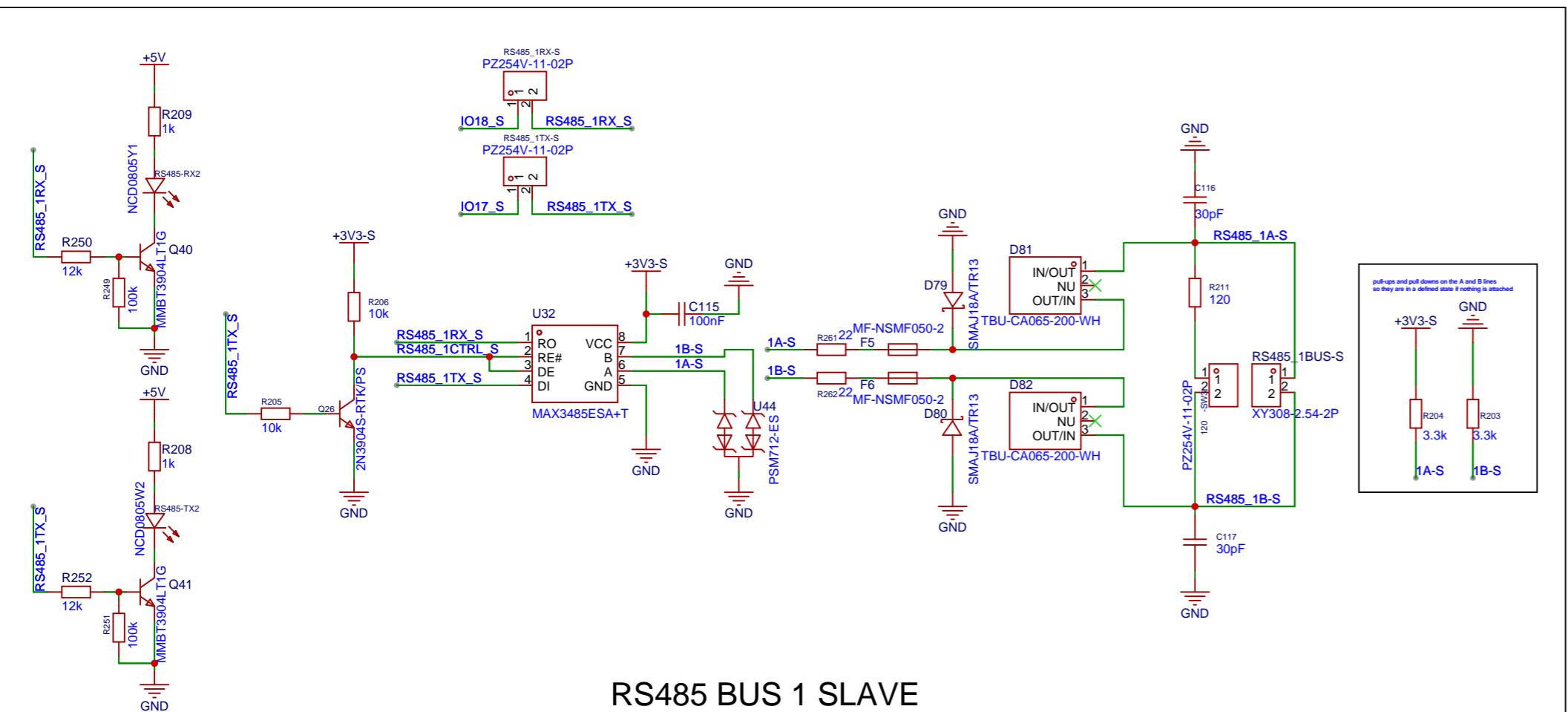
Schematic	Main-Controller-Schem_3		Update Date	2025-10-16
Page	CAN-Bus		Create Date	2025-08-21
Drawn	EasyEDA			Part Number
Reviewed	EasyEDA			JLCPCB-002
	DAC-Main-controller			
			VER	SIZE
			PAGE	6 OF 9
EasyEDA		V0.1	A4	EasyEDA.com



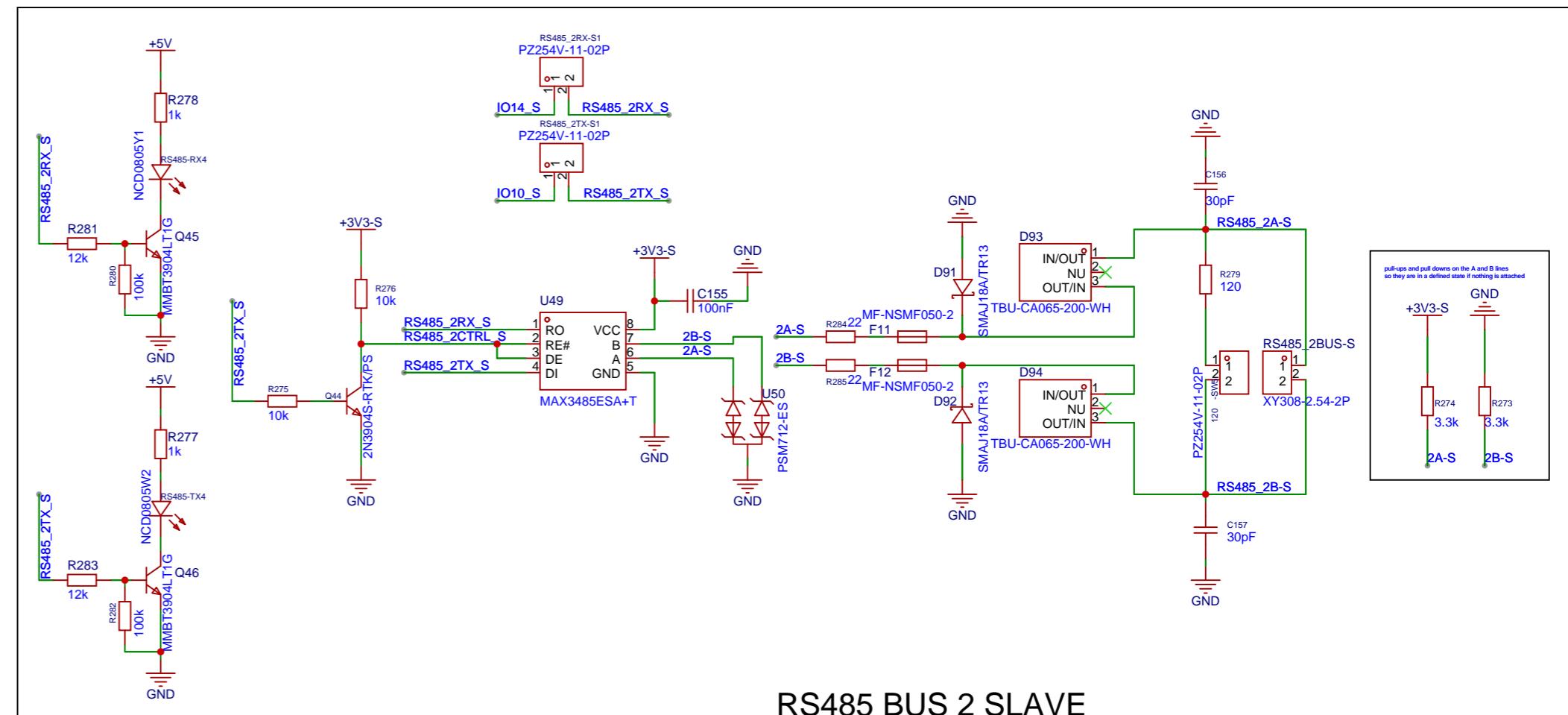
RS485 BUS 1 MASTER



RS485 BUS 2 MASTER

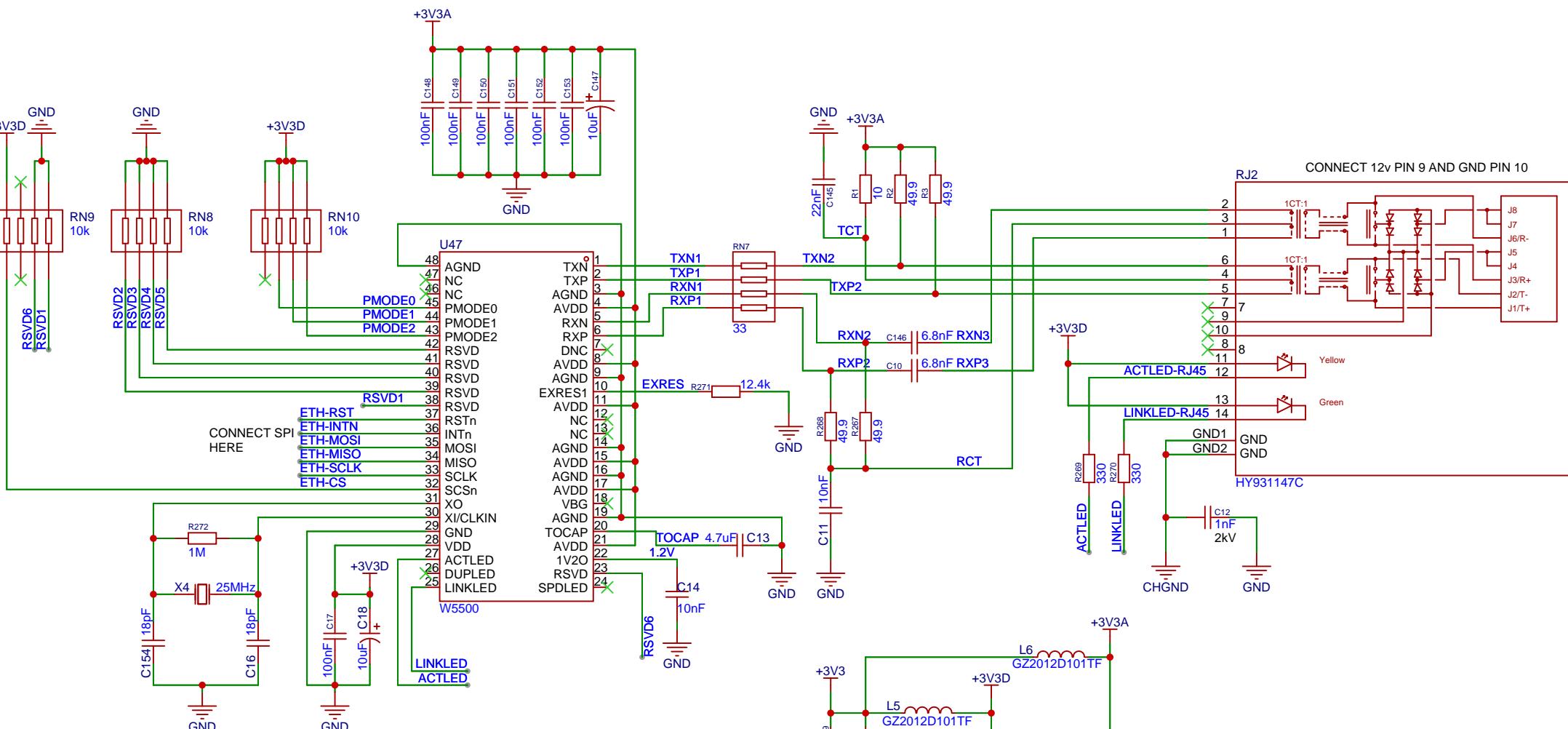


RS485 BUS 1 SLAVE



RS485 BUS 2 SLAVE

Schematic	Main-Controller-Schem_3	Update Date	2025-09-12
Page	RS485-Bus	Create Date	2025-08-21
Drawn	EasyEDA	Part Number	JLCPCB-002
DAC-Main-controller			
Reviewed	EasyEDA	VER	7
		SIZE	OF 9
		PAGE	7
		V0.1	A4
EasyEDA.com			



ETH-RST-SEL ETH-MOSI-SEL ETH-MISO-SEL ETH-SLCK-SEL ETH-CS-SEL ETH-INTN  
PZ254V-11-03P PZ254V-11-03P PZ254V-11-03P PZ254V-11-03P PZ254V-11-03P

This diagram illustrates the internal connections of the CLK MUX section. It shows how multiple MUXes (M1 through M5) and switches (SW1 through SW5) are interconnected to provide various clock paths. The connections are color-coded: red for M1/M2, green for M3/M4, and blue for M5.

Schematic	Main-Controller-Schem_3		Update Date	2025-10-16
			Create Date	2025-08-21
Page	Ethernet		Part Number	JLCPCB-002
Drawn	EasyEDA	DAC-Main-controller		
Reviewed	EasyEDA			
		VER	SIZE	PAGE 8 OF 9
 EasyEDA		V0.1	A4	EasyEDA.com

