3.1 What is the difference between event-driven and multi-threading concurrency

3.2 Low-Energy Earliest Deadline First

Task	Arrival Time [s]	Deadline [s]	Length [MI]
t1	0	4	900
t2	2	8	1800
t3	2.5	8	450
t4	5	20	1000
t5	6	14	800

Processor Speed [MIPS]	Voltage
200	1.5
300	2
450	3.5

$t_0 = 0$:

$$0 + \frac{900}{200} \not\leq 4 \;\Rightarrow\; \text{FALSE}$$

$$0 + \frac{900}{300} \leq 4 \;\Rightarrow\; t = 3 \Rightarrow t1 \; scheduled \; on \; 2V$$

$t_1 = 2$:

$$2 + \frac{300}{200} \leq 4 \Rightarrow\; t = 3.5 \Rightarrow \exists \tau_2 \; with \; 1800 \; MI: 3.5 + \frac{1800}{450} = 7.5 \leq 8 \Rightarrow t1 \; scheduled \; on \; 1.5V$$

$t_2 = 2.5$:

$$2.5 + \frac{200}{200} \leq 4 \Rightarrow\; t = 3.5 \Rightarrow \exists \tau_2 \; with \; 1800 \; MI: 3.5 + \frac{1800}{450} = 7.5 \leq 8 \Rightarrow \exists \tau_3 \; with \; 450 \; MI: 7.5 + \frac{450}{450} = 8.5 \not\leq 8 \Rightarrow \text{BREAK}$$

$$2.5 + \frac{200}{300} \leq 4 \Rightarrow\; t = 3.1\overline{6} \Rightarrow \exists \tau_2 \; with \; 1800 \; MI: 3.1\overline{6} + \frac{1800}{450} = 7.1\overline{6} \leq 8 \Rightarrow \exists \tau_3 \; with \; 450 \; MI: 7.1\overline{6} + \frac{450}{450} = 8.1\overline{6} \not\leq 8 \Rightarrow \text{BREAK}$$

$$2.5 + \frac{200}{450} \leq 4 \Rightarrow\; t = 2.9\overline{4} \Rightarrow \exists \tau_2 \; with \; 1800 \; MI: 2.9\overline{4} + \frac{1800}{450} = 6.9\overline{4} \leq 8 \Rightarrow \exists \tau_3 \; with \; 450 \; MI: 6.9\overline{4} + \frac{450}{450} = 7.9\overline{4} \leq 8 \Rightarrow \text{OK}$$

$t_3 = 5$:

$$7.9\overline{4} + \frac{1000}{450} \leq 20 \Rightarrow \text{OK}$$

$t_4 = 6$:

$$7.9\overline{4} + \frac{800}{450} = 9.7\overline{1} \leq 14 \Rightarrow 9.7\overline{1} + \frac{1000}{450} \leq 20 \Rightarrow \text{OK}$$

$t_6 = 7.9\overline{4}$:

$$7.9\overline{4} + \frac{800}{200} = 11.9\overline{4} \leq 14 \;\Rightarrow \exists \tau_5 \; with \; 1000 \; MI: 11.9\overline{4} + \frac{1000}{450} = 14.1\overline{6} \leq 20 \Rightarrow \text{OK}$$

$t_5 = 11.9\overline{4}$:

$$11.9\overline{4} + \frac{1000}{200} = 16.9\overline{4} \leq 20 \Rightarrow t5 \; scheduled \; on \; 1.5V$$

Therefore we get the execution plan:

Time[s]	Processor Speed [MIPS]	Voltage
0-2	300	2V
2-2.5	200	1.5V
2.5-$7.9\overline{4}$	450	3.5V
$7.9\overline{4}$-$16.9\overline{4}$	200	1.5V