# DATA SHEET

# PCD8544
## 48 × 84 pixels matrix LCD controller/driver

Product specification
File under Integrated Circuits, IC17

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Philips
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**CONTENTS**

## 1 FEATURES

- Single chip LCD controller/driver
- 48 row, 84 column outputs
- Display data RAM 48 × 84 bits
- On-chip:
  - Generation of LCD supply voltage (external supply also possible)
  - Generation of intermediate LCD bias voltages
  - Oscillator requires no external components (external clock also possible).
- External $\overline{\text{RES}}$ (reset) input pin
- Serial interface maximum 4.0 Mbits/s
- CMOS compatible inputs
- Mux rate: 48
- Logic supply voltage range $V_{DD}$ to $V_{SS}$: 2.7 to 3.3 V
- Display supply voltage range $V_{LCD}$ to $V_{SS}$
  - 6.0 to 8.5 V with LCD voltage internally generated (voltage generator enabled)
  - 6.0 to 9.0 V with LCD voltage externally supplied (voltage generator switched-off).
- Low power consumption, suitable for battery operated systems
- Temperature compensation of $V_{LCD}$
- Temperature range: –25 to +70 °C.

## 2 GENERAL DESCRIPTION

The PCD8544 is a low power CMOS LCD controller/driver, designed to drive a graphic display of 48 rows and 84 columns. All necessary functions for the display are provided in a single chip, including on-chip generation of LCD supply and bias voltages, resulting in a minimum of external components and low power consumption.

The PCD8544 interfaces to microcontrollers through a serial bus interface.

The PCD8544 is manufactured in n-well CMOS technology.

## 3 APPLICATIONS

- Telecommunications equipment.

## 4 ORDERING INFORMATION

| TYPE NUMBER | PACKAGE | | |
|---|---|---|---|
| | NAME | DESCRIPTION | VERSION |
| PCD8544U | – | chip with bumps in tray; 168 bonding pads + 4 dummy pads | – |

## 5 BLOCK DIAGRAM

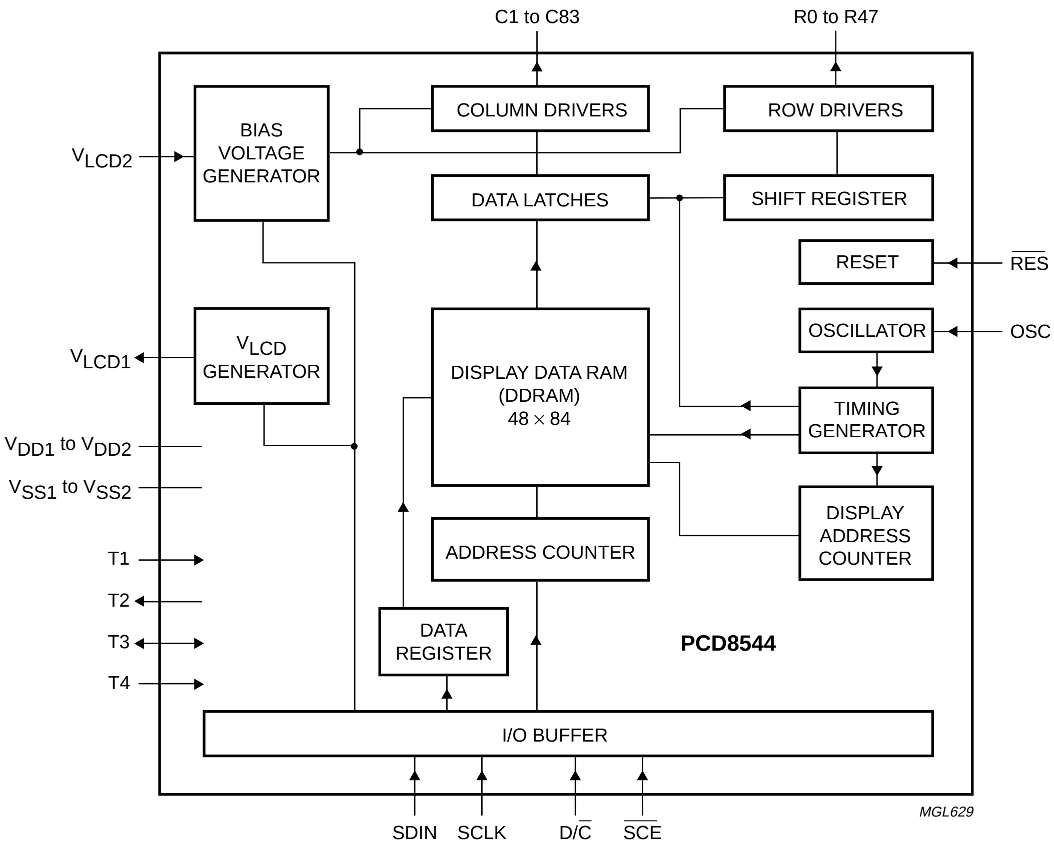



Fig.1 Block diagram.

## 6 PINNING

| SYMBOL | DESCRIPTION |
|---|---|
| R0 to R47 | LCD row driver outputs |
| C0 to C83 | LCD column driver outputs |
| $V_{SS1}$, $V_{SS2}$ | ground |
| $V_{DD1}$, $V_{DD2}$ | supply voltage |
| $V_{LCD1}$, $V_{LCD2}$ | LCD supply voltage |
| T1 | test 1 input |
| T2 | test 2 output |
| T3 | test 3 input/output |
| T4 | test 4 input |
| SDIN | serial data input |
| SCLK | serial clock input |
| D/$\overline{\text{C}}$ | data/$\overline{\text{command}}$ |
| $\overline{\text{SCE}}$ | chip enable |
| OSC | oscillator |
| $\overline{\text{RES}}$ | external reset input |
| dummy1, 2, 3, 4 | not connected |

**Note**

1. For further details, see Fig.18 and Table 7.

### 6.1 Pin functions

#### 6.1.1 R0 TO R47 ROW DRIVER OUTPUTS

These pads output the row signals.

#### 6.1.2 C0 TO C83 COLUMN DRIVER OUTPUTS

These pads output the column signals.

#### 6.1.3 $V_{SS1}$, $V_{SS2}$: NEGATIVE POWER SUPPLY RAILS

Supply rails $V_{SS1}$ and $V_{SS2}$ must be connected together.

#### 6.1.4 $V_{DD1}$, $V_{DD2}$: POSITIVE POWER SUPPLY RAILS

Supply rails $V_{DD1}$ and $V_{DD2}$ must be connected together.

#### 6.1.5 $V_{LCD1}$, $V_{LCD2}$: LCD POWER SUPPLY

Positive power supply for the liquid crystal display. Supply rails $V_{LCD1}$ and $V_{LCD2}$ must be connected together.

#### 6.1.6 T1, T2, T3 AND T4: TEST PADS

T1, T3 and T4 must be connected to $V_{SS}$, T2 is to be left open. Not accessible to user.

#### 6.1.7 SDIN: SERIAL DATA LINE

Input for the data line.

#### 6.1.8 SCLK: SERIAL CLOCK LINE

Input for the clock signal: 0.0 to 4.0 Mbits/s.

#### 6.1.9 D/$\overline{\text{C}}$: MODE SELECT

Input to select either command/address or data input.

#### 6.1.10 $\overline{\text{SCE}}$: CHIP ENABLE

The enable pin allows data to be clocked in. The signal is active LOW.

#### 6.1.11 OSC: OSCILLATOR

When the on-chip oscillator is used, this input must be connected to $V_{DD}$. An external clock signal, if used, is connected to this input. If the oscillator and external clock are both inhibited by connecting the OSC pin to $V_{SS}$, the display is not clocked and may be left in a DC state.
To avoid this, the chip should always be put into Power-down mode before stopping the clock.

#### 6.1.12 $\overline{\text{RES}}$: RESET

This signal will reset the device and must be applied to properly initialize the chip. The signal is active LOW.

## 7 FUNCTIONAL DESCRIPTION

### 7.1 Oscillator

The on-chip oscillator provides the clock signal for the display system. No external components are required and the OSC input must be connected to $V_{DD}$. An external clock signal, if used, is connected to this input.

### 7.2 Address Counter (AC)

The address counter assigns addresses to the display data RAM for writing. The X-address $X_6$ to $X_0$ and the Y-address $Y_2$ to $Y_0$ are set separately. After a write operation, the address counter is automatically incremented by 1, according to the V flag.

### 7.3 Display Data RAM (DDRAM)

The DDRAM is a 48 × 84 bit static RAM which stores the display data. The RAM is divided into six banks of 84 bytes (6 × 8 × 84 bits). During RAM access, data is transferred to the RAM through the serial interface. There is a direct correspondence between the X-address and the column output number.

### 7.4 Timing generator

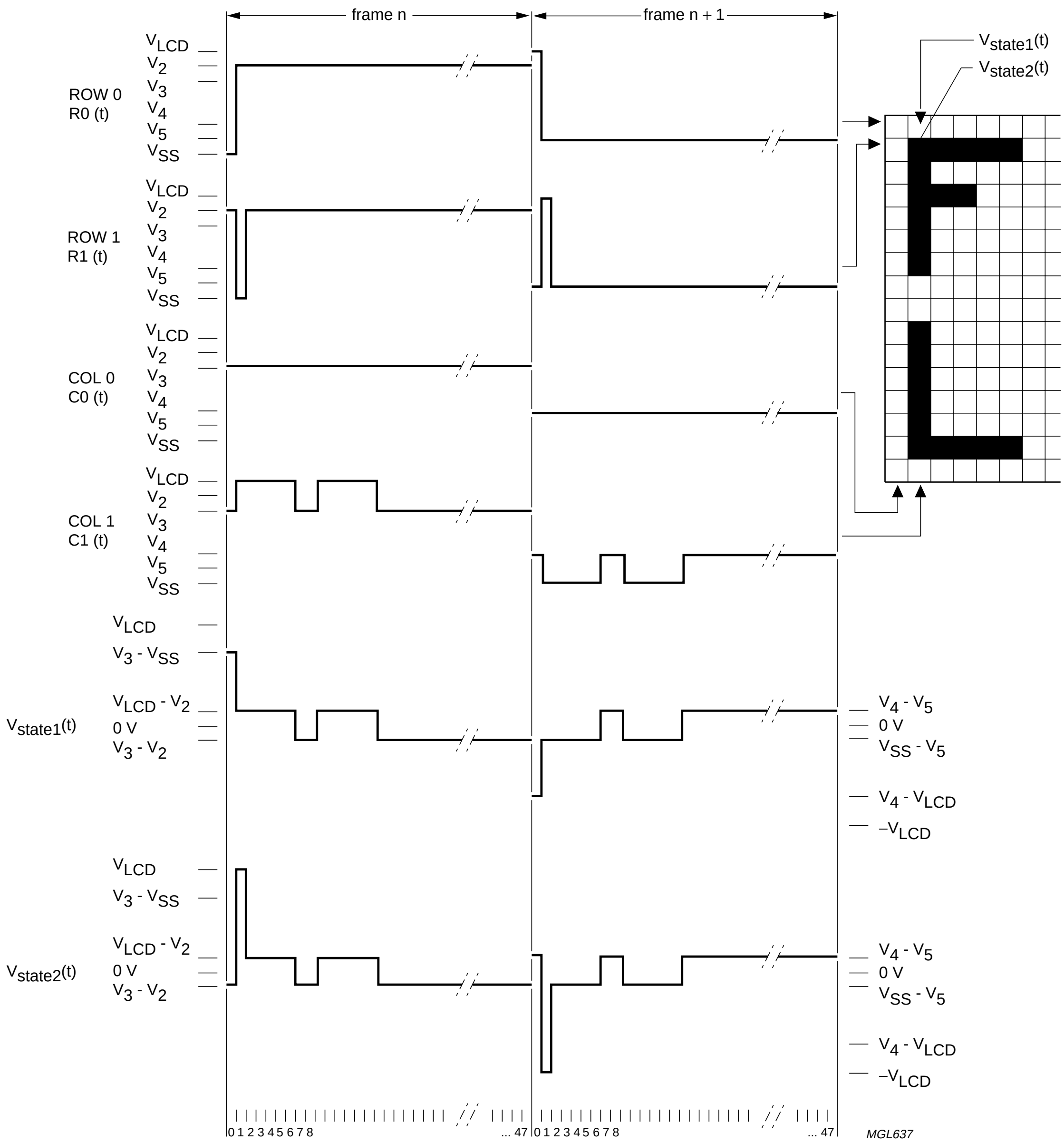
The timing generator produces the various signals required to drive the internal circuits. Internal chip operation is not affected by operations on the data buses.

### 7.5 Display address counter

The display is generated by continuously shifting rows of RAM data to the dot matrix LCD through the column outputs. The display status (all dots on/off and normal/inverse video) is set by bits E and D in the 'display control' command.

### 7.6 LCD row and column drivers

The PCD8544 contains 48 row and 84 column drivers, which connect the appropriate LCD bias voltages in sequence to the display in accordance with the data to be displayed. Figure 2 shows typical waveforms. Unused outputs should be left unconnected.




$V_{state1}(t) = C1(t) - R0(t)$.
$V_{state2}(t) = C1(t) - R1(t)$.

Fig.2 Typical LCD driver waveforms.

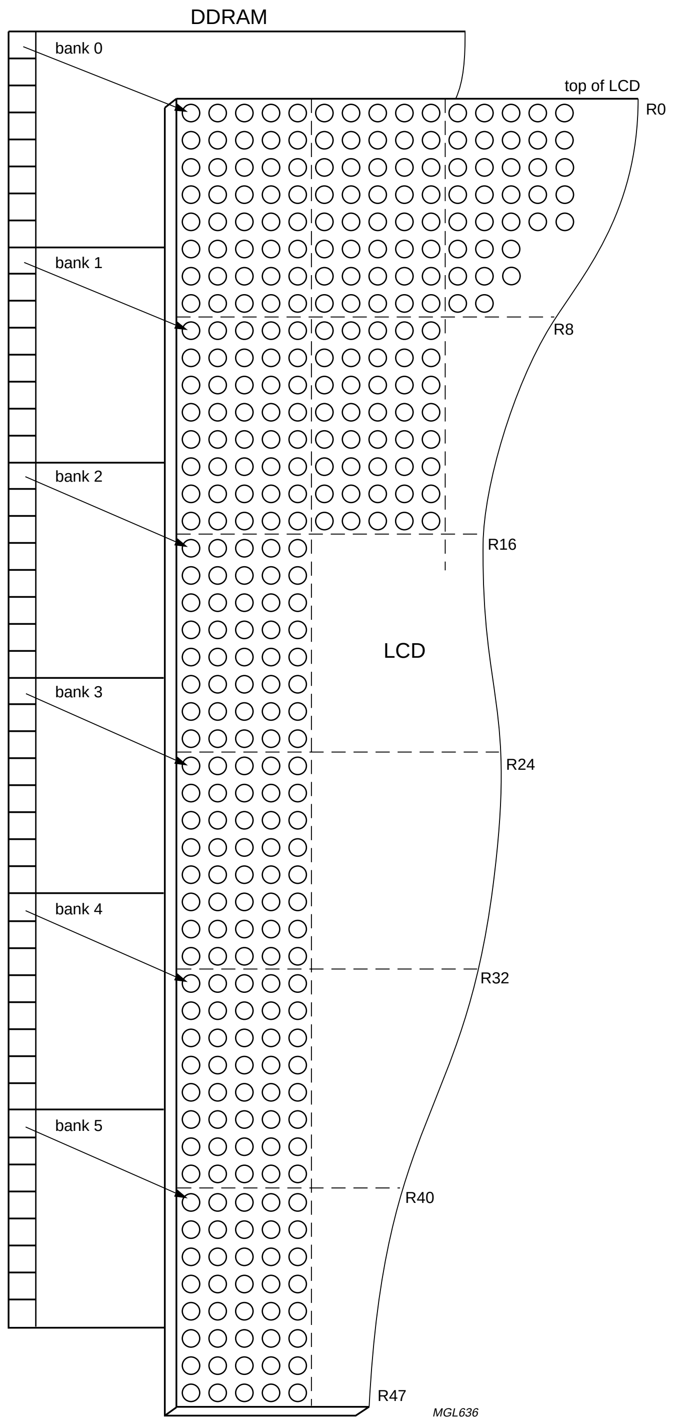



Fig.3 DDRAM to display mapping.

### 7.7 Addressing

Data is downloaded in bytes into the 48 by 84 bits RAM data display matrix of PCD8544, as indicated in Figs. 3, 4, 5 and 6. The columns are addressed by the address pointer. The address ranges are: X 0 to 83 (1010011), Y 0 to 5 (101). Addresses outside these ranges are not allowed. In the vertical addressing mode (V = 1), the Y address increments after each byte (see Fig.5). After the last Y address (Y = 5), Y wraps around to 0 and X increments to address the next column. In the horizontal addressing mode (V = 0), the X address increments after each byte (see Fig.6). After the last X address (X = 83), X wraps around to 0 and Y increments to address the next row. After the very last address (X = 83 and Y = 5), the address pointers wrap around to address (X = 0 and Y = 0).

#### 7.7.1 DATA STRUCTURE

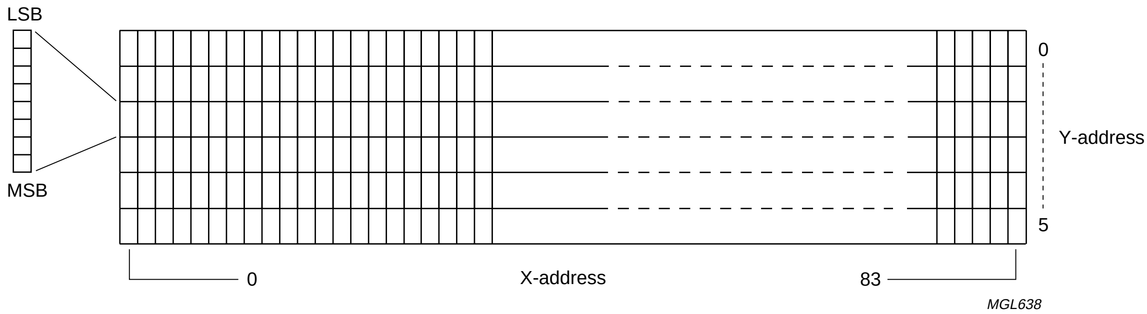



Fig.4 RAM format, addressing.

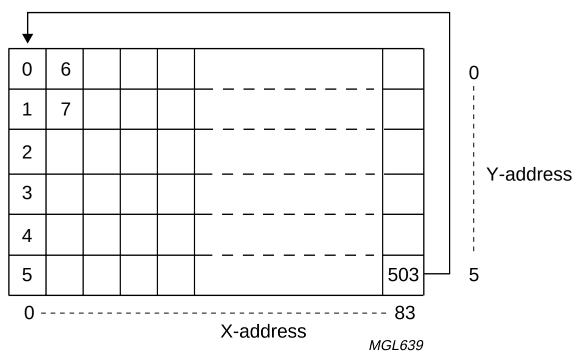



Fig.5 Sequence of writing data bytes into RAM with vertical addressing (V = 1).

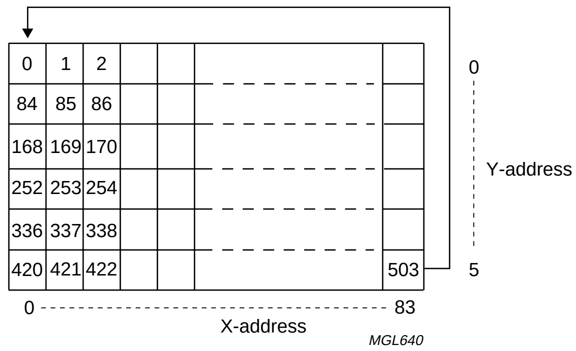
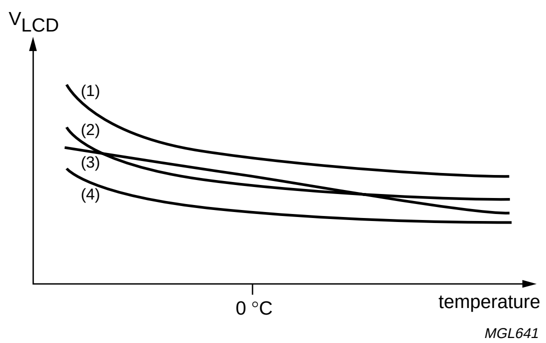



Fig.6 Sequence of writing data bytes into RAM with horizontal addressing (V = 0).

### 7.8 Temperature compensation

Due to the temperature dependency of the liquid crystals' viscosity, the LCD controlling voltage $V_{LCD}$ must be increased at lower temperatures to maintain optimum contrast. Figure 7 shows $V_{LCD}$ for high multiplex rates. In the PCD8544, the temperature coefficient of $V_{LCD}$, can be selected from four values (see Table 2) by setting bits $TC_1$ and $TC_0$.




(1) Upper limit.
(2) Typical curve.
(3) Temperature coefficient of IC.
(4) Lower limit.

Fig.7 $V_{LCD}$ as function of liquid crystal temperature (typical values).

## 8 INSTRUCTIONS

The instruction format is divided into two modes: If $D/\overline{C}$ (mode select) is set LOW, the current byte is interpreted as command byte (see Table 1). Figure 8 shows an example of a serial data stream for initializing the chip. If $D/\overline{C}$ is set HIGH, the following bytes are stored in the display data RAM. After every data byte, the address counter is incremented automatically.

The level of the $D/\overline{C}$ signal is read during the last bit of data byte.

Each instruction can be sent in any order to the PCD8544. The MSB of a byte is transmitted first. Figure 9 shows one possible command stream, used to set up the LCD driver.

The serial interface is initialized when $\overline{SCE}$ is HIGH. In this state, SCLK clock pulses have no effect and no power is consumed by the serial interface. A negative edge on $\overline{SCE}$ enables the serial interface and indicates the start of a data transmission.

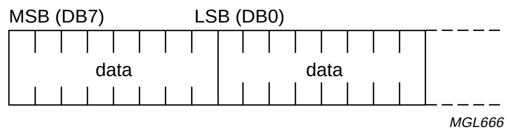



Fig.8 General format of data stream.

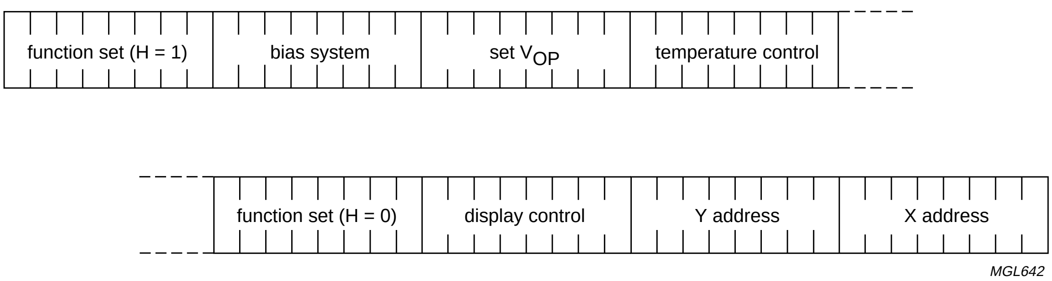



Fig.9 Serial data stream, example.

Figures 10 and 11 show the serial bus protocol.

- When $\overline{SCE}$ is HIGH, SCLK clock signals are ignored; during the HIGH time of $\overline{SCE}$, the serial interface is initialized (see Fig.12)
- SDIN is sampled at the positive edge of SCLK
- $D/\overline{C}$ indicates whether the byte is a command ($D/\overline{C}$ = 0) or RAM data ($D/\overline{C}$ = 1); it is read with the eighth SCLK pulse
- If $\overline{SCE}$ stays LOW after the last bit of a command/data byte, the serial interface expects bit 7 of the next byte at the next positive edge of SCLK (see Fig.12)
- A reset pulse with $\overline{RES}$ interrupts the transmission. No data is written into the RAM. The registers are cleared. If $\overline{SCE}$ is LOW after the positive edge of $\overline{RES}$, the serial interface is ready to receive bit 7 of a command/data byte (see Fig.13).

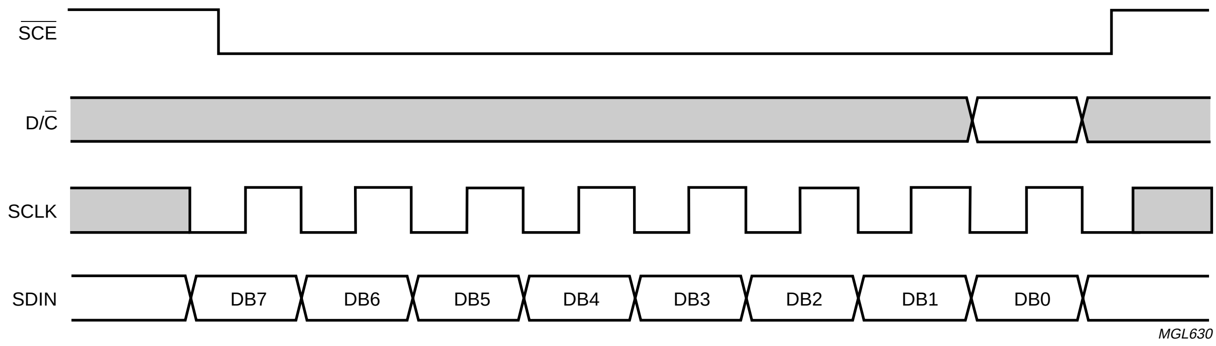



Fig.10 Serial bus protocol - transmission of one byte.

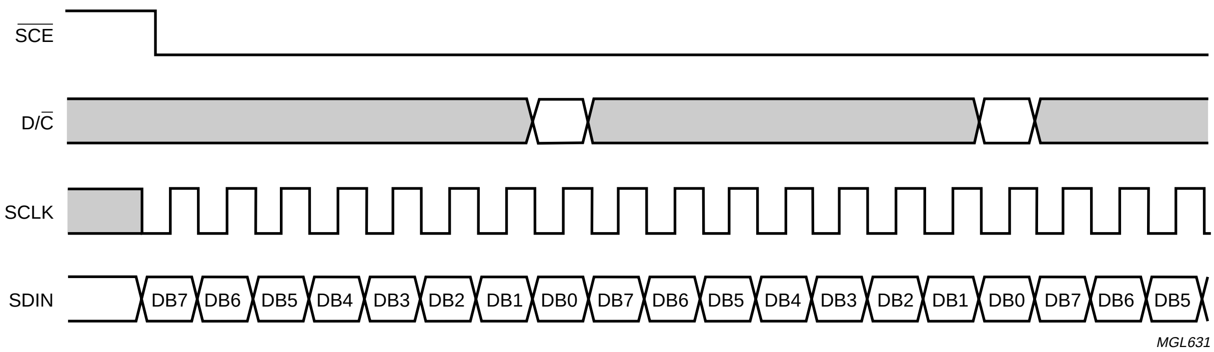



Fig.11 Serial bus protocol - transmission of several bytes.

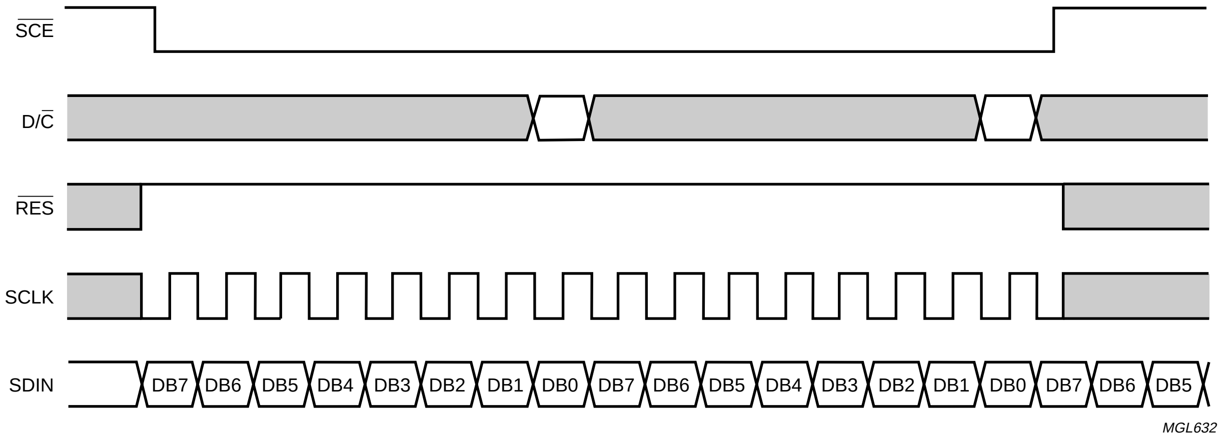



Fig.12 Serial bus reset function ($\overline{\text{SCE}}$).

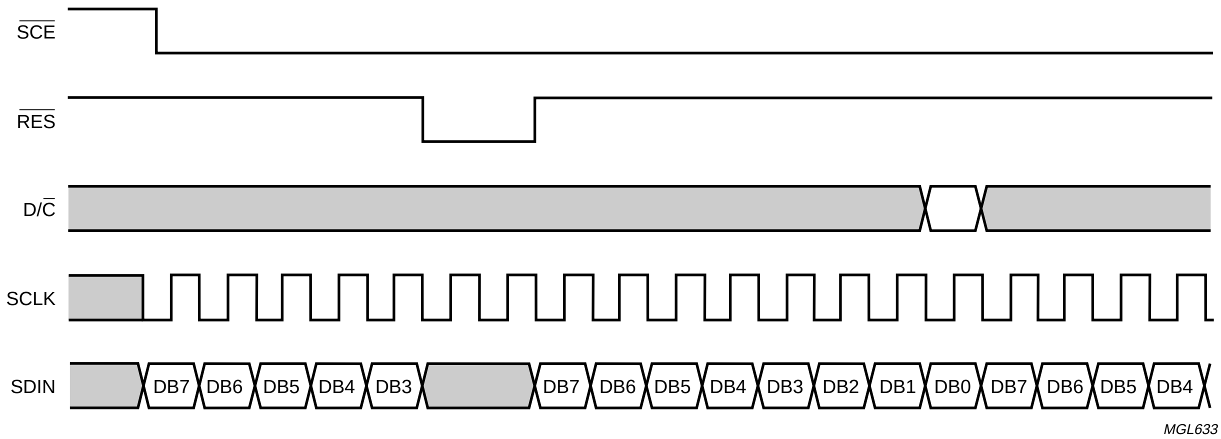



Fig.13 Serial bus reset function ($\overline{\text{RES}}$).

**Table 1** Instruction set

| INSTRUCTION | D/$\overline{C}$ | COMMAND BYTE | | | | | | | | DESCRIPTION |
|---|---|---|---|---|---|---|---|---|---|---|
| | | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 | |
| **(H = 0 or 1)** | | | | | | | | | | |
| NOP | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | no operation |
| Function set | 0 | 0 | 0 | 1 | 0 | 0 | PD | V | H | power down control; entry mode; extended instruction set control (H) |
| Write data | 1 | $D_7$ | $D_6$ | $D_5$ | $D_4$ | $D_3$ | $D_2$ | $D_1$ | $D_0$ | writes data to display RAM |
| **(H = 0)** | | | | | | | | | | |
| Reserved | 0 | 0 | 0 | 0 | 0 | 0 | 1 | X | X | do not use |
| Display control | 0 | 0 | 0 | 0 | 0 | 1 | D | 0 | E | sets display configuration |
| Reserved | 0 | 0 | 0 | 0 | 1 | X | X | X | X | do not use |
| Set Y address of RAM | 0 | 0 | 1 | 0 | 0 | 0 | $Y_2$ | $Y_1$ | $Y_0$ | sets Y-address of RAM; $0 \leq Y \leq 5$ |
| Set X address of RAM | 0 | 1 | $X_6$ | $X_5$ | $X_4$ | $X_3$ | $X_2$ | $X_1$ | $X_0$ | sets X-address part of RAM; $0 \leq X \leq 83$ |
| **(H = 1)** | | | | | | | | | | |
| Reserved | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | do not use |
| | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | X | do not use |
| Temperature control | 0 | 0 | 0 | 0 | 0 | 0 | 1 | $TC_1$ | $TC_0$ | set Temperature Coefficient ($TC_x$) |
| Reserved | 0 | 0 | 0 | 0 | 0 | 1 | X | X | X | do not use |
| Bias system | 0 | 0 | 0 | 0 | 1 | 0 | $BS_2$ | $BS_1$ | $BS_0$ | set Bias System ($BS_x$) |
| Reserved | 0 | 0 | 1 | X | X | X | X | X | X | do not use |
| Set $V_{OP}$ | 0 | 1 | $V_{OP6}$ | $V_{OP5}$ | $V_{OP4}$ | $V_{OP3}$ | $V_{OP2}$ | $V_{OP1}$ | $V_{OP0}$ | write $V_{OP}$ to register |

**Table 2** Explanations of symbols in Table 1

| BIT | 0 | 1 |
|---|---|---|
| PD | chip is active | chip is in Power-down mode |
| V | horizontal addressing | vertical addressing |
| H | use basic instruction set | use extended instruction set |
| D and E | | |
| 00 | display blank | |
| 10 | normal mode | |
| 01 | all display segments on | |
| 11 | inverse video mode | |
| $TC_1$ and $TC_0$ | | |
| 00 | $V_{LCD}$ temperature coefficient 0 | |
| 01 | $V_{LCD}$ temperature coefficient 1 | |
| 10 | $V_{LCD}$ temperature coefficient 2 | |
| 11 | $V_{LCD}$ temperature coefficient 3 | |

### 8.1 Initialization

Immediately following power-on, the contents of all internal registers and of the RAM are undefined. **A $\overline{\text{RES}}$ pulse must be applied**. Attention should be paid to the possibility that the **device may be damaged** if not properly reset.

All internal registers are reset by applying an external $\overline{\text{RES}}$ pulse (active LOW) at pad 31, within the specified time. However, the RAM contents are still undefined. The state after reset is described in Section 8.2.

The $\overline{\text{RES}}$ input must be $\leq 0.3V_{DD}$ when $V_{DD}$ reaches $V_{DDmin}$ (or higher) within a maximum time of 100 ms after $V_{DD}$ goes HIGH (see Fig.16).

### 8.2 Reset function

After reset, the LCD driver has the following state:

- Power-down mode (bit PD = 1)
- Horizontal addressing (bit V = 0) normal instruction set (bit H = 0)
- Display blank (bit E = D = 0)
- Address counter $X_6$ to $X_0$ = 0; $Y_2$ to $Y_0$ = 0
- Temperature control mode ($TC_1$ $TC_0$ = 0)
- Bias system ($BS_2$ to $BS_0$ = 0)
- $V_{LCD}$ is equal to 0, the HV generator is switched off ($V_{OP6}$ to $V_{OP0}$ = 0)
- After power-on, the RAM contents are undefined.

### 8.3 Function set

#### 8.3.1 BIT PD

- All LCD outputs at $V_{SS}$ (display off)
- Bias generator and $V_{LCD}$ generator off, $V_{LCD}$ can be disconnected
- Oscillator off (external clock possible)
- Serial bus, command, etc. function
- Before entering Power-down mode, the RAM needs to be filled with ‘0’s to ensure the specified current consumption.

#### 8.3.2 BIT V

When V = 0, the horizontal addressing is selected. The data is written into the DDRAM as shown in Fig.6. When V = 1, the vertical addressing is selected. The data is written into the DDRAM, as shown in Fig.5.

#### 8.3.3 BIT H

When H = 0 the commands ‘display control’, ‘set Y address’ and ‘set X address’ can be performed; when H = 1, the others can be executed. The ‘write data’ and ‘function set’ commands can be executed in both cases.

### 8.4 Display control

#### 8.4.1 BITS D AND E

Bits D and E select the display mode (see Table 2).

### 8.5 Set Y address of RAM

$Y_n$ defines the Y vector addressing of the display RAM.

**Table 3** Y vector addressing

| $Y_2$ | $Y_1$ | $Y_0$ | BANK |
|---|---|---|---|
| 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 1 |
| 0 | 1 | 0 | 2 |
| 0 | 1 | 1 | 3 |
| 1 | 0 | 0 | 4 |
| 1 | 0 | 1 | 5 |

### 8.6 Set X address of RAM

The X address points to the columns. The range of X is 0 to 83 (53H).

### 8.7 Temperature control

The temperature coefficient of $V_{LCD}$ is selected by bits $TC_1$ and $TC_0$.

### 8.8 Bias value

The bias voltage levels are set in the ratio of R - R - nR - R - R, giving a 1/(n + 4) bias system. Different multiplex rates require different factors n (see Table 4). This is programmed by $BS_2$ to $BS_0$. For Mux 1 : 48, the optimum bias value n, resulting in 1/8 bias, is given by:

$$n = \sqrt{48} - 3 = 3.928 = 4 \quad (1)$$

**Table 4** Programming the required bias system

| **$BS_2$** | **$BS_1$** | **$BS_0$** | **n** | **RECOMMENDED MUX RATE** |
|---|---|---|---|---|
| 0 | 0 | 0 | 7 | 1 : 100 |
| 0 | 0 | 1 | 6 | 1 : 80 |
| 0 | 1 | 0 | 5 | 1 : 65/1 : 65 |
| 0 | 1 | 1 | 4 | 1 : 48 |
| 1 | 0 | 0 | 3 | 1 : 40/1 : 34 |
| 1 | 0 | 1 | 2 | 1 : 24 |
| 1 | 1 | 0 | 1 | 1 : 18/1 : 16 |
| 1 | 1 | 1 | 0 | 1 : 10/1 : 9/1 : 8 |

**Table 5** LCD bias voltage

| **SYMBOL** | **BIAS VOLTAGES** | **BIAS VOLTAGE FOR $\frac{1}{8}$ BIAS** |
|---|---|---|
| V1 | $V_{LCD}$ | $V_{LCD}$ |
| V2 | (n + 3)/(n + 4) | $\frac{7}{8} \times V_{LCD}$ |
| V3 | (n + 2)/(n + 4) | $\frac{6}{8} \times V_{LCD}$ |
| V4 | 2/(n + 4) | $\frac{2}{8} \times V_{LCD}$ |
| V5 | 1/(n + 4) | $\frac{1}{8} \times V_{LCD}$ |
| V6 | $V_{SS}$ | $V_{SS}$ |

### 8.9 Set $V_{OP}$ value

The operation voltage $V_{LCD}$ can be set by software. The values are dependent on the liquid crystal selected. $V_{LCD} = a + (V_{OP6}$ to $V_{OP0}) \times b$ [V]. In the PCD8544, a = 3.06 and b = 0.06 giving a program range of 3.00 to 10.68 at room temperature.

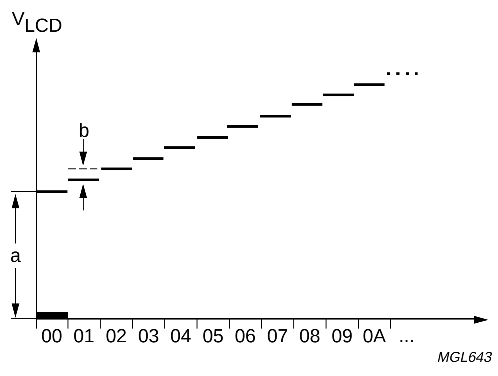
Note that the charge pump is turned off if $V_{OP6}$ to $V_{OP0}$ is set to zero.

For Mux 1 : 48, the optimum operation voltage of the liquid can be calculated as:

$$V_{LCD} = \frac{1 + \sqrt{48}}{\sqrt{2 \cdot \left(1 - \frac{1}{\sqrt{48}}\right)}} \cdot V_{th} = 6.06 \cdot V_{th} \qquad (2)$$

where $V_{th}$ is the threshold voltage of the liquid crystal material used.

**Caution, as $V_{OP}$ increases with lower temperatures, care must be taken not to set a $V_{OP}$ that will exceed the maximum of 8.5 V when operating at –25 °C**.




a = 3.06.
b = 0.06.
$V_{OP6}$ to $V_{OP0}$ (programmed) [00 to 7FH].

Fig.14 $V_{OP}$ programming.

## 9 LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134); see notes 1 and 2.

| SYMBOL | PARAMETER | CONDITIONS | MIN. | MAX. | UNIT |
|---|---|---|---|---|---|
| $V_{DD}$ | supply voltage | note 3 | –0.5 | +7 | V |
| $V_{LCD}$ | supply voltage LCD | note 4 | –0.5 | +10 | V |
| $V_i$ | all input voltages | | –0.5 | $V_{DD}$ + 0.5 | V |
| $I_{SS}$ | ground supply current | | –50 | +50 | mA |
| $I_I$, $I_O$ | DC input or output current | | –10 | +10 | mA |
| $P_{tot}$ | total power dissipation | | – | 300 | mW |
| $P_O$ | power dissipation per output | | – | 30 | mW |
| $T_{amb}$ | operating ambient temperature | | –25 | +70 | °C |
| $T_j$ | operating junction temperature | | –65 | +150 | °C |
| $T_{stg}$ | storage temperature | | –65 | +150 | °C |

**Notes**

1. Stresses above those listed under limiting values may cause permanent damage to the device.
2. Parameters are valid over operating temperature range unless otherwise specified. All voltages are with respect to $V_{SS}$ unless otherwise noted.
3. With external LCD supply voltage externally supplied (voltage generator disabled). $V_{DDmax}$ = 5 V if LCD supply voltage is internally generated (voltage generator enabled).
4. When setting $V_{LCD}$ by software, take care not to set a $V_{OP}$ that will exceed the maximum of 8.5 V when operating at –25 °C, see Caution in Section 8.9.

## 10 HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices (see *"Handling MOS devices"*).

## 11 DC CHARACTERISTICS

$V_{DD}$ = 2.7 to 3.3 V; $V_{SS}$ = 0 V; $V_{LCD}$ = 6.0 to 9.0 V; $T_{amb}$ = –25 to +70 °C; unless otherwise specified.

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| $V_{DD1}$ | supply voltage 1 | LCD voltage externally supplied (voltage generator disabled) | 2.7 | – | 3.3 | V |
| $V_{DD2}$ | supply voltage 2 | LCD voltage internally generated (voltage generator enabled) | 2.7 | – | 3.3 | V |
| $V_{LCD1}$ | LCD supply voltage | LCD voltage externally supplied (voltage generator disabled) | 6.0 | – | 9.0 | V |
| $V_{LCD2}$ | LCD supply voltage | LCD voltage internally generated (voltage generator enabled); note 1 | 6.0 | – | 8.5 | V |
| $I_{DD1}$ | supply current 1 (normal mode) for internal $V_{LCD}$ | $V_{DD}$ = 2.85 V; $V_{LCD}$ = 7.0 V; $f_{SCLK}$ = 0; $T_{amb}$ = 25 °C; display load = 10 µA; note 2 | – | 240 | 300 | µA |
| $I_{DD2}$ | supply current 2 (normal mode) for internal $V_{LCD}$ | $V_{DD}$ = 2.70 V; $V_{LCD}$ = 7.0 V; $f_{SCLK}$ = 0; $T_{amb}$ = 25 °C; display load = 10 µA; note 2 | – | – | 320 | µA |
| $I_{DD3}$ | supply current 3 (Power-down mode) | with internal or external LCD supply voltage; note 3 | – | 1.5 | – | µA |
| $I_{DD4}$ | supply current external $V_{LCD}$ | $V_{DD}$ = 2.85 V; $V_{LCD}$ = 9.0 V; $f_{SCLK}$ = 0; notes 2 and 4 | – | 25 | – | µA |
| $I_{LCD}$ | supply current external $V_{LCD}$ | $V_{DD}$ = 2.7 V; $V_{LCD}$ = 7.0 V; $f_{SCLK}$ = 0; T = 25 °C; display load = 10 µA; notes 2 and 4 | – | 42 | – | µA |
| **Logic** | | | | | | |
| $V_{IL}$ | LOW level input voltage | | $V_{SS}$ | – | $0.3V_{DD}$ | V |
| $V_{IH}$ | HIGH level input voltage | | $0.7V_{DD}$ | – | $V_{DD}$ | V |
| $I_L$ | leakage current | $V_I = V_{DD}$ or $V_{SS}$ | –1 | – | +1 | µA |
| **Column and row outputs** | | | | | | |
| $R_{o(C)}$ | column output resistance C0 to C83 | | – | 12 | 20 | kΩ |
| $R_{o(R)}$ | row output resistance R0 to R47 | | – | 12 | 20 | kΩ |
| $V_{bias(tol)}$ | bias voltage tolerance on C0 to C83 and R0 to R47 | | –100 | 0 | +100 | mV |

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| **LCD supply voltage generator** | | | | | | |
| $V_{LCD}$ | $V_{LCD}$ tolerance internally generated | $V_{DD}$ = 2.85 V; $V_{LCD}$ = 7.0 V; $f_{SCLK}$ = 0; display load = 10 μA; note 5 | – | 0 | 300 | mV |
| TC0 | $V_{LCD}$ temperature coefficient 0 | $V_{DD}$ = 2.85 V; $V_{LCD}$ = 7.0 V; $f_{SCLK}$ = 0; display load = 10 μA | – | 1 | – | mV/K |
| TC1 | $V_{LCD}$ temperature coefficient 1 | $V_{DD}$ = 2.85 V; $V_{LCD}$ = 7.0 V; $f_{SCLK}$ = 0; display load = 10 μA | – | 9 | – | mV/K |
| TC2 | $V_{LCD}$ temperature coefficient 2 | $V_{DD}$ = 2.85 V; $V_{LCD}$ = 7.0 V; $f_{SCLK}$ = 0; display load = 10 μA | – | 17 | – | mV/K |
| TC3 | $V_{LCD}$ temperature coefficient 3 | $V_{DD}$ = 2.85 V; $V_{LCD}$ = 7.0 V; $f_{SCLK}$ = 0; display load = 10 μA | – | 24 | – | mV/K |

**Notes**

1. The maximum possible $V_{LCD}$ voltage that may be generated is dependent on voltage, temperature and (display) load.
2. Internal clock.
3. RAM contents equal ‘0’. During power-down, all static currents are switched off.
4. If external $V_{LCD}$, the display load current is not transmitted to $I_{DD}$.
5. Tolerance depends on the temperature (typically zero at 27 °C, maximum tolerance values are measured at the temperate range limit).

## 12 AC CHARACTERISTICS

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| $f_{OSC}$ | oscillator frequency | | 20 | 34 | 65 | kHz |
| $f_{clk(ext)}$ | external clock frequency | | 10 | 32 | 100 | kHz |
| $f_{frame}$ | frame frequency | $f_{OSC}$ or $f_{clk(ext)}$ = 32 kHz; note 1 | – | 67 | – | Hz |
| $t_{VHRL}$ | $V_{DD}$ to $\overline{RES}$ LOW | Fig.16 | 0(2) | – | 30 | ms |
| $t_{WL(RES)}$ | $\overline{RES}$ LOW pulse width | Fig.16 | 100 | – | – | ns |
| **Serial bus timing characteristics** | | | | | | |
| $f_{SCLK}$ | clock frequency | $V_{DD}$ = 3.0 V ±10% | 0 | – | 4.00 | MHz |
| $T_{cy}$ | clock cycle SCLK | All signal timing is based on 20% to 80% of $V_{DD}$ and maximum rise and fall times of 10 ns | 250 | – | – | ns |
| $t_{WH1}$ | SCLK pulse width HIGH | | 100 | – | – | ns |
| $t_{WL1}$ | SCLK pulse width LOW | | 100 | – | – | ns |
| $t_{su2}$ | $\overline{SCE}$ set-up time | | 60 | – | – | ns |
| $t_{h2}$ | $\overline{SCE}$ hold time | | 100 | – | – | ns |
| $t_{WH2}$ | $\overline{SCE}$ min. HIGH time | | 100 | – | – | ns |
| $t_{h5}$ | $\overline{SCE}$ start hold time; note 3 | | 100 | – | – | ns |
| $t_{su3}$ | D/$\overline{C}$ set-up time | | 100 | – | – | ns |
| $t_{h3}$ | D/$\overline{C}$ hold time | | 100 | – | – | ns |
| $t_{su4}$ | SDIN set-up time | | 100 | – | – | ns |
| $t_{h4}$ | SDIN hold time | | 100 | – | – | ns |

### Notes

1. $T_{frame} = \frac{f_{clk(ext)}}{480}$
2. $\overline{RES}$ may be LOW before $V_{DD}$ goes HIGH.
3. $t_{h5}$ is the time from the previous SCLK positive edge (irrespective of the state of $\overline{SCE}$) to the negative edge of $\overline{SCE}$ (see Fig.15).

### 12.1 Serial interface

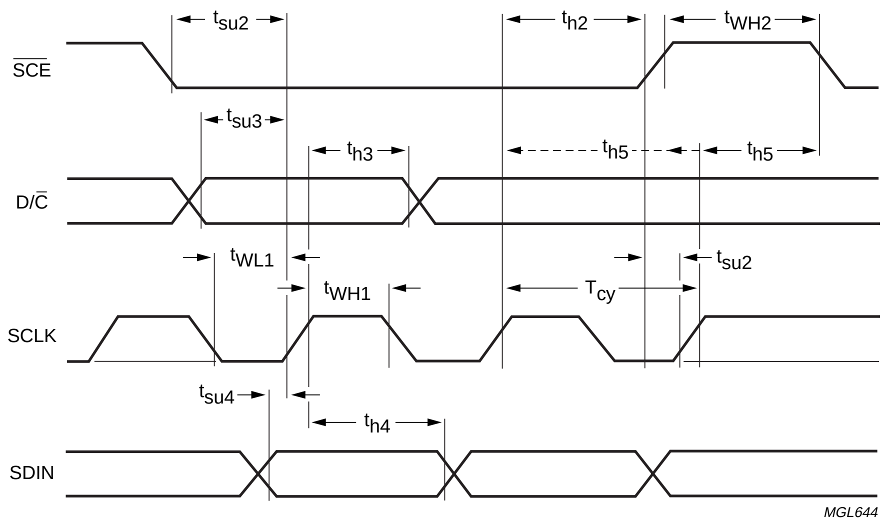



Fig.15 Serial interface timing.

### 12.2 Reset

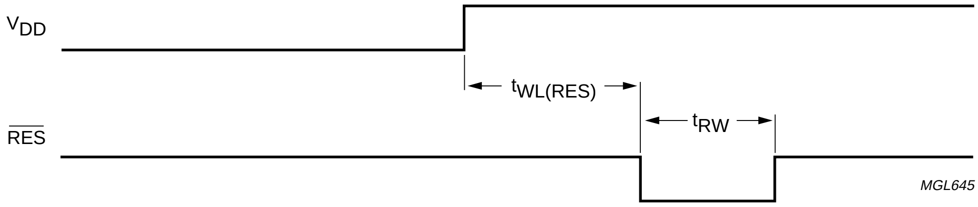
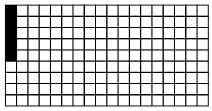
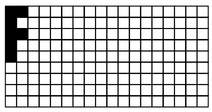
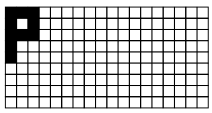
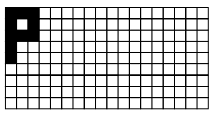
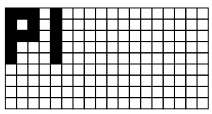
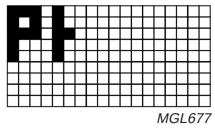
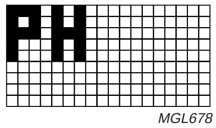
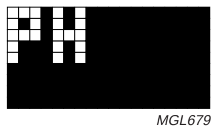
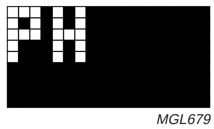
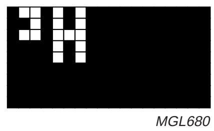



Fig.16 Reset timing.

## 13 APPLICATION INFORMATION

**Table 6** Programming example

| STEP | SERIAL BUS BYTE | | | | | | | | | DISPLAY | OPERATION |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | $D/\overline{C}$ | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 | | |
| 1 | start | | | | | | | | | | $\overline{SCE}$ is going LOW |
| 2 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | | function set<br>PD = 0 and V = 0, select extended instruction set (H = 1 mode) |
| 3 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | | set $V_{OP}$; $V_{OP}$ is set to a +16 × b [V] |
| 4 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | | function set<br>PD = 0 and V = 0, select normal instruction set (H = 0 mode) |
| 5 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | | display control set normal mode (D = 1 and E = 0) |
| 6 | 1 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 |  MGL673 | data write Y and X are initialized to 0 by default, so they are not set here |
| 7 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 |  MGL674 | data write |
| 8 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 |  MGL675 | data write |
| 9 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |  MGL675 | data write |
| 10 | 1 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 |  MGL676 | data write |

| STEP | SERIAL BUS BYTE | | | | | | | | | DISPLAY | OPERATION |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | D/$\overline{C}$ | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 | | |
| 11 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 |  | data write |
| 12 | 1 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 |  | data write |
| 13 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 1 |  | display control; set inverse video mode (D = 1 and E = 1) |
| 14 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |  | set X address of RAM; set address to ‘0000000’ |
| 15 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |  | data write |

The pinning is optimized for single plane wiring e.g. for chip-on-glass display modules. Display size: 48 × 84 pixels.

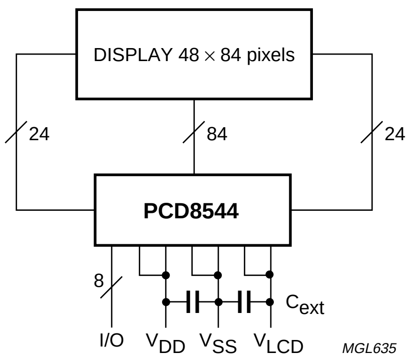



Fig.17 Application diagram.

The required minimum value for the external capacitors is: $C_{ext}$ = 1.0 μF.

Higher capacitor values are recommended for ripple reduction.

## 14 BONDING PAD LOCATIONS

### 14.1 Bonding pad information (see Fig.18)

| PARAMETER | SIZE |
|---|---|
| Pad pitch | min. 100 μm |
| Pad size, aluminium | 80 × 100 μm |
| Bump dimensions | 59 × 89 × 17.5 (±5) μm |
| Wafer thickness | max. 380 μm |

### 14.2 Bonding pad location

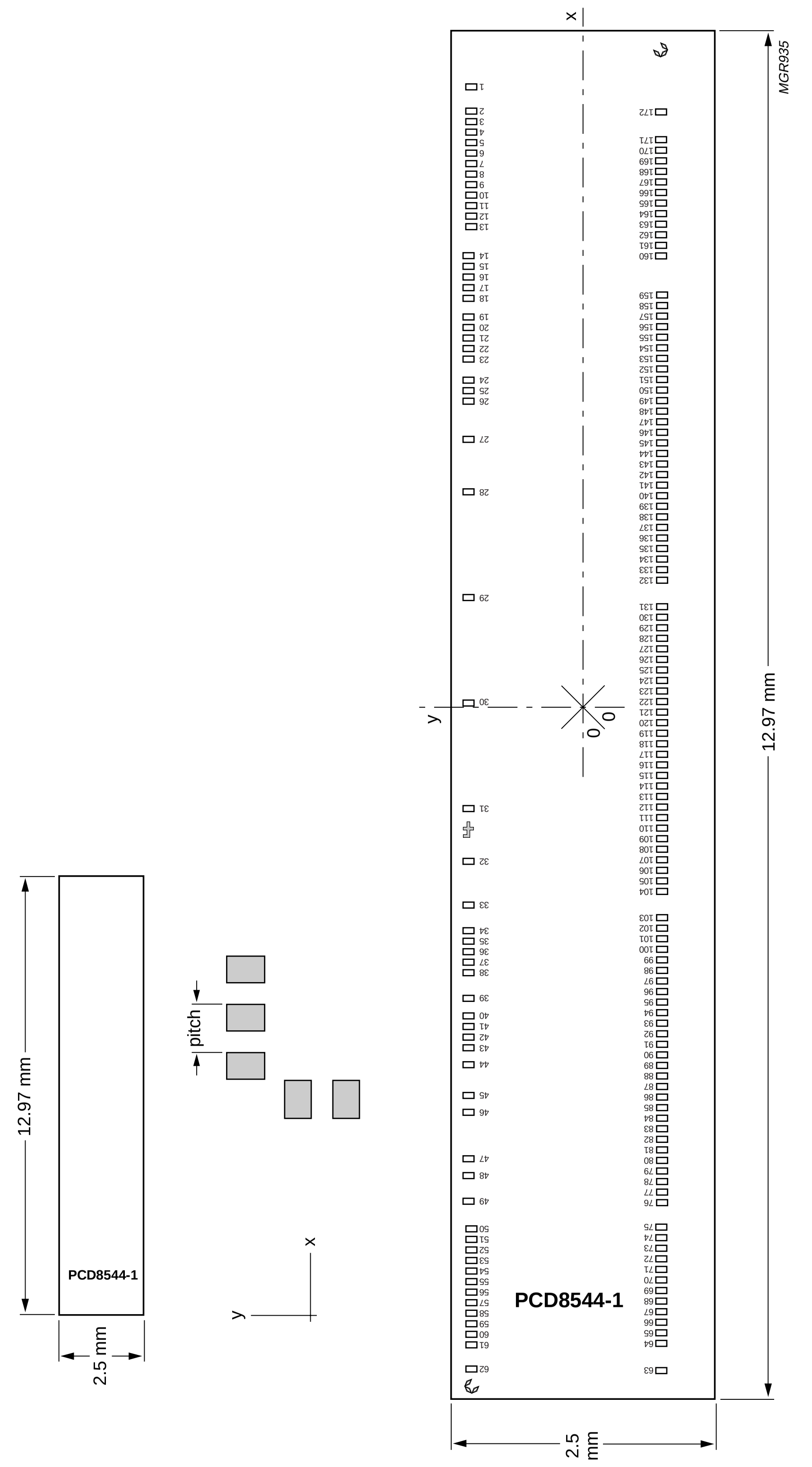



Fig.18 Bonding pad locations.

**Table 7** Bonding pad locations (dimensions in μm). All X/Y coordinates are referenced to the centre of chip (see Fig.18)

| PAD | PAD NAME | x | y |
|---|---|---|---|
| 1 | dummy1 | +5932 | +1060 |
| 2 | R36 | +5704 | +1060 |
| 3 | R37 | +5604 | +1060 |
| 4 | R38 | +5504 | +1060 |
| 5 | R39 | +5404 | +1060 |
| 6 | R40 | +5304 | +1060 |
| 7 | R41 | +5204 | +1060 |
| 8 | R42 | +5104 | +1060 |
| 9 | R43 | +5004 | +1060 |
| 10 | R44 | +4904 | +1060 |
| 11 | R45 | +4804 | +1060 |
| 12 | R46 | +4704 | +1060 |
| 13 | R47 | +4604 | +1060 |
| 14 | $V_{DD1}$ | +4330 | +1085 |
| 15 | $V_{DD1}$ | +4230 | +1085 |
| 16 | $V_{DD1}$ | +4130 | +1085 |
| 17 | $V_{DD1}$ | +4030 | +1085 |
| 18 | $V_{DD1}$ | +3930 | +1085 |
| 19 | $V_{DD2}$ | +3750 | +1085 |
| 20 | $V_{DD2}$ | +3650 | +1085 |
| 21 | $V_{DD2}$ | +3550 | +1085 |
| 22 | $V_{DD2}$ | +3450 | +1085 |
| 23 | $V_{DD2}$ | +3350 | +1085 |
| 24 | $V_{DD2}$ | +3250 | +1085 |
| 25 | $V_{DD2}$ | +3150 | +1085 |
| 26 | $V_{DD2}$ | +3050 | +1085 |
| 27 | SCLK | +2590 | +1085 |
| 28 | SDIN | +2090 | +1085 |
| 29 | $D/\overline{C}$ | +1090 | +1085 |
| 30 | $\overline{SCE}$ | +90 | +1085 |
| 31 | $\overline{RES}$ | –910 | +1085 |
| 32 | OSC | –1410 | +1085 |
| 33 | T3 | –1826 | +1085 |
| 34 | $V_{SS2}$ | –2068 | +1085 |
| 35 | $V_{SS2}$ | –2168 | +1085 |
| 36 | $V_{SS2}$ | –2268 | +1085 |
| 37 | $V_{SS2}$ | –2368 | +1085 |
| 38 | $V_{SS2}$ | –2468 | +1085 |
| 39 | T4 | –2709 | +1085 |
| 40 | $V_{SS1}$ | –2876 | +1085 |
| 41 | $V_{SS1}$ | –2976 | +1085 |
| 42 | $V_{SS1}$ | –3076 | +1085 |
| 43 | $V_{SS1}$ | –3176 | +1085 |
| 44 | T1 | –3337 | +1085 |
| 45 | $V_{LCD2}$ | –3629 | +1085 |
| 46 | $V_{LCD2}$ | –3789 | +1085 |
| 47 | $V_{LCD1}$ | –4231 | +1085 |
| 48 | $V_{LCD1}$ | –4391 | +1085 |
| 49 | T2 | –4633 | +1085 |
| 50 | R23 | –4894 | +1060 |
| 51 | R22 | –4994 | +1060 |
| 52 | R21 | –5094 | +1060 |
| 53 | R20 | –5194 | +1060 |
| 54 | R19 | –5294 | +1060 |
| 55 | R18 | –5394 | +1060 |
| 56 | R17 | –5494 | +1060 |
| 57 | R16 | –5594 | +1060 |
| 58 | R15 | –5694 | +1060 |
| 59 | R14 | –5794 | +1060 |
| 60 | R13 | –5894 | +1060 |
| 61 | R12 | –5994 | +1060 |
| 62 | dummy2 | –6222 | +1060 |
| 63 | dummy3 | –6238 | –738 |
| 64 | R0 | –5979 | –738 |
| 65 | R1 | –5879 | –738 |
| 66 | R2 | –5779 | –738 |
| 67 | R3 | –5679 | –738 |
| 68 | R4 | –5579 | –738 |
| 69 | R5 | –5479 | –738 |
| 70 | R6 | –5379 | –738 |
| 71 | R7 | –5279 | –738 |
| 72 | R8 | –5179 | –738 |
| 73 | R9 | –5079 | –738 |
| 74 | R10 | –4979 | –738 |
| 75 | R11 | –4879 | –738 |
| 76 | C0 | –4646 | –746 |

| PAD | PAD NAME | x | y |
|---|---|---|---|
| 77 | C1 | –4546 | –746 |
| 78 | C2 | –4446 | –746 |
| 79 | C3 | –4346 | –746 |
| 80 | C4 | –4246 | –746 |
| 81 | C5 | –4146 | –746 |
| 82 | C6 | –4046 | –746 |
| 83 | C7 | –3946 | –746 |
| 84 | C8 | –3846 | –746 |
| 85 | C9 | –3746 | –746 |
| 86 | C10 | –3646 | –746 |
| 87 | C11 | –3546 | –746 |
| 88 | C12 | –3446 | –746 |
| 89 | C13 | –3346 | –746 |
| 90 | C14 | –3246 | –746 |
| 91 | C15 | –3146 | –746 |
| 92 | C16 | –3046 | –746 |
| 93 | C17 | –2946 | –746 |
| 94 | C18 | –2846 | –746 |
| 95 | C19 | –2746 | –746 |
| 96 | C20 | –2646 | –746 |
| 97 | C21 | –2546 | –746 |
| 98 | C22 | –2446 | –746 |
| 99 | C23 | –2346 | –746 |
| 100 | C24 | –2246 | –746 |
| 101 | C25 | –2146 | –746 |
| 102 | C26 | –2046 | –746 |
| 103 | C27 | –1946 | –746 |
| 104 | C28 | –1696 | –746 |
| 105 | C29 | –1596 | –746 |
| 106 | C30 | –1496 | –746 |
| 107 | C31 | –1396 | –746 |
| 108 | C32 | –1296 | –746 |
| 109 | C33 | –1196 | –746 |
| 110 | C34 | –1096 | –746 |
| 111 | C35 | –996 | –746 |
| 112 | C36 | –896 | –746 |
| 113 | C37 | –796 | –746 |
| 114 | C38 | –696 | –746 |
| 115 | C39 | –596 | –746 |
| 116 | C40 | –496 | –746 |
| 117 | C41 | –396 | –746 |

| PAD | PAD NAME | x | y |
|---|---|---|---|
| 118 | C42 | –296 | –746 |
| 119 | C43 | –196 | –746 |
| 120 | C44 | –96 | –746 |
| 121 | C45 | +4 | –746 |
| 122 | C46 | +104 | –746 |
| 123 | C47 | +204 | –746 |
| 124 | C48 | +304 | –746 |
| 125 | C49 | +404 | –746 |
| 126 | C50 | +504 | –746 |
| 127 | C51 | +604 | –746 |
| 128 | C52 | +704 | –746 |
| 139 | C53 | +804 | –746 |
| 130 | C54 | +904 | –746 |
| 131 | C55 | +1004 | –746 |
| 132 | C56 | +1254 | –746 |
| 133 | C57 | +1354 | –746 |
| 134 | C58 | +1454 | –746 |
| 135 | C59 | +1554 | –746 |
| 136 | C60 | +1654 | –746 |
| 137 | C61 | +1754 | –746 |
| 138 | C62 | +1854 | –746 |
| 139 | C63 | +1954 | –746 |
| 140 | C64 | +2054 | –746 |
| 141 | C65 | +2154 | –746 |
| 142 | C66 | +2254 | –746 |
| 143 | C67 | +2354 | –746 |
| 144 | C68 | +2454 | –746 |
| 145 | C69 | +2554 | –746 |
| 146 | C70 | +2654 | –746 |
| 147 | C71 | +2754 | –746 |
| 148 | C72 | +2854 | –746 |
| 149 | C73 | +2954 | –746 |
| 150 | C74 | +3054 | –746 |
| 151 | C75 | +3154 | –746 |
| 152 | C76 | +3254 | –746 |
| 153 | C77 | +3354 | –746 |
| 154 | C78 | +3454 | –746 |
| 155 | C79 | +3554 | –746 |
| 156 | C80 | +3654 | –746 |
| 157 | C81 | +3754 | –746 |
| 158 | C82 | +3854 | –746 |

| PAD | PAD NAME | x | y |
|---|---|---|---|
| 159 | C83 | +3954 | –746 |
| 160 | R35 | +4328 | –738 |
| 161 | R34 | +4428 | –738 |
| 162 | R33 | +4528 | –738 |
| 163 | R32 | +4628 | –738 |
| 164 | R31 | +4728 | –738 |
| 165 | R30 | +4828 | –738 |
| 166 | R29 | +4928 | –738 |
| 167 | R28 | +5028 | –738 |
| 168 | R27 | +5128 | –738 |
| 169 | R26 | +5228 | –738 |
| 170 | R25 | +5328 | –738 |
| 171 | R24 | +5428 | –738 |
| 172 | dummy4 | +5694 | –738 |

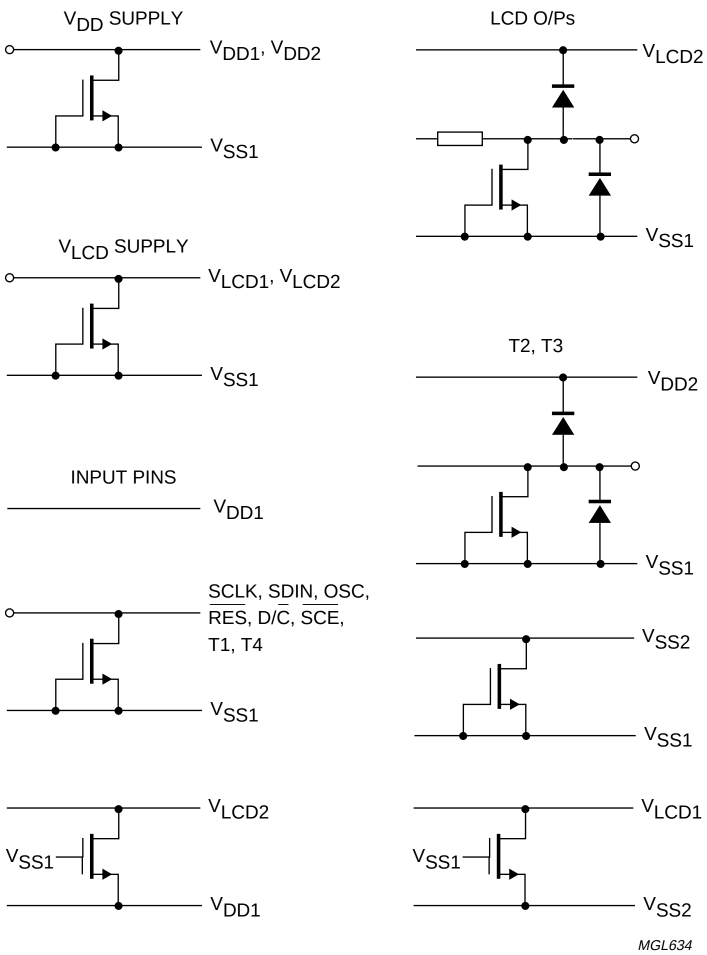
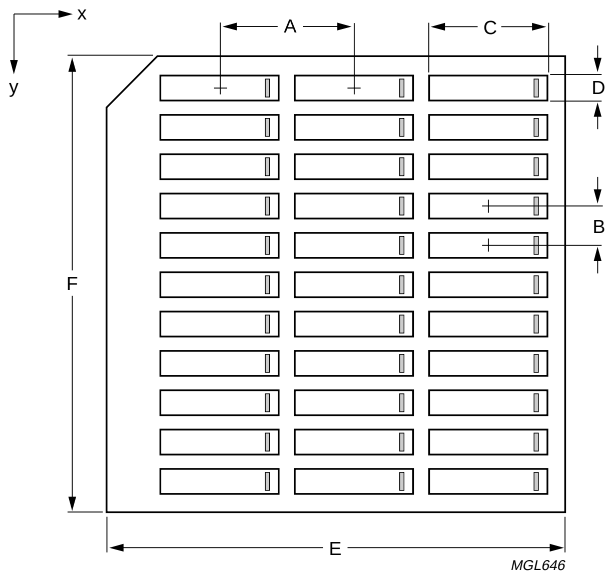


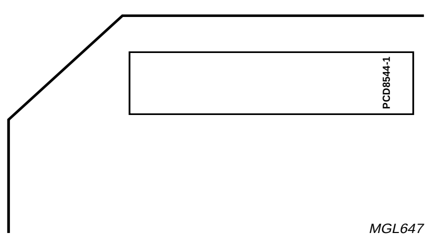

Fig.19 Device protection diagram.

## 15 TRAY INFORMATION




For the dimensions of x, y and A to F, see Table 8.

Fig.20 Tray details.




The orientation of the IC in a pocket is indicated by the position of the IC type name on the die surface with respect to the chamfer on the upper left corner of the tray. Refer to the bonding pad location diagram for the orientation and position of the type name on the die surface.

Fig.21 Tray alignment.

**Table 8** Dimensions

| DIM. | DESCRIPTION | VALUE |
|---|---|---|
| A | pocket pitch, in the x direction | 14.82 mm |
| B | pocket pitch, in the y direction | 4.39 mm |
| C | pocket width, in the x direction | 13.27 mm |
| D | pocket width, in the y direction | 2.8 mm |
| E | tray width, in the x direction | 50.67 mm |
| F | tray width, in the y direction | 50.67 mm |
| x | no. of pockets in the x direction | 3 |
| y | no. of pockets in the y direction | 11 |

## 16 DEFINITIONS

| | |
|---|---|
| **Data sheet status** | |
| Objective specification | This data sheet contains target or goal specifications for product development. |
| Preliminary specification | This data sheet contains preliminary data; supplementary data may be published later. |
| Product specification | This data sheet contains final product specifications. |
| **Limiting values** | |
| Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability. | |
| **Application information** | |
| Where application information is given, it is advisory and does not form part of the specification. | |

## 17 LIFE SUPPORT APPLICATIONS

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips for any damages resulting from such improper use or sale.

## NOTES

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