THE ISLAMIC UNIVERSITY – FACULTY OF ENGINEERING

COMPUTER ENGINEERING DEPARTMENT

LCOM 3010 – Introduction to Computer Architecture Lab

Lab #3
MEMORY DESIGN

BY

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Submitted for

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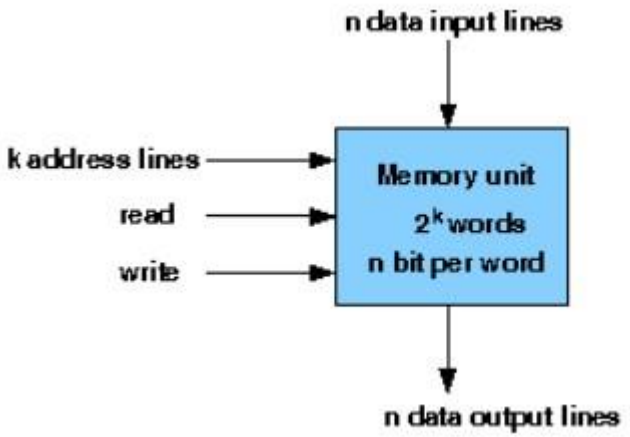
Memory Design

Objective:

1. Understanding behavior of memory from working module and the module designed by the student as part of the experiment.
2. Designing Memory for given parameter

Theory: Design of Memory:

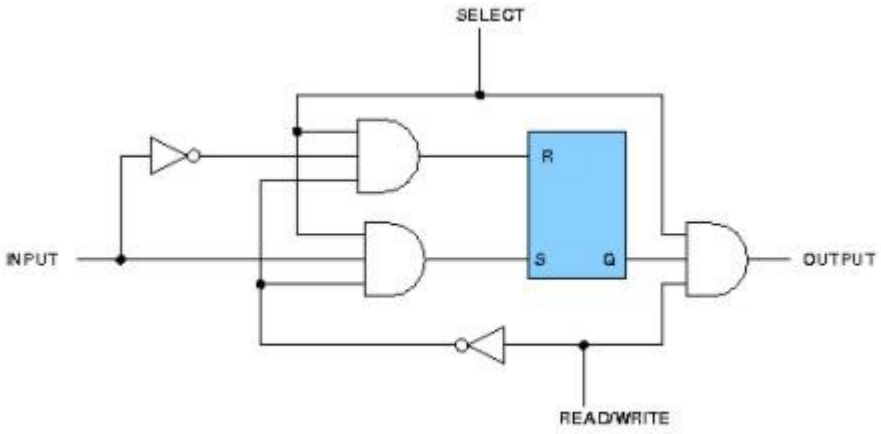
A memory unit is a collection of storage cells together with associated circuits needed to transform information in and out of the device. Memory cells which can be accessed for information transfer to or from any desired random location is called random access memory (RAM). The block diagram of a memory unit-



Internal Construction: The internal construction of a random-access memory of m words with n bits per word consists of m*n binary storage cells and associated decoding circuits for selecting individual words. The binary cell is the basic building block of a memory unit.

Design of a RAM cell:

The binary cell has three inputs and one output. The select input enables the cell for reading or writing and the read/write input determines the cell operation when it is selected. A 1 in the read/write input provides the read operation by forming a path from the flip-flop to the output terminal. A 0 in the read/write input provides the write operation by forming a path from the input terminal to the flip-flop. The logic diagram
is-

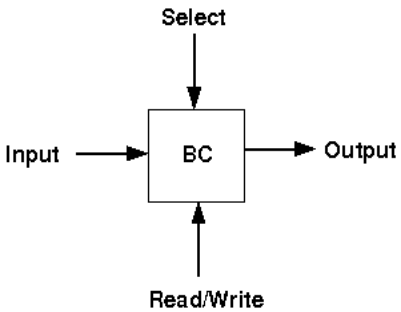


To build a RAM Cell, we need:

- AND Gate (2 input)-6
- NOT Gate-2
- RS Flip Flop-1

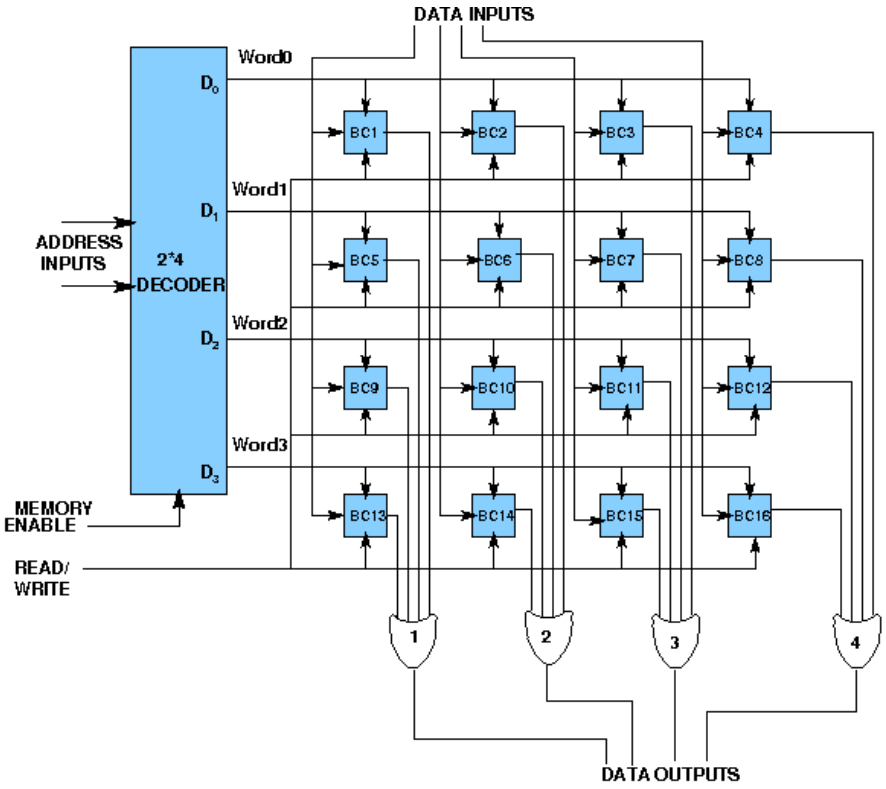
Design of a 4X4 RAM:

The logical construction of a small RAM 4X3 is shown below. It consists of 4 words of 3 bits each and has a total of 12 binary cells. Each block labeled BC represents the binary cell with its 3 inputs and 1 output. The block diagram of a binary cell-



A memory with 4 words needs two address lines. The two address inputs go through a 2*4 decoder to select one of the four words. The decoder is enabled with the memory enable input. When the memory enable is 0, all

outputs of the decoder are 0 and none of the memory words are selected. With the memory enable at 1, one of the four words is selected, dictated by the value in the two address lines. Once a word has been selected, the read/write input determines the operation. The logic diagram is-



To build a 4X3 RAM, we need:

1. OR Gate(2 input)-11
2. RAM Cell-12
3. 2X4 Decoder with Enable-1

Test plan:

1. Do some read operation by properly setting the R/W', memory enable then give input and check the output.
2. Do some write operation by properly setting the R/W', memory enable then give input and check the output.
3. Do some read operation without setting the memory enable but properly setting the R/W' then give input and check the output.

Use Display units for checking output. Try to use minimum number of components to build. The pin configuration of the canned components are shown when mouse hovered over a component.

Assignment Statements:

1. Design a binary RAM cell using an S-R flip-flop, AND gates, NOT gates having select, read/write, input, output and test it by giving proper input.
2. Design a 4X3 RAM memory which will have 4 words each of 3 bits using binary RAM cells, decoder with enable, OR gates and test it by giving proper input.