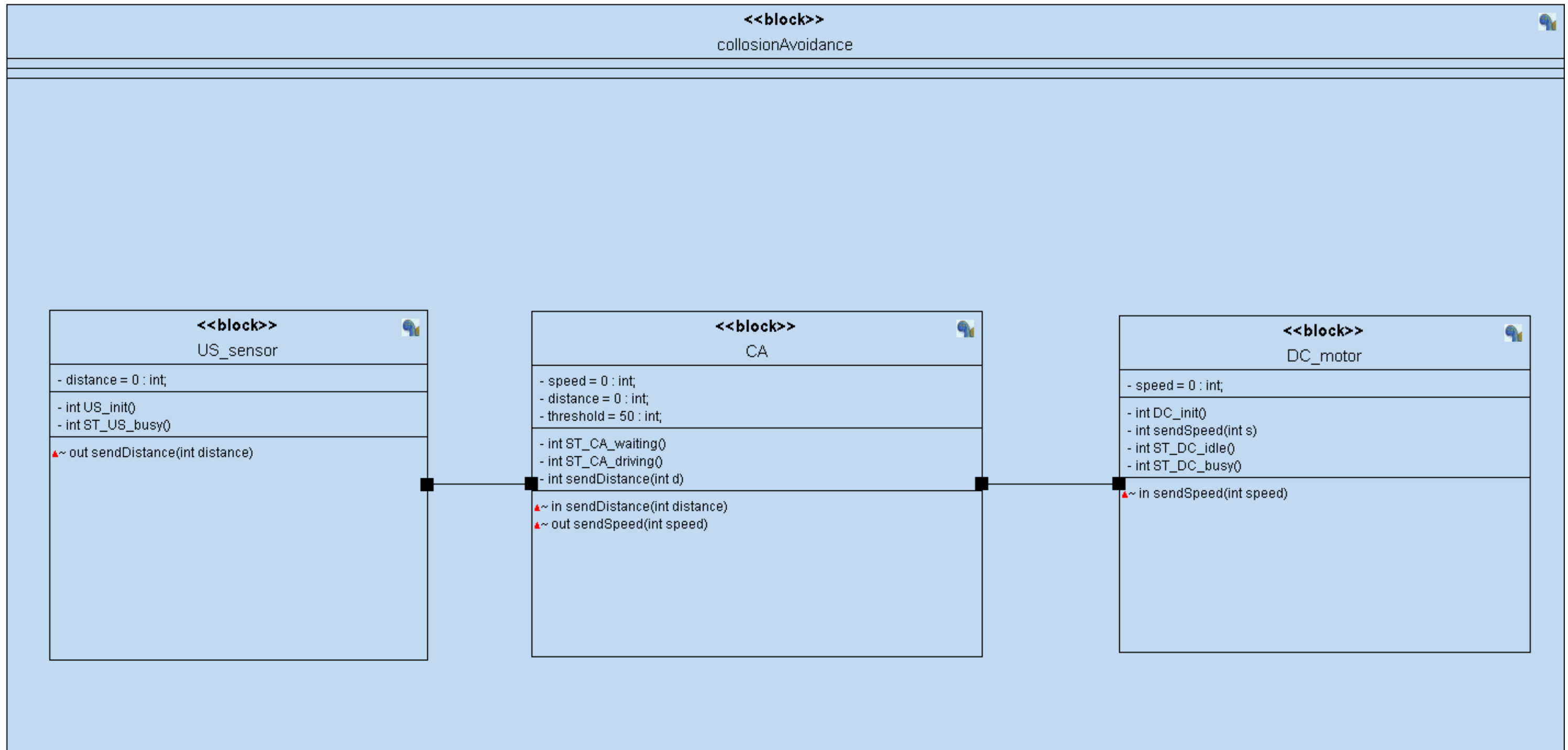
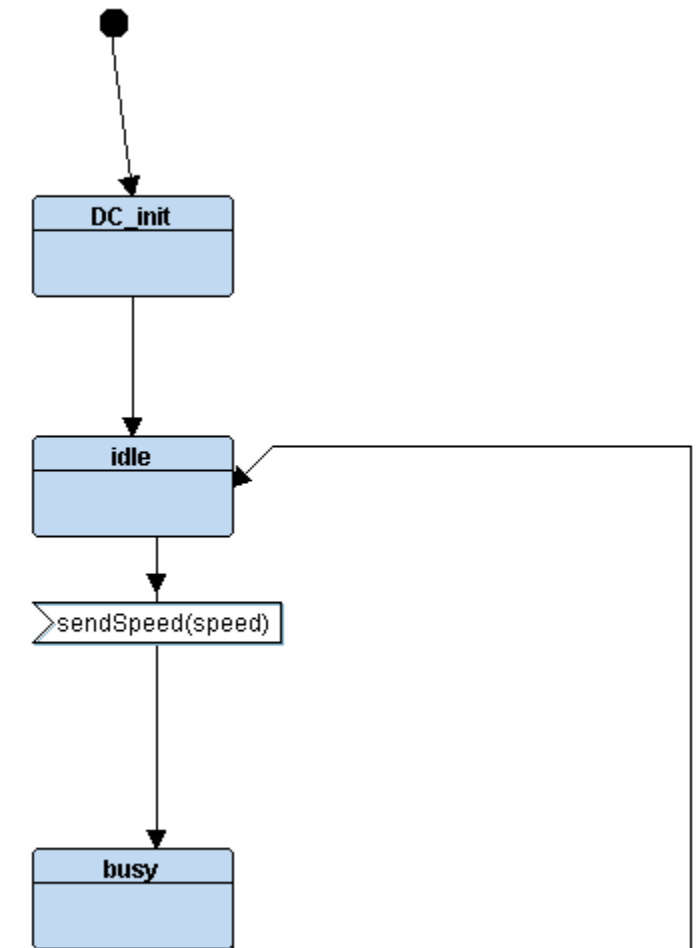
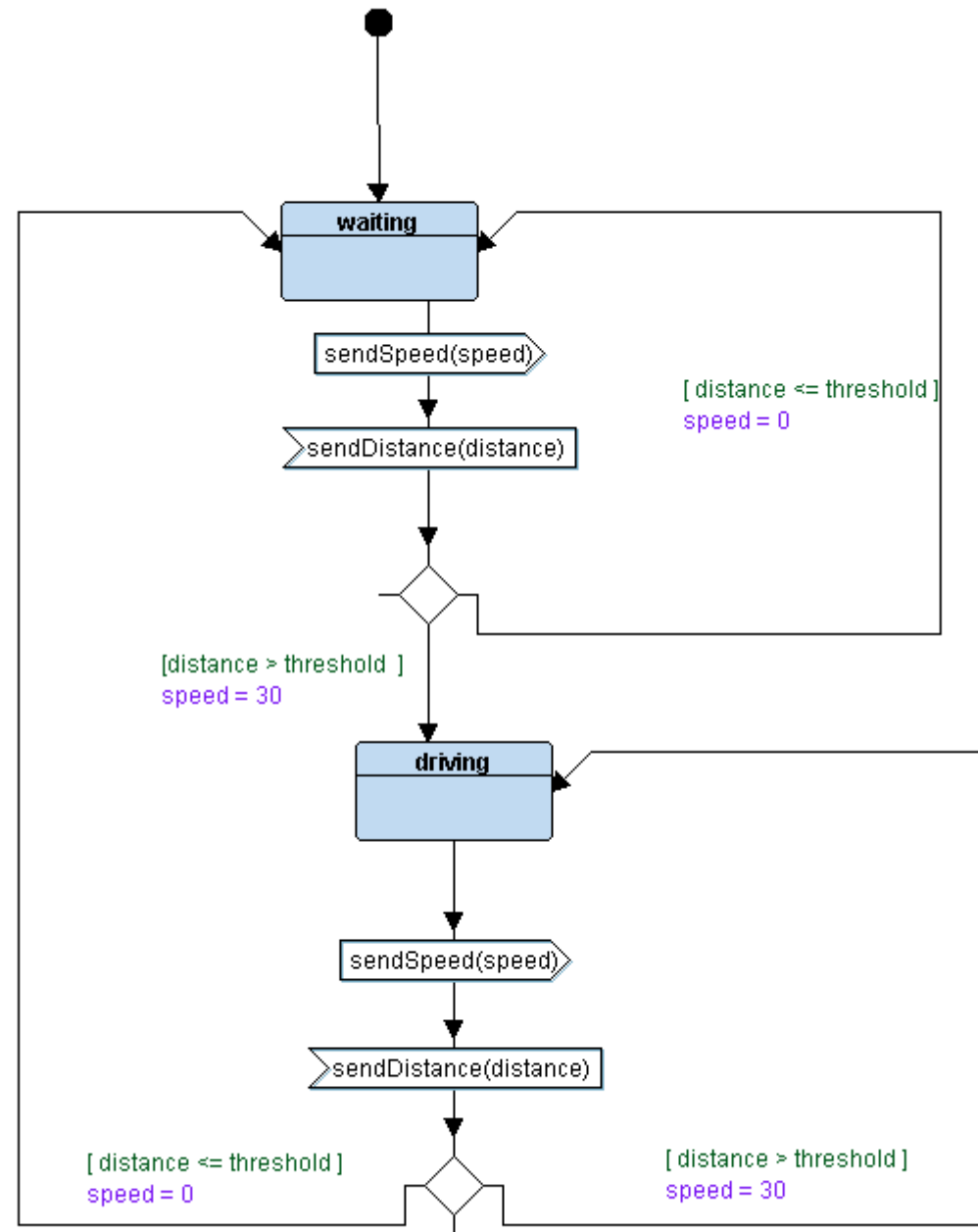
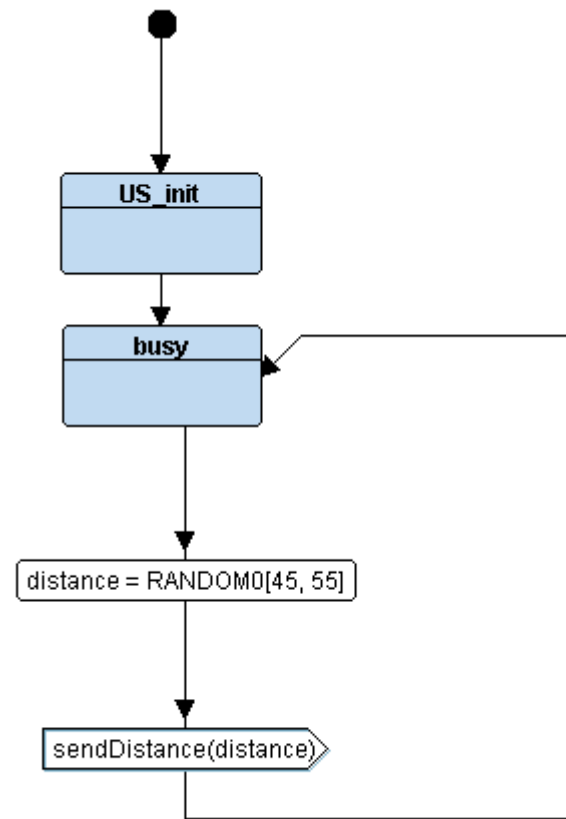


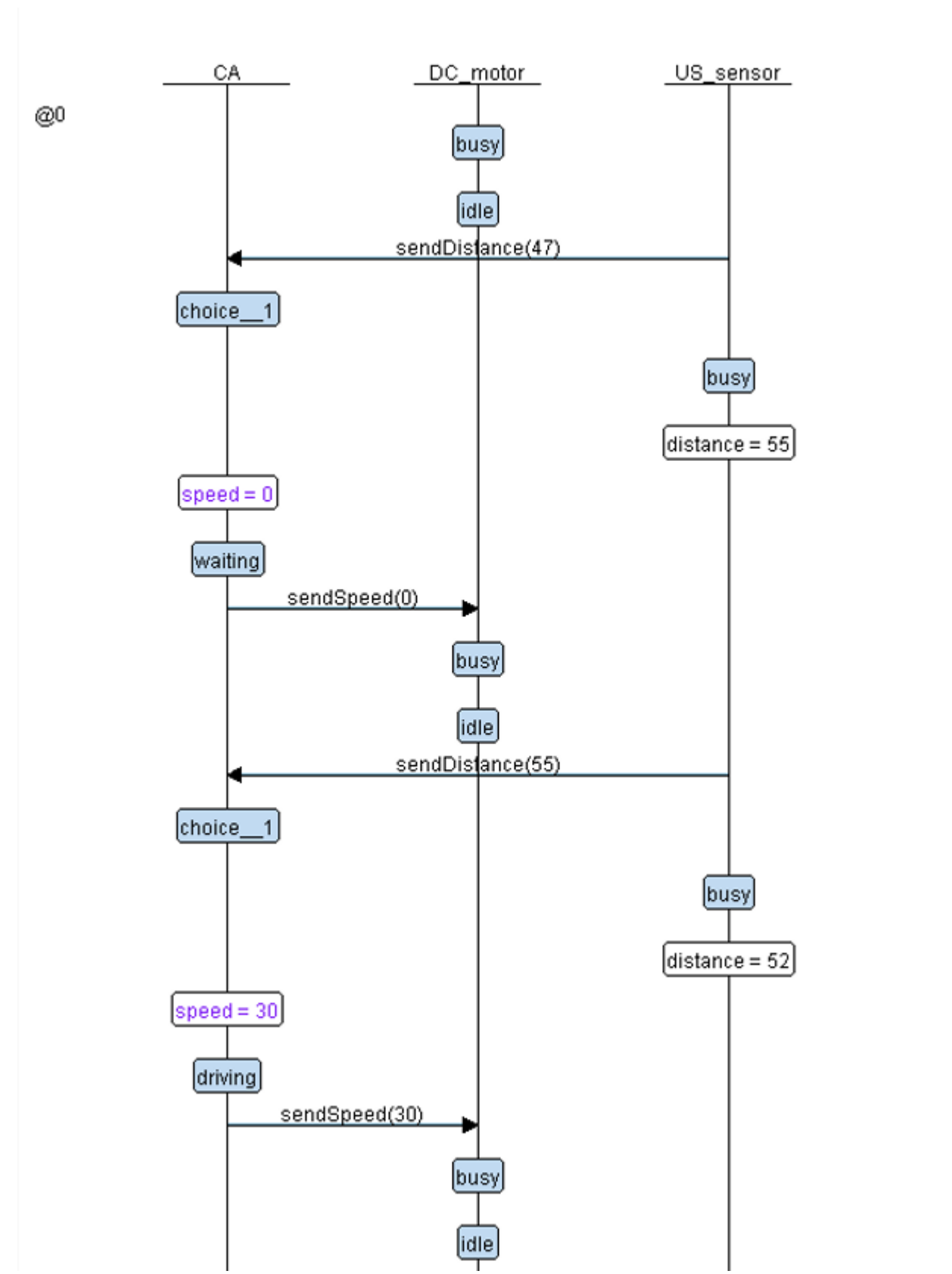
MODULES



DIAGRAMS



Logical Verification



```
1 US_init
2 DC_init
3 US ----- distance = 42 -----> CA
4 CA ----- Speed = 0 -----> DC
5 CA_waiting State distance = 42 , Speed = 0
6 DC_busy state : Speed = 0
7 US ----- distance = 43 -----> CA
8 CA ----- Speed = 0 -----> DC
9 CA_waiting State distance = 43 , Speed = 0
10 DC_busy state : Speed = 0
11 US ----- distance = 10 -----> CA
12 CA ----- Speed = 0 -----> DC
13 CA_waiting State distance = 10 , Speed = 0
14 DC_busy state : Speed = 0
15 US ----- distance = 46 -----> CA
16 CA ----- Speed = 0 -----> DC
17 CA_waiting State distance = 46 , Speed = 0
18 DC_busy state : Speed = 0
19 US ----- distance = 30 -----> CA
20 CA ----- Speed = 0 -----> DC
21 CA_waiting State distance = 30 , Speed = 0
22 DC_busy state : Speed = 0
23 US ----- distance = 50 -----> CA
24 CA ----- Speed = 0 -----> DC
25 CA_waiting State distance = 50 , Speed = 0
26 DC_busy state : Speed = 0
```