Incorrect Functionality of unsigned() System Function Due to Selection of Synthesis Parameters such as bufg.

I have encountered an inconsistency issue while using Vivado in non-project mode on Linux. After modifying certain parameters in the synthesis settings using the 'synth_design' command, specifically, 'synth_design -top top -flatten_hierarchy none -gated_clock_conversion off -bufg 10 -directive AlternateRoutability -fsm_extraction sequential -resource_sharing on', we intended to improve the code optimization efficiency through these parameter modifications. However, these changes should not affect the code consistency. Nevertheless, after synthesis, we observed errors in the functionality of functions like 'unsigned,' which led to an error during assignment to 'wire145' (line 227 in the attached 'rtl.v' file). Consequently, this inconsistency resulted in discrepancies in the output signals during simulation (line 9 in the simulation results), as shown in the attached image：

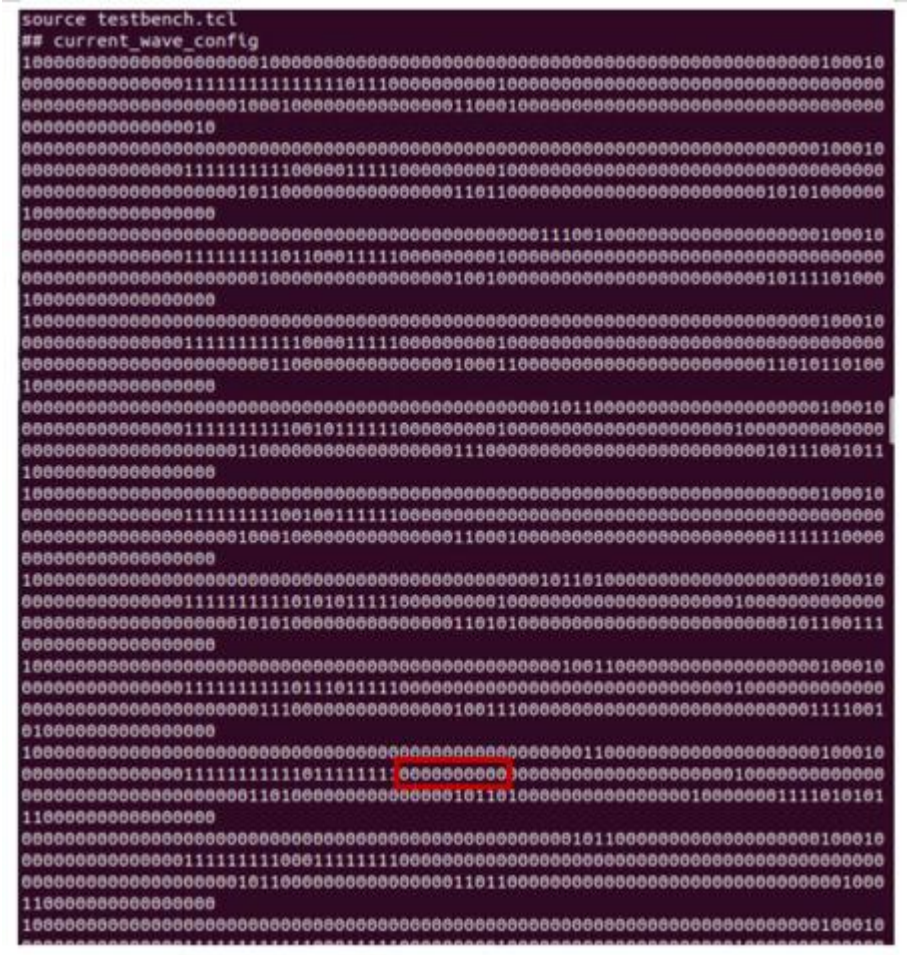

Figure 1: Synthesis with Default Parameters

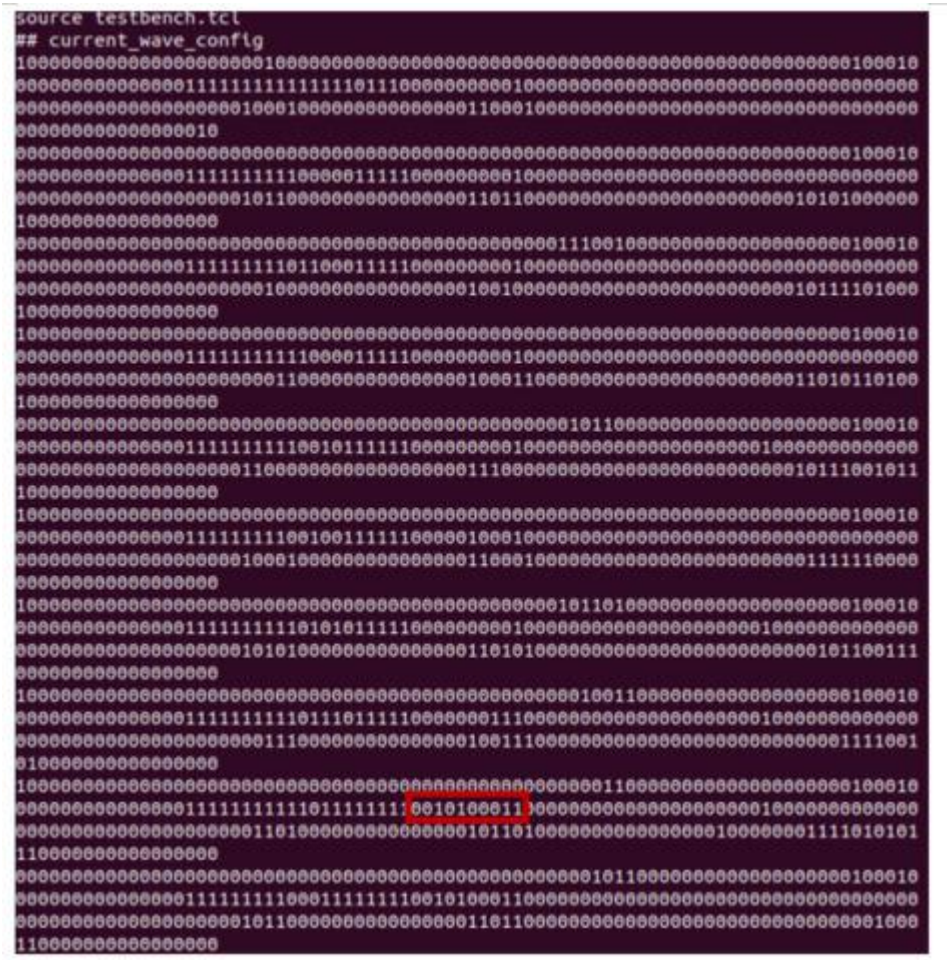

Figure 2:Modified some Parameter Values

In order to better reproduce the issue I encountered and identify the root cause, I will provide more detailed steps of my actions. The uploaded file package includes the following files: the original design file 'rtl.v'; TCL script files 'vivado.tcl' and 'new_vivado.tcl'; and the testbench files 'vivado_testbench.v' and 'new_vivado_testbench.v.

1.The "vivado.tcl" script reads the design file "rtl.v," synthesizes it using the default synthesis parameters, and generates the synthesis file "syn_vivado.v." Then, it performs simulation using the testbench file "vivado_testbench.v" to obtain simulation results.

2.The "new_vivado.tcl" script reads the same design file "rtl.v" but modifies some synthesis parameters (specified in the second line of the script: synth_design -top top -flatten_hierarchy none -gated_clock_conversion off -bufg 10 -directive AlternateRoutability -fsm_extraction sequential -resource_sharing on). It then synthesizes the design and generates the file "new_syn_vivado.v." The script performs simulation using the testbench file "new_vivado_testbench.v" to obtain simulation results.

3.The "vivado_testbench.v" and "new_vivado_testbench.v" files only differ in the include statement (line 6) where one includes "syn_vivado.v," and the other includes "new_syn_vivado.v"

to reflect the different synthesis files' names.

4.Run the Vivado synthesis and simulation in batch mode on Linux by executing "vivado -mode batch -source vivado.tcl" and "vivado -mode batch -source new_vivado.tcl" in separate terminals.

5.The simulation results are saved in "file1.txt" (default parameters) and "file2.txt" (modified parameters). The inconsistent part of the simulation results appears in the middle of the 9th line, with "0000000000" for the default parameters and "0010100011" for the modified parameters., as shown in the attached image：

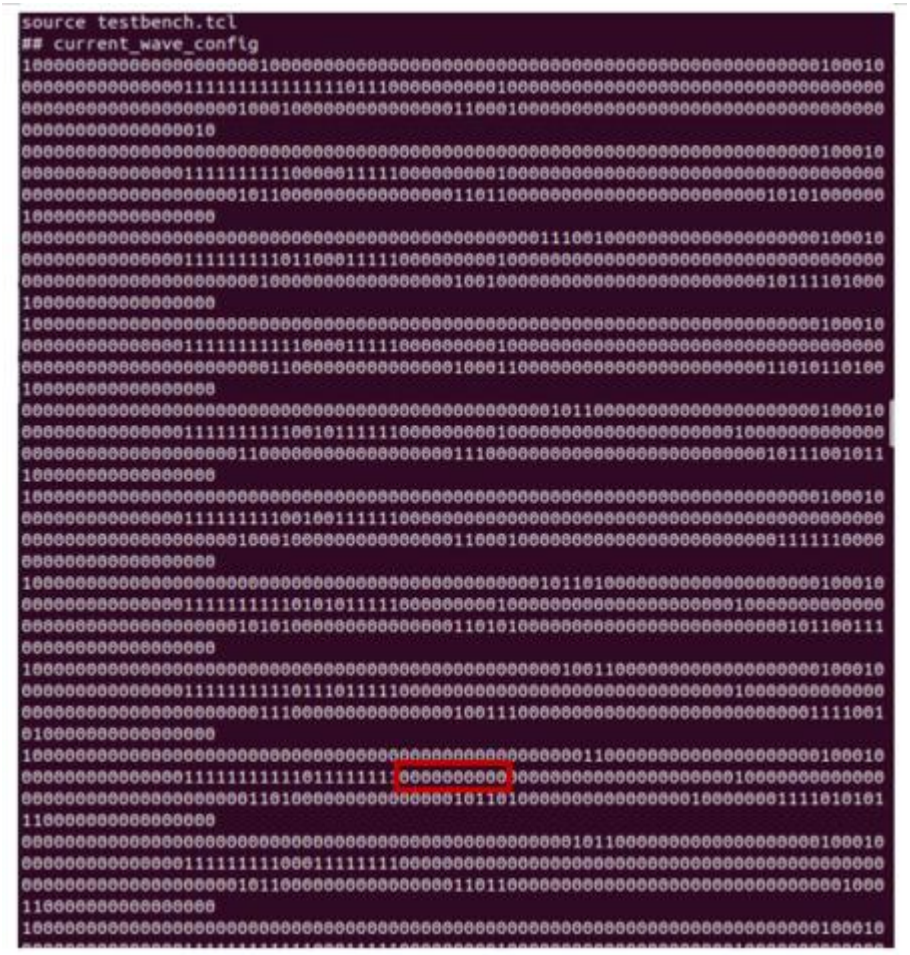

Figure 1: Synthesis with Default Parameters

Figure 2:Modified some Parameter Values

Please find attached the code of my program.

Thank you in advance for your attention to this matter.

I look forward to hearing from you regarding this issue.