Vivado Freezes During Optimization When Synthesizing Large Design.

Hello,

I am facing a problem where Vivado freezes during the synthesis of a large design. My setup includes Linux OS and Vivado version 2024.1. The synthesis commands are as follows:

vivado -mode tcl

read_verilog rtl.v

synth_design -top top -flatten_hierarchy full -gated_clock_conversion off -bufg 8 -directive AreaOptimized_medium -fsm_extraction johnson -resource_sharing auto -cascade_dsp force -incremental_mode off

Attached are the design file rtl.v, relevant system logs, and synthesis logs from both tools.

Thank you for your support in this matter.