Yosys Synthesis Fails with std::out_of_range Error in OPT_DEMORGAN Pass.

Hello,

I encountered a crash issue while using Yosys to synthesize a Verilog file. The specific details are as follows:

When running Yosys on the attached Verilog file (rtl.v), the synthesis process crashes during the OPT_DEMORGAN pass. The error message indicates a std::out_of_range exception, which occurs when the tool tries to inspect a $reduce_or cell and push inverters through reduction.

To rule out issues with the file itself, I have checked the Verilog file for syntax errors but did not find any obvious problems. Additionally, I am using the following version of Yosys:Yosys 0.41+126 (git sha1 855ac28, g++ 11.4.0-1ubuntu1~22.04 -fPIC -Os)

Here is the synthesis command I used:
yosys -p "
read_verilog rtl.v
hierarchy; proc; opt_clean; opt_dff; opt_demorgan; opt_lut_ins; opt_merge; opt_reduce; opt_dff; opt_expr; opt_muxtree; opt_share; opt_dff; opt_clean; opt_lut_ins; opt_reduce; opt_demorgan;
write_verilog syn_yosys.v"

Here is a snippet of the error log:

```
17. Executing OPT_REDUCE pass (consolidate $*mux and $reduce_* inputs).
  Optimizing cells in module \top.
    New input vector for $reduce_or cell $reduce_or$rtl.v:30$20: { }
  Optimizing cells in module \top.
Performed a total of 1 changes.

18. Executing OPT_DEMORGAN pass (push inverters through $reduce_* cells).
Inspecting $reduce_or cell $reduce_or$rtl.v:30$20 (0 inputs)
  0 / 0 inputs are inverted, pushing inverter through reduction
terminate called after throwing an instance of 'std::out_of_range'
  what():  vector::_M_range_check: __n (which is 0) >= this->size() (which is 0)
nyosys_script_n.sh: 第 4 行:  2469949 已放弃               （核心已转储） yosys
-p "
            read_verilog rtl.v
            hierarchy; proc; opt_clean; opt_dff; opt_demorgan; opt_lut_ins; opt_
merge; opt_reduce; opt_dff; opt_expr; opt_muxtree; opt_share; opt_dff; opt_clean
; opt_lut_ins; opt_reduce; opt_demorgan;
            write_verilog syn_yosys.v"
```