Vivado Stuck During Synthesis Process on Ubuntu System.

你好，

在使用 Vivado 综合设计文件时，我遇到了系统挂起的问题。我的系统运行在 Linux 上，使用的 Vivado 版本是 2024.1。我在 Ubuntu 终端中使用的相关命令如下：

vivado -mode tcl
read_verilog rtl.v
synth_design -top top -flatten_hierarchy full -gated_clock_conversion auto -bufg 45 -directive AreaOptimized_high -fsm_extraction sequential -resource_sharing off

本次 Using part: xc7k70tfbv676-1，我尝试了使用 -part xcvp1802-lsvc4072-2MP-e-S，但无法match。

```
source vivado_top.tcl
# read_verilog rtl.v
# synth_design -part xcvp1802-lsvc4072-2MP-e-S -top top -flatten_hierarchy full
-gated_clock_conversion auto -bufg 45 -directive AreaOptimized_high -fsm_extract
ion sequential -resource_sharing off
Command: synth_design -part xcvp1802-lsvc4072-2MP-e-S -top top -flatten_hierarch
y full -gated_clock_conversion auto -bufg 45 -directive AreaOptimized_high -fsm_
extraction sequential -resource_sharing off
WARNING: [Device 21-436] No parts matched 'xcvp1802-lsvc4072-2MP-e-S'
0 Infos, 1 Warnings, 0 Critical Warnings and 1 Errors encountered.
synth_design failed
ERROR: [Common 17-162] Invalid option value specified for '-part'.
INFO: [Common 17-206] Exiting Vivado at Sat Jul  6 18:02:27 2024...
```