Yosys Synthesis Error: Hash Table Exceeded Maximum Size.

Hello,
I encountered another issue while using Yosys to synthesize a Verilog file. The specific details are as follows:
I used the Verilog file rtl.v, and during the Yosys synthesis, a yosys_stderr.log file was generated with the following content:

“terminate called after throwing an instance of 'std::length_error'
what(): hash table exceeded maximum size.”

The synthesis process was interrupted due to this error. I suspect this is because the design file is too large, causing the hash table to exceed its maximum size limit. To rule out issues with the design file itself, I have checked the structure of the Verilog file but did not find any obvious problems. Additionally, I am using the latest version of Yosys.

Attached is the Verilog file (rtl.v) that triggers this issue. I hope to get the community's help and attention.