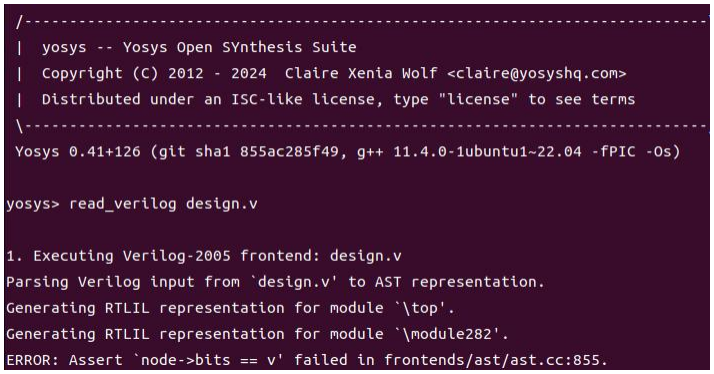
Yosys Verilog Parsing Error: Unable to Synthesize After Reading File.

Hello,
I encountered an error while using Yosys to read a Verilog file. The steps and the error message are as follows:



After this error, the parsing process is interrupted. I have checked the Verilog file for syntax errors but couldn't find any obvious issues. I am using the latest version of Yosys.

Attached is the Verilog file (design.v) that triggers the error.
Thank you in advance for your attention to this matter.
I look forward to hearing from you regarding this issue.