# POWER-EFFICIENT DRAM SENSE AMPLIFIER DESIGN USING POWER GATING IN 45NM TECHNOLOGY

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***Abstract* — This paper presents aVLSI circuit design, power consumption is a critical concern for memory and digital systems. This study presents the FSPA-VLSA methodology to enhance power efficiency in DRAM sense amplifiers, achieving an 81% reduction in power consumption. The proposed architecture offers significant benefits for low-power VLSI/ULSI applications. Implementation was carried out using Cadence Virtuoso at the 45nm technology node.**

**In the realm of VLSI circuit design, power consumption represents a fundamental consideration for both memory components and digital systems. This investigation introduces the FSPA-VLSA (Foot Switch PMOS Access Voltage Latch Type Sense Amplifier) methodology as an innovative solution for optimizing power efficiency in DRAM sense amplifiers. Through strategic integration of this approach within the open-bit architecture during memory read cycles, the implementation achieves an impressive 81% reduction in overall power consumption. The proposed circuit architecture demonstrates significant advantages for low-power VLSI/ULSI design applications. The development and implementation were executed utilizing Cadence Virtuoso tools at the 45nm technology node..**

**Keywords: Latch-type sense amplifier, capacitor, DRAM cell, FSPA-VLSA**

## I.INTRODUCTION

VLSI The advancement of semiconductor technology has profoundly shaped computing systems, with dynamic random-access memory (DRAM) emerging as a fundamental component in modern electronics. DRAM serves as the primary memory in various devices, such as computers, smartphones, and IoT systems, enabling fast data access and storage. Within DRAM architecture, sense amplifiers play a crucial role in optimizing read operations, directly impacting overall system efficiency. As semiconductor fabrication techniques continue to evolve, the design of DRAM sense amplifiers becomes increasingly vital to address growing demands for higher memory density, speed, and energy efficiency.

A strong understanding of DRAM technology is necessary to appreciate the importance of sense amplifiers in memory cells. DRAM stores data as charge within capacitors, where each cell consists of a capacitor and an access transistor. During read operations, sense amplifiers detect and amplify small voltage differences between charged and discharged states, ensuring accurate data retrieval. Additionally, DRAM refresh cycles are critical for maintaining data integrity, as stored charge degrades over time.

Analysing existing DRAM sense amplifier designs provides insight into architectural advancements and performance attributes. A thorough literature review, covering academic research and industry developments, evaluates sense amplifier designs based on factors such as speed, power efficiency, noise immunity, and area footprint. This analysis highlights the progression of sense amplifier architectures across technology nodes, showcasing their strengths and limitations.

With a solid grasp of DRAM and sense amplifier design principles, this study establishes clear objectives for designing DRAM sense amplifiers at 45nm technology. The design focuses on maximizing read speed, reducing power consumption, and improving robustness against process variations. A structured approach is employed for circuit

design, simulation, optimization, and validation, utilizing advanced semiconductor design tools.

**TYPES OF RAMS**

Random-access memory (RAM) is a fundamental component of modern computing, enabling rapid data access and temporary storage for active processes. Unlike non-volatile storage options like hard disk drives (HDDs) and solid-state drives (SSDs), RAM loses data when power is turned off. Several types of RAMS exist, each with distinct characteristics tailored for specific applications:

1. **Dynamic Random-Access Memory :** The most widely used RAM type, DRAM stores data in capacitors and requires periodic refreshing to maintain information. It offers high storage density and cost-effectiveness, despite slower access times compared to other RAM types.
2. **Static Random-Access Memory :** Unlike DRAM, SRAM uses latching circuitry to retain data, eliminating the need for refresh cycles. This results in faster access speedsand lower power consumption, making SRAM ideal for cache memory and high-speed applications.
3. **Synchronous Dynamic Random-Access Memory :** SDRAM synchronizes operations with the system clock for improved data transfer efficiency. Advanced variants like DDR (Double Data Rate) SDRAM and DDR4 further increase throughput by doubling data transfer rates per clock cycle.
4. **Non-Volatile RAM (NVRAM):** NVRAM retains stored data even without power, bridging the gap between volatile RAM and persistent storage. Technologies such as Magneto resistive RAM (MRAM) and Phase-Change RAM (PRAM) provide high-speed performance similar to volatile RAM while maintaining data persistence.

**Role of Sense Amplifiers in Memory Systems**

Sense amplifiers are essential in memory design, significantly enhancing the reliability, speed, and efficiency of data retrieval. These circuits act as intermediaries between memory cells and external processing units, ensuring accurate signal detection and amplification.

**Functions of Sense Amplifiers**

1. **Signal Amplification:** Sense amplifiers strengthen weak electrical signals from memory cells, ensuring accurate differentiation between stored binary states (0 and 1).
2. **Signal Detection and Interpretation:** Using differential sensing, they compare amplified signals against thresholds to determine the logical state of memory cells.
3. **Noise Rejection:** Advanced circuit techniques minimize interference and improve signal integrity, enhancing the reliability of read operations.
4. **Speed Optimization:** By accelerating the signal amplification and interpretation process, sense amplifiers reduce memoryaccess latency and improve system performance.

**Significance in Memory Systems**

Sense amplifiers play a vital role in ensuring accurate data retrieval, mitigating noise, and enabling high-speed operations. As semiconductor memory continues to evolve, optimizing sense amplifier designs remains a key research focus. The emergence of non-volatile memory and 3D memory architectures introduces new challenges and opportunities, requiring innovative solutions to enhance efficiency and reliability.

**Sense Amplifiers in DRAM Systems**

In DRAM, sense amplifiers are crucial for both read and write operations. Since DRAM stores data as charge, sense amplifiers detect and amplify small voltage differences during read operations, ensuring accurate data retrieval. Their efficiency directly influences memory speed and accuracy.

During write operations, sense amplifiers assist in driving the correct charge onto memory cells, ensuring reliable data storage. Additionally, they contribute to maintaining signal integrity by minimizing noise and external interference, which enhances overall system reliability

Since DRAM requires fast access times and high throughput, sense amplifiers must operate efficiently to reduce latency and improve performance. Their design significantly impacts the effectiveness of DRAM systems in modern computing applications.

Sense amplifiers are indispensable components in DRAM, playing a key role in read and write processes, noise reduction, and system efficiency. As memory technologies continue to evolve, optimizing sense amplifiers remains a priority for achieving faster, more energy-efficient, and reliable memory architectures. This study aims to contribute to this field by designing and optimizing DRAM sense amplifiers at 45nm technology, focusing on improving speed, power efficiency, and resilience against process variations.

## I. EXISTING METHOD

**Methodology for DRAM Sense Amplifier Open Bit Architecture**

This implementation combines the DRAM sense amplifier with the FSPA-VLSA to optimize performance characteristics. The DRAM memory array is configured in a dual-halves arrangement, with the FSPA-VLSA positioned centrally within the circuit structure. As shown in Figure 1, the architecture incorporates a pair of Inverters with cross couplings. The common input signal "SENSE" is distributed to transistors PM2, PM3, and NM2. The left and right bit lines (BLL and BLR) are connected to the FSPA-VLSA output terminals. For reference purposes, dummy cell columns are integrated on both sides of the circuit. NM5 and NM8, along with their associated storage capacitances (Cs), serve as dummy cells and are highlighted in the shaded region of the circuit diagram. Furthermore, two DRAM cells, each comprising an NMOS transistor and a capacitor, are positioned on either side of the FSPA-VLSA for data storage in the DRAM sense amplifier's open-bit architecture.

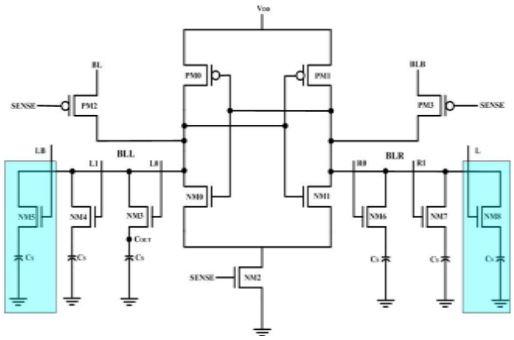


**Fig.1: Existing design of DRAM**

## II. PROPOSED METHOD

**Power Gating Mechanism**

The block diagram demonstrates how power gating implements power control through strategically placed switches along the circuit blocks' power supply lines. These control elements operate under the supervision of a dedicated power management unit (PMU), which severs power connections to inactive circuit sections, resulting in reduced overall energy usage. Power gating frequently integrates with complementary power optimization methodologies, notably Dynamic Voltage and Frequency Scaling (DVFS), to achieve enhanced energy efficiency in integrated circuits. Nevertheless, implementing this technology presents certain architectural challenges, including potential timing conflicts and increased complexity during state transitions. Despite these technical hurdles, power gating continues to serve as a crucial power conservation mechanism, establishing itself as a vital component in contemporary electronic devices ranging from smartphones to laptops and other portable equipment.

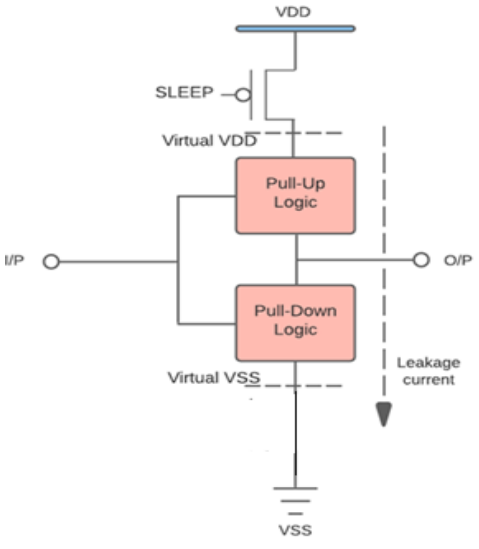



**Fig2: Block diagram of Power gating technique**

**Application of Power Gating in PMOS Transistors**

The figure below illustrates the power gating technique implemented in the proposed circuit. Previously, the VDD supply was directly applied to the circuit. However, in the extended design, power gating is incorporated into the PMOS transistor, allowing the VDD supply to pass through the PMOS switch.

By introducing this modification, the overall power consumption of the design is significantly reduced, improving energy efficiency without compromising performance.

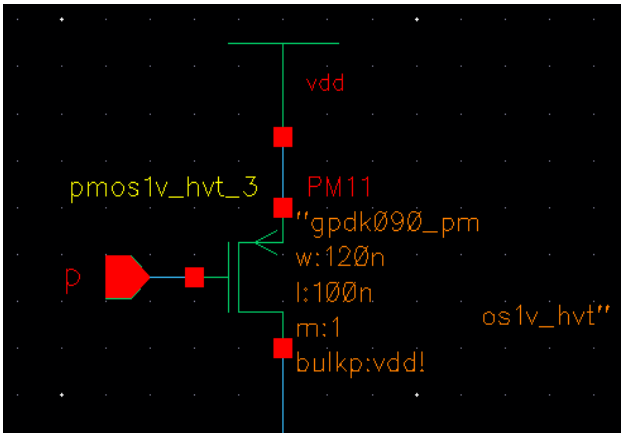



**Fig: PMOS TRANSISTOR FOR POWER GATING**

This diagram illustrates the implementation of the power gating technique. Previously, the VDD supply was applied directly to the circuit. In the extended design, power gating is incorporated by routing the VDD supply through a PMOS transistor. The implementation of this enhancement leads to substantial improvements in the design's energy efficiency.

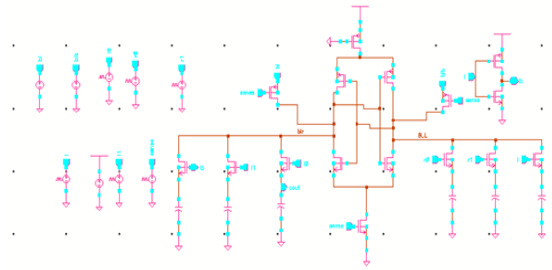


**Fig: The proposed circuit diagram with power gating technique**

**The Functional Principles of DRAM Sense Amplifier Open Bit Architecture Design**

The process begins by activating the L and LB lines simultaneously to ensure that the dummy cells charge to a voltage of VDD/2**.** During the read operation, one of the word lines **(**L0, L1, R0, or R1) is enabled. For instance, when Word Line L0 is activated, it causes a

voltage shift in BLL. Simultaneously, voltage generation occurs through the selection of a dummy cell located in the opposing memory segment, accomplished by elevating L.

Under these conditions, BLL and BLR remain balanced, positioning the BLR voltage between logic ‘0’ and ‘1’. This differential voltage causes the sense amplifier latch to toggle, ensuring accurate data retrieval.

**RESULTS:**

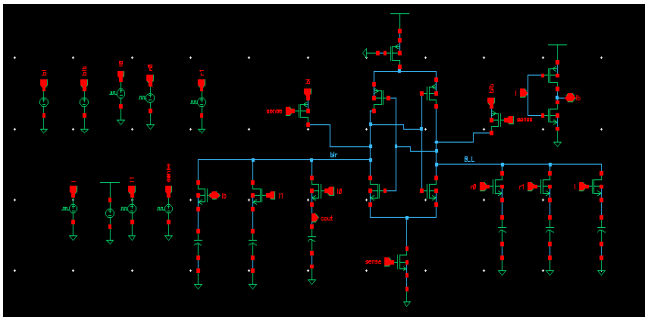


**Fig4: Schematic of DRAM**

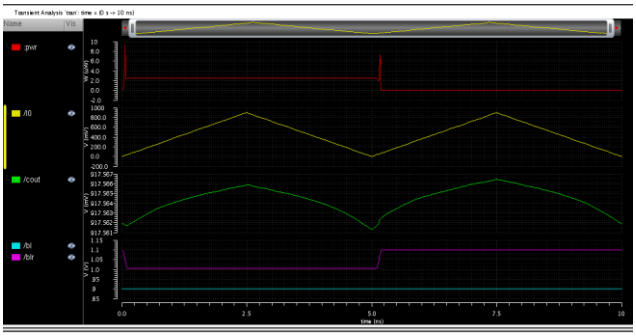
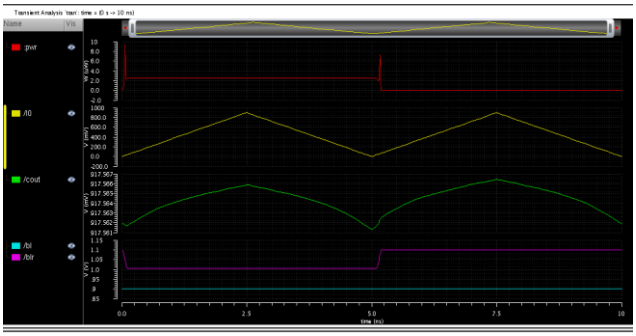


**Fig5: Output**



**WAVEFORMS OF DRAM**

```
Circuit inventory:
                 nodes  37
                 bsim4  17
      bsource_b538d7 17
             capacitor  6
               vsource  8
```

**Fig6: mos count for existing method**

```
Circuit inventory:
                 nodes  34
                 bsim4  15
      bsource_b538d7 15
             capacitor  6
               vsource  9
```

**Fig7: mos count for proposed method**

```
Circuit inventory:
                 nodes  36
                 bsim4  16
      bsource_b538d7 16
             capacitor  6
               vsource  9
```

**Fig8: mos count for extension method**

**COMPARISON TABLE OF MOS COUNT**

| | Mos count |
|---|---|
| **Existing** | 17 |
| **Proposed** | 15 |
| **Extension** | 16 |

**Table1: Comparison Table of MOS count**

The MOS count for the existing design is 17, while the proposed design reduces it to 15, and the extended version has 16. By using the FSPA-VLSA the MOS count is effectively reduced to 15 in the proposed method. In the extended version, the application of the power gating concept slightly increases the MOS count to 16, balancing power efficiency with circuit performance.

```
6.195E-6
```

**Fig9: power of existing method**

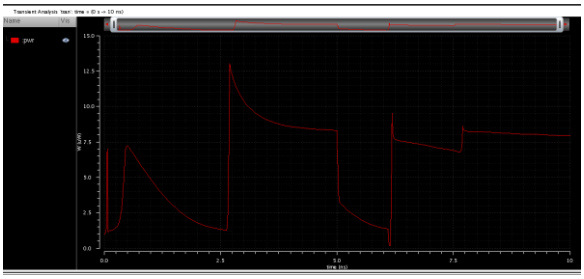


**Fig10: Existing method power consumption Graph**

```
1.328E-6
```

**Fig11: Proposed method power consumption**

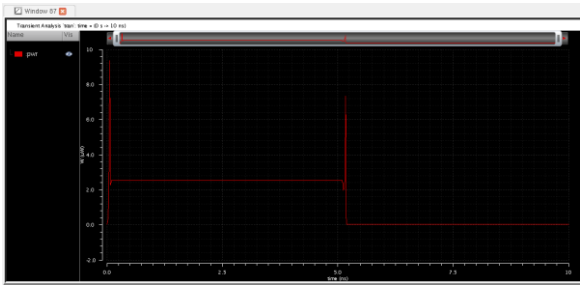


**Fig12: Proposed method power consumption Graph**

```
919.2E-9
```

**Fig13: Extension method power consumption**

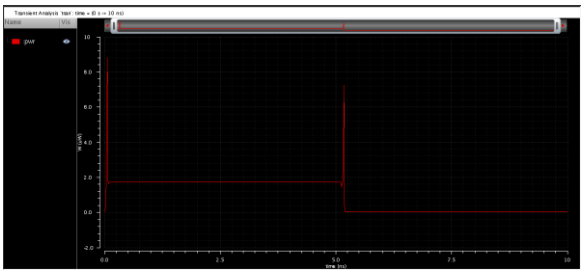


**Fig14: Extension method power consumption Graph**

**COMPARISON TABLE OF POWER**

| | Power (w) |
|---|---|
| **Existing** | 6.195 uw |
| **Proposed** | 1.328 uw |
| **Extension** | 919.2 nW |

**Table2: Comparison Table of Power**

The existing design consumes 6.195 µW of power, primarily due to high leakage and dynamic power dissipation. By adopting the proposed approach, which utilizes the FSPA-VLSA, power consumption is significantly lowered to 1.328 µW. This improvement is achieved by refining the sensing mechanism and reducing unnecessary power loss during read and write operations. Additionally, in the extended version, a power gating technique is implemented to further minimize leakage by disabling inactive circuit sections. As a result, power efficiency is significantly improved, reducing power consumption to 919.2 nW. This highlights a major advancement over both the existing and proposed designs, making the extended version highly suitable for low-power applications.


**Fig12: Delay of existing method**

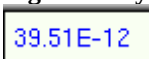



**Fig13: Delay of proposed method**

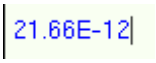



**Fig14: Delay of Extension**

**COMPARISON TABLE OF DELAY**

| | Delay(ps) |
|---|---|
| **Existing** | 331.4 |
| **Proposed** | 39.51 |
| **Extension** | 21.66 |

**Table3: Comparison Table of Delay**

The existing design experiences a delay of 331.4 ps, which affects overall performance. By implementing the proposed method, the delay is significantly reduced to 39.51 ps due to improved circuit efficiency and optimized signal propagation. Furthermore, the extended version enhances performance even further, bringing the delay down to 21.66 ps by incorporating advanced techniques that minimize transition time and improve response speed. This substantial reduction in delay makes the extended design highly efficient for high-speed applications.

**CONCLUSION:**

This research investigates energy usage patterns during memory retrieval processes in DRAM sense amplifiers utilizing the open-bit architectural approach. Findings indicate that the FSPA-VLSA-based DRAM sense amplifier consumes significantly less power compared to a basic latch-type sense amplifier within the same architecture. This reduction is due to the application of a uniform pulse across all circuit inputs. During operation, the PMOS transistor remains active while the NMOS transistor is inactive for half of the cycle, and in the other half When the NMOS transistor enters its conducting phase, the PMOS transistor simultaneously transitions to its blocking state. Consequently, the circuit primarily functions in a non-conductive mode, alternating between isolation through either the NMOS or PMOS transistor. leading to a substantial decrease in overall power consumption.

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