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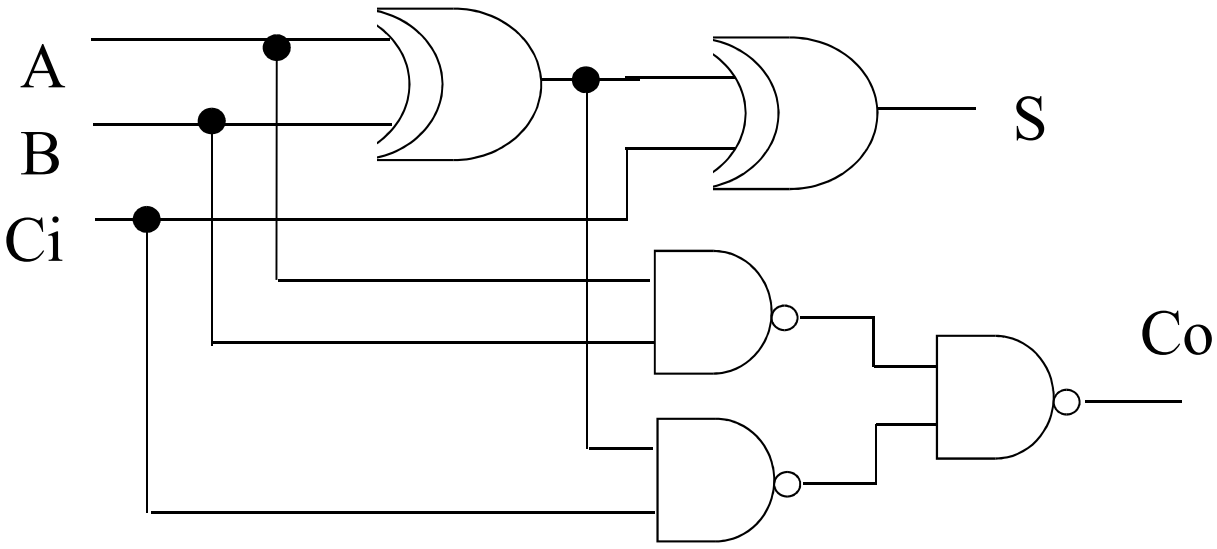
È stato chiesto di realizzare un sommatore a 16_Bit con ritardo massimo=30ns.

Come prima cosa era la scelta del full_adder.

Circuito FA

$$S = \bar{A}.Y + A.\bar{Y} = A \oplus B \oplus Ci$$

$$Co = (A \oplus B) . Ci \; . \; \overline{A.B}$$



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Descrizione in VDHL:

```
1  library IEEE;
2  use IEEE.STD_LOGIC_1164.ALL;
3  entity  FA IS
4      Port (A,B,Cin:IN STD_LOGIC;
5          Cout,S:OUT STD_LOGIC );
6  end ENTITY ;
7  architecture CIRCUITO of FA is
8  SIGNAL P:STD_LOGIC;
9  SIGNAL x:STD_LOGIC;
10 SIGNAL y:STD_LOGIC;
11 begin
12 P<=A XOR B after 1ns;
13 S<=P XOR Cin after 1ns;
14 x<=(A NAND B)after 1 ns;
15 y<=(P NAND Cin)after 1 ns;
16 Cout<=x NAND y after 1 ns ;
17 end architecture;
```

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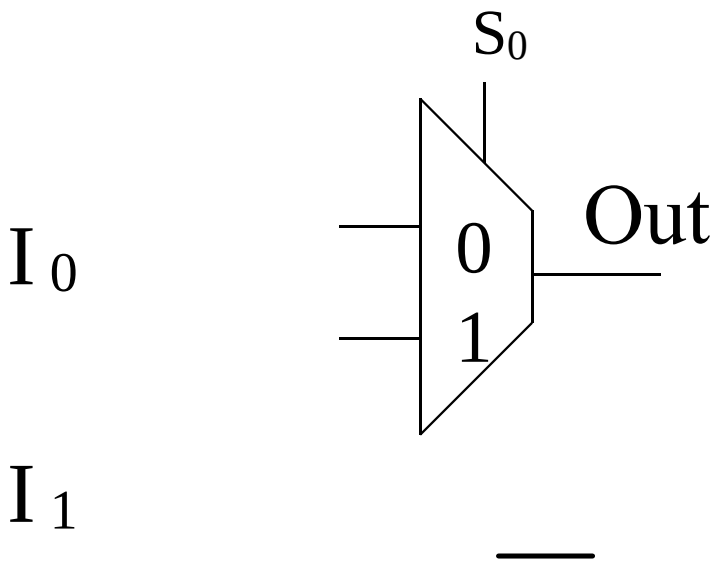
Come seconda cosa era la scelta del multiplexer

Multiplexer

Multiplexer 2:1



S_0	I_0	I_1	Out
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	0
1	1	1	1

$$Out = I_0 .\overline{S_0} + I_1.S_0$$

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Descrizione in VDHL.

```
1  library IEEE;
2  use IEEE.STD_LOGIC_1164.all;
3
4  entity mux2_1 is
5  port(A,B,Sel : in STD_LOGIC;
6       Z: out STD_LOGIC);
7  end entity;
8
9  architecture RTL of mux2_1 is
10 begin
11 with Sel select
12 Z <= A  after 1ns when  '0' ,
13       B after 1ns when  '1',
14       'X' when others;
15 end architecture;
```

Il Ripple-Carry Adder

E’ il sommatore più semplice e meno costoso: richiede meno porte logiche di

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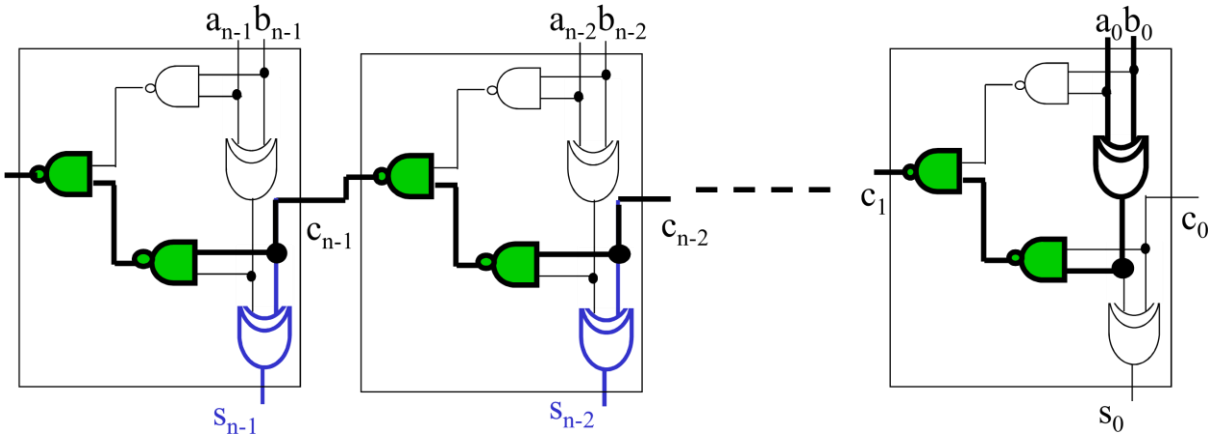
qualsiasi altro tipo di sommatore

Sommatore più lento.

Problema legato alla propagazione del riporto: l'i-esimo FA può generare il risultato corretto solo dopo avere ricevuto in ingresso il riporto generato dal precedente FA



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Path critici:

per s_{n-1} : 1 XOR+2·(n-1)NAND+1 XOR

per c_n : 1 XOR+2·n NAND

facendo i calcoli tenendo in considerazione (AND2, OR2, XOR2, MUX2, etc.) pari ad 1ns. Il ritardo incrementa del 10% per ogni ingresso aggiuntivo (Es. AND3=1.1ns, XOR4=1.2ns):

S_{delay}=32 ns

C_{delay}=31 ns

Quindi sono all' di fuori della soglia, per risolvere questo problema posso utilizzare un carry_select_adder per velocizzare la somma

Carry-Select Adder

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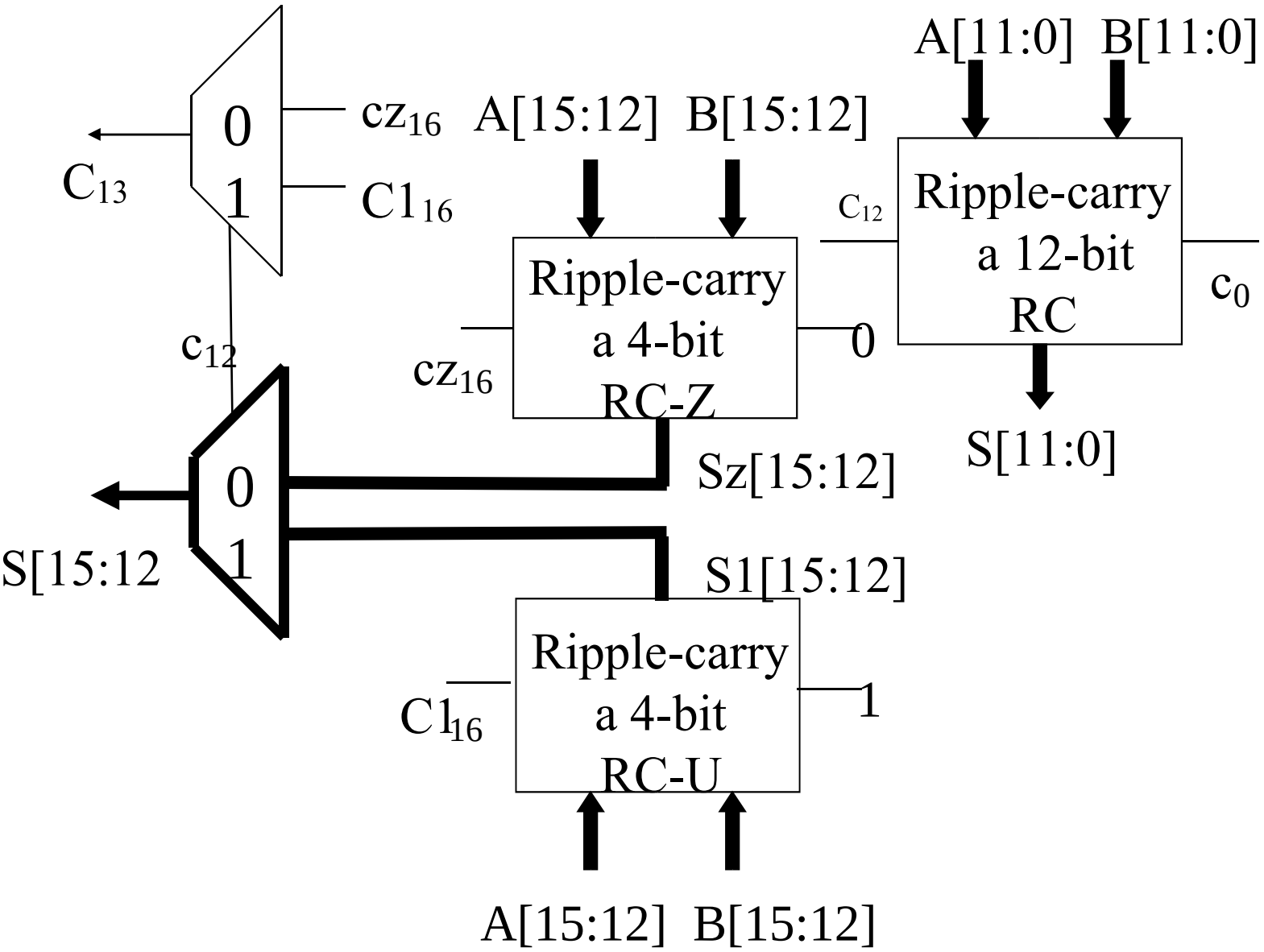

I blocchi RC, RC-Z e RC-U lavorano in parallelo

Path critici:

per s_{15} : 1 XOR+8 NAND+1 MUX

per c_{16} : 1 XOR+8 NAND+1 MUX

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facendo i calcoli tenendo in considerazione (AND2, OR2, XOR2, MUX2, etc.) pari ad 1ns. Il ritardo incrementa del 10% per ogni ingresso aggiuntivo (Es. AND3=1.1ns, XOR4=1.2ns):

S_{delay}=25 ns.

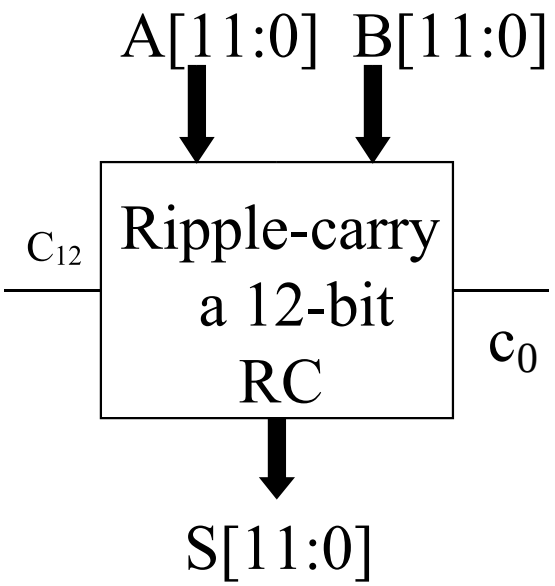
C_{delay}=26 ns.

Siamo nella soglia (30 ns).

Descrizione in VDHL.

```
1  library IEEE;
2  use IEEE.STD_LOGIC_1164.ALL;
3  entity adder_16 is
4    Port ( A,B:in std_logic_vector(15 downto 0);
5    Cin:in std_logic;
6    S:out std_logic_vector(15 downto 0);
7    Cout:out std_logic);
8  end adder_16;
9
10 architecture Behavioral of adder_16 is
11 component FA IS
12     Port (A,B,Cin:IN STD_LOGIC;
13         Cout,S:OUT STD_LOGIC );
14  end component;
15  component mux2_1 is
16 port(A,B,Sel : in STD_LOGIC;
17     Z: out STD_LOGIC);
18  end component;
19  signal c:std_logic_vector(13 downto 0);
20  signal cz,c1,Sz,S1:std_logic_vector(16 downto 12);

21 begin
22 c(0)<=Cin;
23 FA_f1:for i in 0 to 11 generate
24 FA1I:FA PORT MAP(A=>A(i),B=> B(i), Cin=>C(i), Cout=>C(i+1),S=>S(i));
25 end generate;
```



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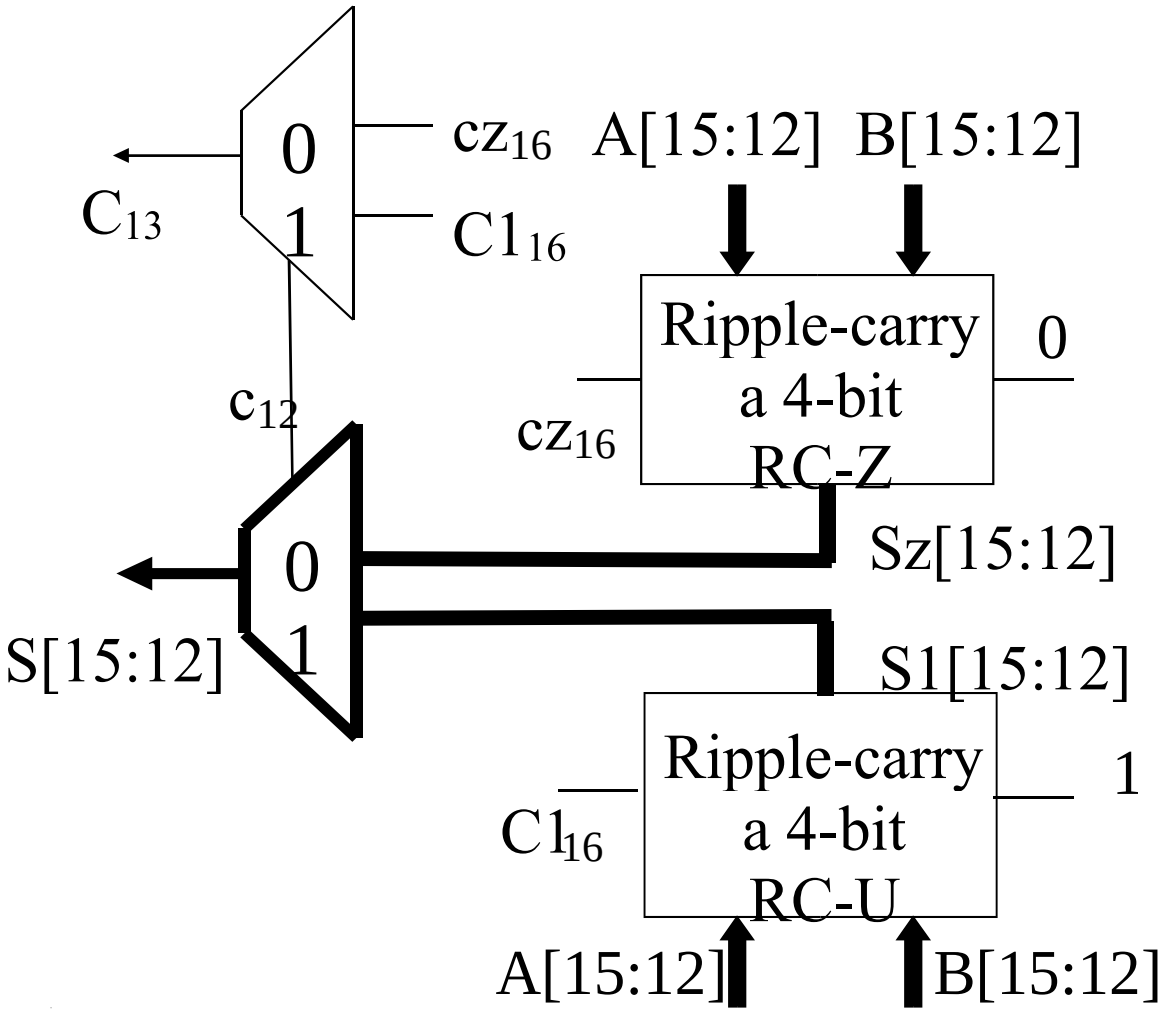


```
26 cz(12)<='0';
27 CSA0_f:for i in 12 to 15 generate
28 CSA0_I:FA PORT MAP(A=>A(i),B=> B(i), Cin=>cz(i), Cout=>cz(i+1),S=>Sz(i));
29 end generate;
30 c1(12)<='1';
31 CSA1_f:for i in 12 to 15 generate
32 CSA1_I:FA PORT MAP(A=>A(i),B=> B(i), Cin=>c1(i), Cout=>C1(i+1),S=>S1(i));
33 end generate;
34 MUX_f:for i in 12 to 15 generate
35 MUXI: mux2_1 PORT MAP(A=>Sz(i),B=>S1(i),Sel=>c(12),z=>S(i));
36 end generate;
37 MUXc: mux2_1 PORT MAP(A=>cz(16),B=>c1(16),Sel=>c(12),z=>c(13));
38
39 Cout<=c(13);
40 end Behavioral;
```

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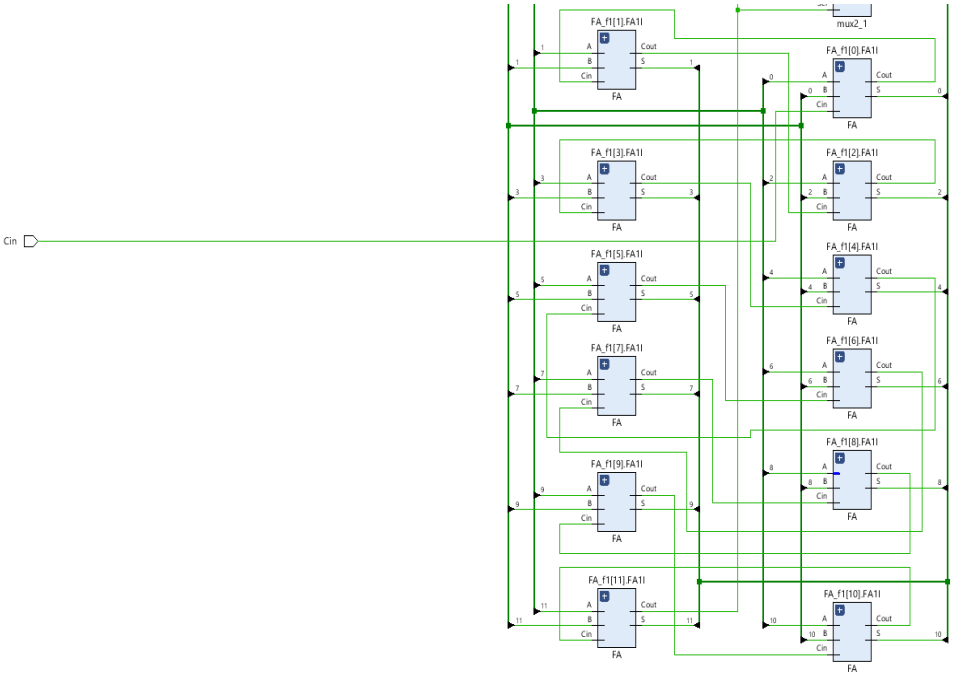
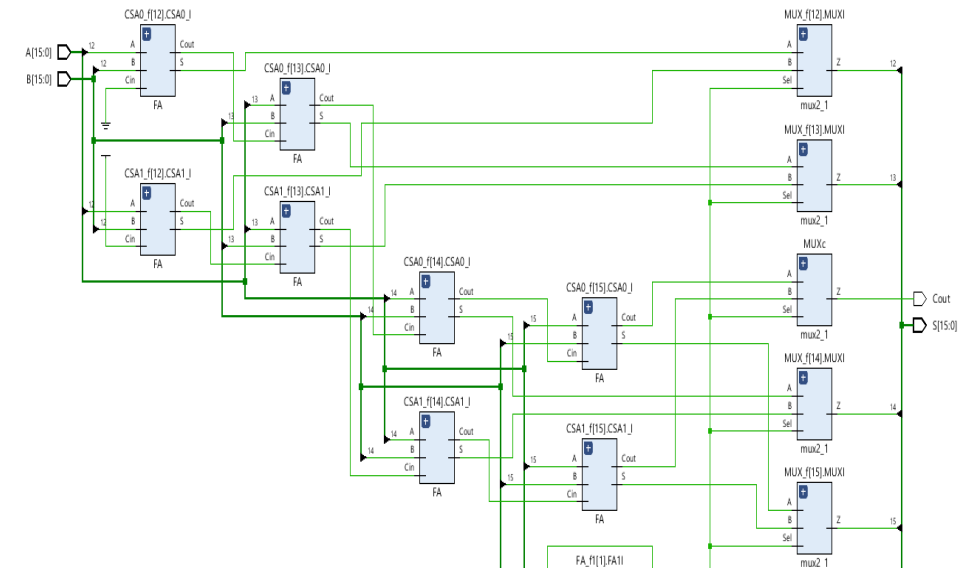
Ripple-carry a 12_Bit



Carry_select_adder a 4_Bit



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Codice TestBench

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
entity tb_adder16 is
--  Port ( );
end tb_adder16;
architecture Behavioral of tb_adder16 is
COMPONENT adder_16 is
  Port ( A,B:in std_logic_vector(15 downto 0);
  Cin:in std_logic;
  S:out std_logic_vector(15 downto 0);
  Cout:out std_logic);
END COMPONENT;
--Inputs
signal A : std_logic_vector(15 downto 0) := (others => '0');
signal B : std_logic_vector(15 downto 0) := (others => '0');
signal Cin : std_logic := '0';
--Outputs
signal S : std_logic_vector(15 downto 0);
signal Cout : std_logic;
BEGIN

uut: adder_16 PORT MAP (A=>A ,B=>B,Cin=>Cin,S=>S,Cout=>Cout);
STIMOLI: process
begin
 wait for 10 ns;
    A <= "1111111111111111";
    B <= "1111111111111111";
    Cin <= '1';
 wait for 29 ns;
    A <= "1111111111111111";
    B <= "0000000000000001";
    Cin <= '0';
 wait for 29 ns;
    A <= "0011000011110111";
    B <= "0100000101000001";
    Cin <= '0';
    wait for 29 ns;
  A <= "0100010010110000";
  B <= "0001010111011110";
  Cin <= '1';
```

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```
40    wait for 29 ns;
41        A <= "1111111111111111";
42        B <= "0000000000000001";
43        Cin <= '1';
44        wait for 29 ns;
45        A <= "0011000011110111";
46        B <= "0100000101000001";
47        Cin <= '0';
48        wait for 29 ns;
49        A <= "0000000000000001";
50        B <= "0010011000000111";
51        Cin <= '0';
52        wait for 29 ns;
53        A <= "0011110010110011";
54        B <= "1000111101011110";
55        Cin <= '0';
56        wait for 29 ns;
57        A <= "0010000100100001";
58        B <= "1111101000100111";
59        Cin <= '0';
60        wait for 29 ns;
61        A <= "0001011100100011";
62        B <= "0101101101101101";
63        Cin <= '0';
64        wait for 29 ns;
65        A <= "1011000110111001";
66        B <= "1001011001011111";
67        Cin <= '0';
68        wait for 29 ns;
69        A <= "0000001011001010";
70        B <= "1000011011101011";
71        Cin <= '1';
72        wait for 29 ns;
73        A <= "0011110110100000";
74        B <= "1100111000000010";
75        Cin <= '1';
76        wait for 29 ns;
77        A <= "0100000111111000";
78        B <= "0001001111100101";
79        Cin <= '1';
```

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```
80      wait for 29 ns;
81      A <= "1011111001111100";
82      B <= "0100001101010111";
83      Cin <= '1';
84      wait for 29 ns;
85      A <= "1111000110000001";
86      B <= "1010000100001110";
87      Cin <= '1';
88      wait for 29 ns;
89      A <= "0111000111001011";
90      B <= "1011000111010100";
91      Cin <= '1';
92      wait for 29 ns;
93      A <= "1011011101101010";
94      B <= "1100111100101110";
95      Cin <= '1';
96      wait for 29 ns;
97      A <= "1111001001010111";
98      B <= "0110010000100001";
99      Cin <= '0';
100     wait for 29 ns;
101     A <= "0111111101101100";
102     B <= "0111000100001111";
103     Cin <= '0';
104     wait for 29 ns;
105
106     A <= "0000111101111000";
107     B <= "1100011111101100";
108     Cin <= '0';
109     wait for 29 ns;
110
111     Cin <= '0';
112     A <= "0011100001100111";
113     B <= "1010101100100000";
114     Cin <= '0';
115     wait for 29 ns;
116
117     A <= "1111111101000111";
118     B <= "0110111101011100";
119     Cin <= '0';
```

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```
120     wait for 29 ns;
121     Cin <= '0';
122     A <= "0011111101000001";
123     B <= "1100100001100100";
124     Cin <= '0';
125     wait for 29 ns;
126     A <= "1011011111000111";
127     B <= "1000111101011011";
128     Cin <= '0';
129     wait for 29 ns;
130     A <= "1001011010010100";
131     B <= "0110001100101111";
132     Cin <= '0';
133     wait for 29 ns;
134     A <= "1111111000100101";
135     B <= "1111111110001010";
136     Cin <= '0';
137 wait;
138 end process;
139 end Behavioral;
```

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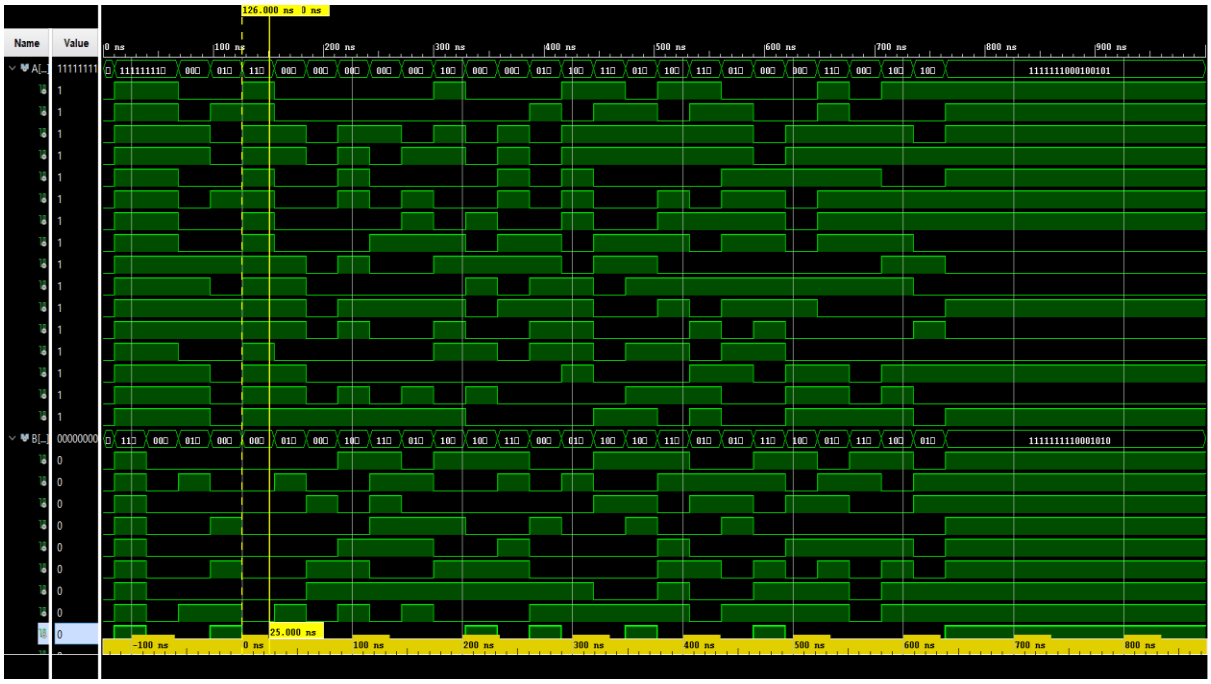
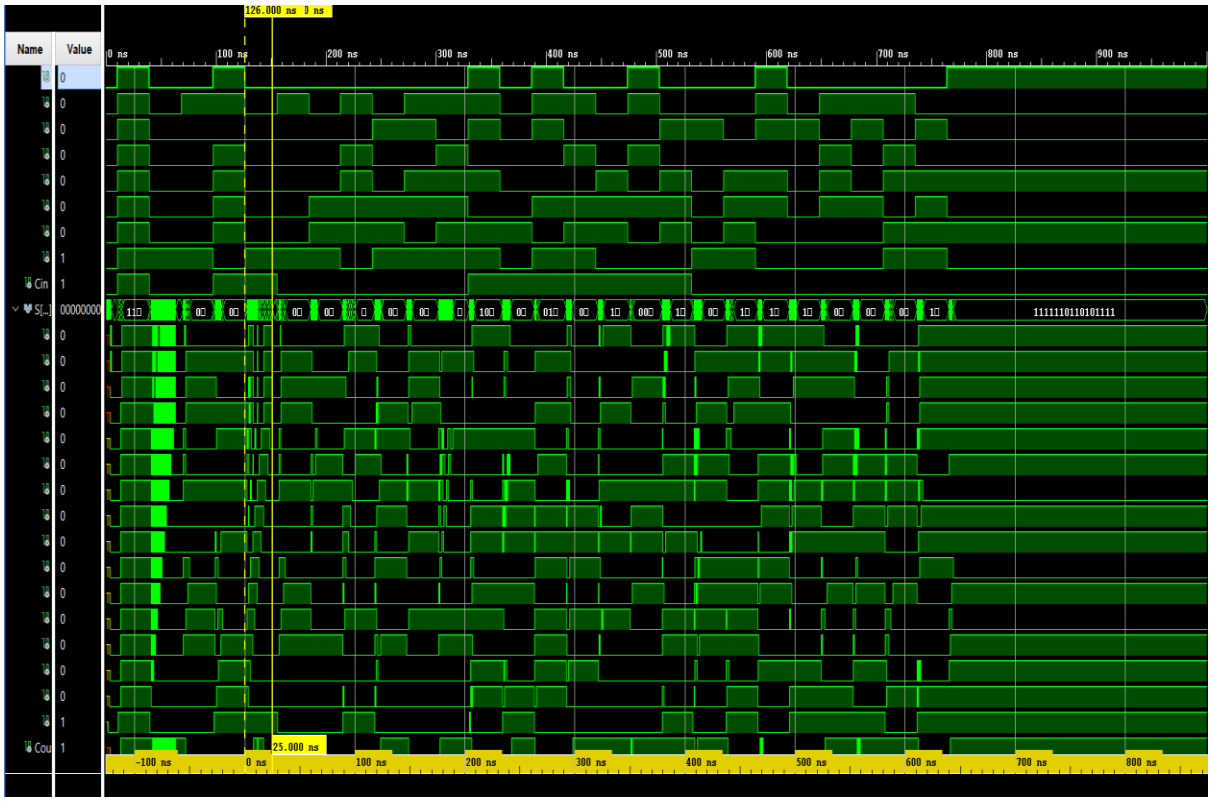
Simulazione:





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Path critici: