DIGITAL DESIGN

CS223

LAB-03 PRELIMINARY REPORT

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SECTION: 2

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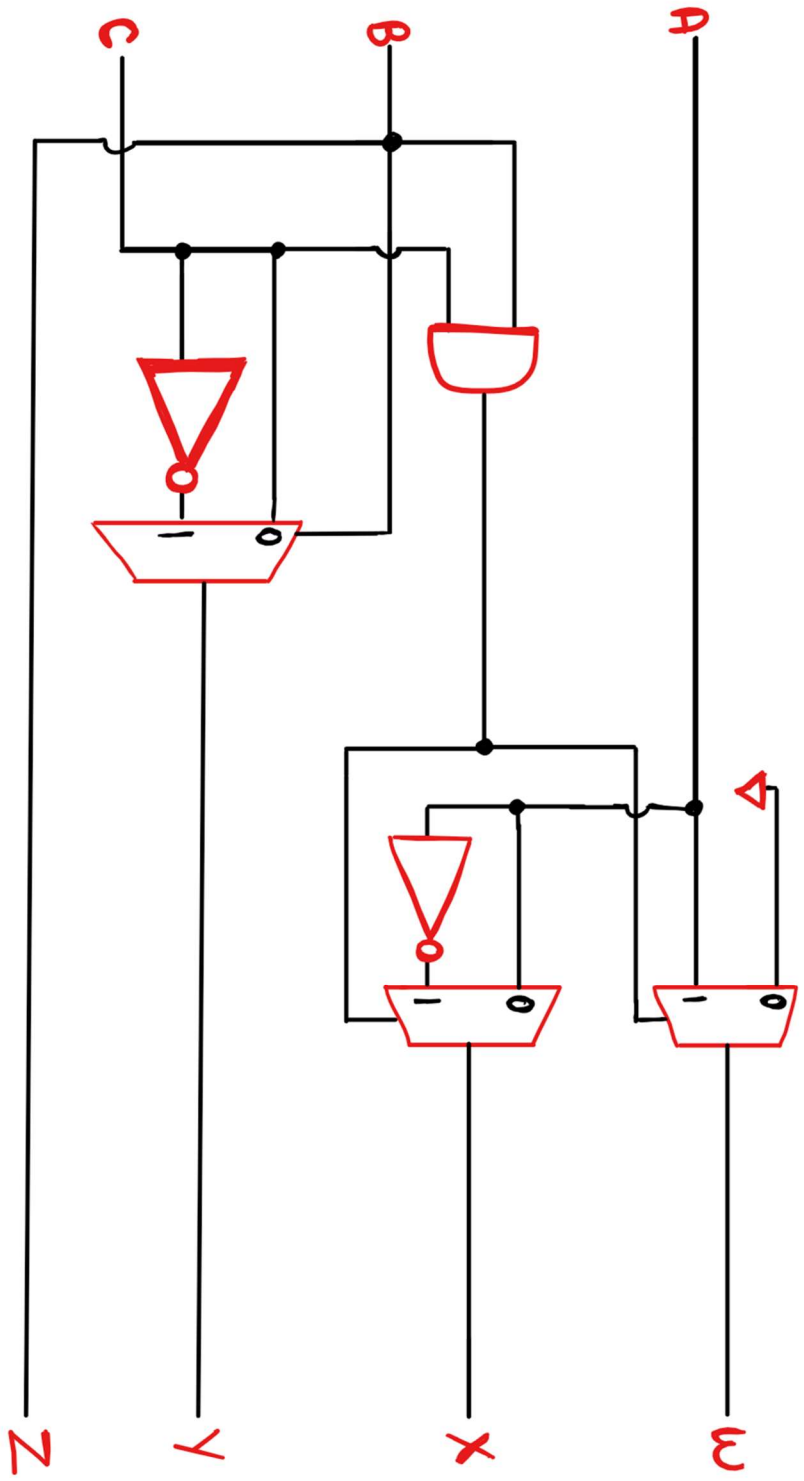
TRAINING PACK: 47

CODE CONVERTER (DESIGN)



CODE CONVERTER – LED OUTPUT (.SV CODE)

MODULE:

```
module twoToOneMux( input logic in0, in1, s,
                            output logic out);
       assign out = s ? in1 : in0;
endmodule
module codeConverter( input logic a, b, c,
                        output logic[3:0] out);
       logic andBC;
       logic notA;
       logic notC;

       and and0( andBC, b, c);
       not not0(notA, a);
       not not1(notC, c);
       twoToOneMux mux0( 0, a, andBC, out[3]);
    twoToOneMux mux1( a, notA, andBC, out[2]);
       twoToOneMux mux2( c, notC, b, out[1]);
    assign out[0] = b;
endmodule
```

TESTBENCH:

```
module codeConverter_testb();
       logic a, b, c;
       logic[3:0] out;
       codeConverter conv( a, b, c, out);
       initial begin
              a=0; b=0; c=0; #10;
              c=1; #10;
              b=1; c=0; #10;
              c=1; #10;
              a=1; b=0; c=0; #10;
              c=1; #10;
              b=1; c=0; #10;
              c=1; #10;
       end
endmodule
```

CODE CONVERTER – LED OUTPUT (CONSTRAINTS)

```
# Switches
set_property PACKAGE_PIN V17 [get_ports {c}]
      set_property IOSTANDARD LVCMOS33 [get_ports {c}]
set_property PACKAGE_PIN V16 [get_ports {b}]
      set_property IOSTANDARD LVCMOS33 [get_ports {b}]
set_property PACKAGE_PIN W16 [get_ports {a}]
      set_property IOSTANDARD LVCMOS33 [get_ports {a}]

# LEDs
set_property PACKAGE_PIN U16 [get_ports {out[0]}]
      set_property IOSTANDARD LVCMOS33 [get_ports {out[0]}]
set_property PACKAGE_PIN E19 [get_ports {out[1]}]
      set_property IOSTANDARD LVCMOS33 [get_ports {out[1]}]
set_property PACKAGE_PIN U19 [get_ports {out[2]}]
      set_property IOSTANDARD LVCMOS33 [get_ports {out[2]}]
set_property PACKAGE_PIN V19 [get_ports {out[3]}]
      set_property IOSTANDARD LVCMOS33 [get_ports {out[3]}]
```

CODE CONVERTER – 7 SEGMENT DISPLAY OUPUT(.SV CODE)

MODULE:

```
module codeConverter( input logic a, b, c, clock,
                      output logic[3:0] out, an,
                      output logic d, e, f, g, h, i, j, dp);
	logic andBC;
	logic notA;
	logic notC;

	and and0( andBC, b, c);
	not not0(notA, a);
	not not1(notC, c);
	twoToOneMux mux0( 0, a, andBC, out[3]);
	twoToOneMux mux1( a, notA, andBC, out[2]);
	twoToOneMux mux2( c, notC, b, out[1]);

	assign out[0] = b

	sevenSegDisplay seg( clock,
	                     out, 4'b0000, 4'b0000, 4'b0000,
	                     d, e, f, g, h, i, j, dp,
	                     an);
endmodule
```

CODE CONVERTER – 7 SEGMENT DISPLAY OUPUT(CONSTRAINTS)

```
# Clock signal
set_property PACKAGE_PIN W5 [get_ports clock]
	set_property IOSTANDARD LVCMOS33 [get_ports clock]
create_clock -add -name sys_clk_pin -period 10.00 -waveform {0 5} [get_ports clock]

#SWITCHES
set_property PACKAGE_PIN V17 [get_ports {c}]
	set_property IOSTANDARD LVCMOS33 [get_ports {c}]
set_property PACKAGE_PIN V16 [get_ports {b}]
	set_property IOSTANDARD LVCMOS33 [get_ports {b}]
set_property PACKAGE_PIN W16 [get_ports {a}]
	set_property IOSTANDARD LVCMOS33 [get_ports {a}]
```

```
# LEDs
set_property PACKAGE_PIN U16 [get_ports {out[0]}]
       set_property IOSTANDARD LVCMOS33 [get_ports {out[0]}]
set_property PACKAGE_PIN E19 [get_ports {out[1]}]
       set_property IOSTANDARD LVCMOS33 [get_ports {out[1]}]
set_property PACKAGE_PIN U19 [get_ports {out[2]}]
       set_property IOSTANDARD LVCMOS33 [get_ports {out[2]}]
set_property PACKAGE_PIN V19 [get_ports {out[3]}]
       set_property IOSTANDARD LVCMOS33 [get_ports {out[3]}]


#7 segment display
set_property PACKAGE_PIN W7 [get_ports {d}]
       set_property IOSTANDARD LVCMOS33 [get_ports {d}]
set_property PACKAGE_PIN W6 [get_ports {e}]
       set_property IOSTANDARD LVCMOS33 [get_ports {e}]
set_property PACKAGE_PIN U8 [get_ports {f}]
       set_property IOSTANDARD LVCMOS33 [get_ports {f}]
set_property PACKAGE_PIN V8 [get_ports {g}]
       set_property IOSTANDARD LVCMOS33 [get_ports {g}]
set_property PACKAGE_PIN U5 [get_ports {h}]
       set_property IOSTANDARD LVCMOS33 [get_ports {h}]
set_property PACKAGE_PIN V5 [get_ports {i}]
       set_property IOSTANDARD LVCMOS33 [get_ports {i}]
set_property PACKAGE_PIN U7 [get_ports {j}]
       set_property IOSTANDARD LVCMOS33 [get_ports {j}]
set_property PACKAGE_PIN V7 [get_ports dp]
    set_property IOSTANDARD LVCMOS33 [get_ports dp]
set_property PACKAGE_PIN U2 [get_ports {an[0]}]
    set_property IOSTANDARD LVCMOS33 [get_ports {an[0]}]
set_property PACKAGE_PIN U4 [get_ports {an[1]}]
    set_property IOSTANDARD LVCMOS33 [get_ports {an[1]}]
set_property PACKAGE_PIN V4 [get_ports {an[2]}]
    set_property IOSTANDARD LVCMOS33 [get_ports {an[2]}]
set_property PACKAGE_PIN W4 [get_ports {an[3]}]
    set_property IOSTANDARD LVCMOS33 [get_ports {an[3]}]
```