**DIGITAL DESIGN**

**CS223**

**LAB-03 PRELIMINARY REPORT**

**NAME: MUHAMMAD ARHAM KHAN**

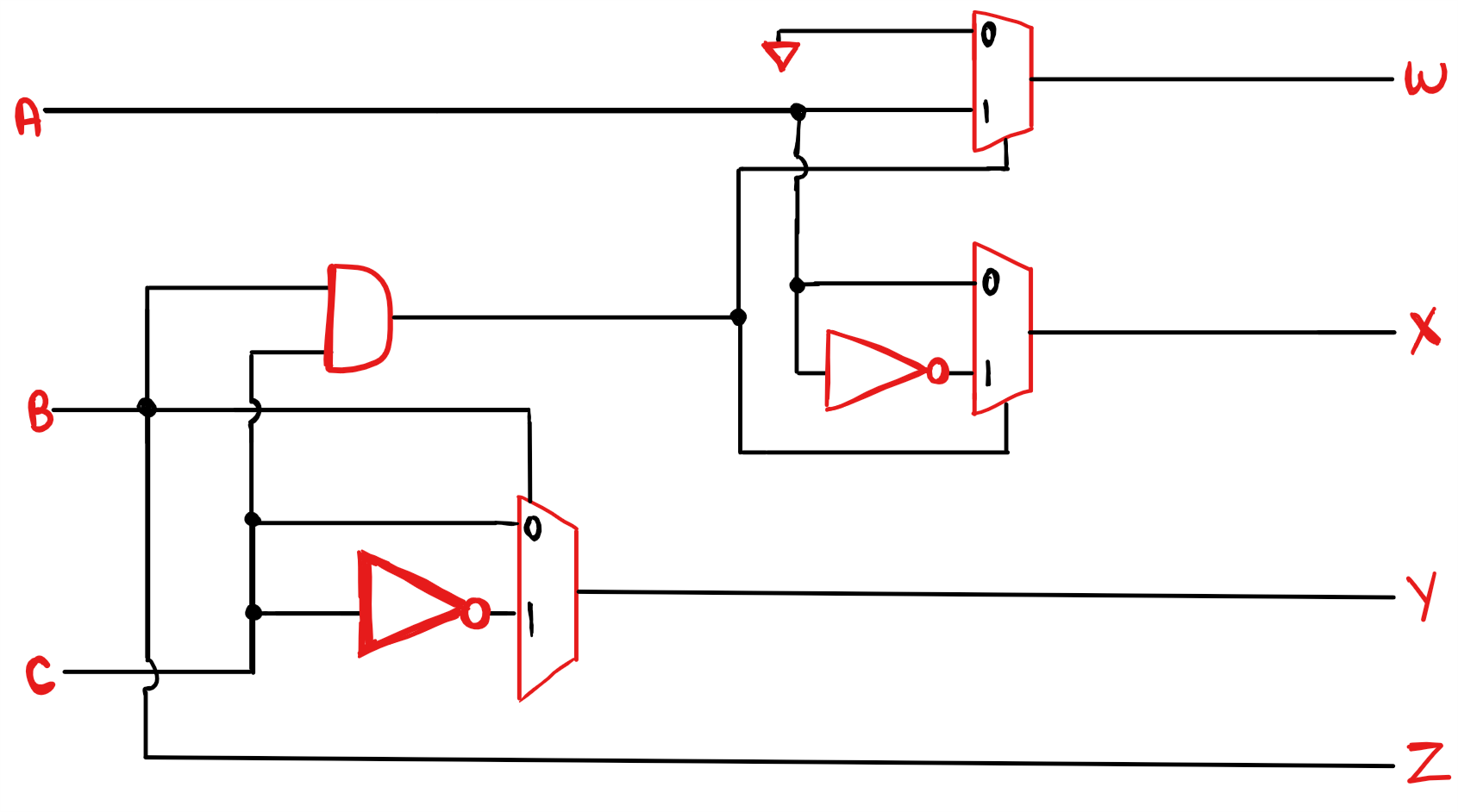
**BILKENT ID: 21701848**

**SECTION: 2**

**DATE: 6 NOV, 2018**

**TRAINING PACK: 47**

**CODE CONVERTER (DESIGN)**

****

**CODE CONVERTER – LED OUTPUT (.SV CODE)**

**MODULE:**

module twoToOneMux( input logic in0, in1, s,

output logic out);

assign out = s ? in1 : in0;

endmodule

module codeConverter( input logic a, b, c,

output logic[3:0] out);

logic andBC;

logic notA;

logic notC;

and and0( andBC, b, c);

not not0(notA, a);

not not1(notC, c);

twoToOneMux mux0( 0, a, andBC, out[3]);

twoToOneMux mux1( a, notA, andBC, out[2]);

twoToOneMux mux2( c, notC, b, out[1]);

assign out[0] = b;

endmodule

**TESTBENCH:**

module codeConverter\_testb();

logic a, b, c;

logic[3:0] out;

codeConverter conv( a, b, c, out);

initial begin

a=0; b=0; c=0; #10;

c=1; #10;

b=1; c=0; #10;

c=1; #10;

a=1; b=0; c=0; #10;

c=1; #10;

b=1; c=0; #10;

c=1; #10;

end

endmodule

**CODE CONVERTER – LED OUTPUT (CONSTRAINTS)**

# Switches

set\_property PACKAGE\_PIN V17 [get\_ports {c}]

set\_property IOSTANDARD LVCMOS33 [get\_ports {c}]

set\_property PACKAGE\_PIN V16 [get\_ports {b}]

set\_property IOSTANDARD LVCMOS33 [get\_ports {b}]

set\_property PACKAGE\_PIN W16 [get\_ports {a}]

set\_property IOSTANDARD LVCMOS33 [get\_ports {a}]

# LEDs

set\_property PACKAGE\_PIN U16 [get\_ports {out[0]}]

set\_property IOSTANDARD LVCMOS33 [get\_ports {out[0]}]

set\_property PACKAGE\_PIN E19 [get\_ports {out[1]}]

set\_property IOSTANDARD LVCMOS33 [get\_ports {out[1]}]

set\_property PACKAGE\_PIN U19 [get\_ports {out[2]}]

set\_property IOSTANDARD LVCMOS33 [get\_ports {out[2]}]

set\_property PACKAGE\_PIN V19 [get\_ports {out[3]}]

set\_property IOSTANDARD LVCMOS33 [get\_ports {out[3]}]

**CODE CONVERTER – 7 SEGMENT DISPLAY OUPUT(.SV CODE)**

**MODULE:**

module codeConverter( input logic a, b, c, clock,

output logic[3:0] out, an,

output logic d, e, f, g, h, i, j, dp);

logic andBC;

logic notA;

logic notC;

and and0( andBC, b, c);

not not0(notA, a);

not not1(notC, c);

twoToOneMux mux0( 0, a, andBC, out[3]);

twoToOneMux mux1( a, notA, andBC, out[2]);

twoToOneMux mux2( c, notC, b, out[1]);

assign out[0] = b

sevenSegDisplay seg( clock,

out, 4'b0000, 4'b0000, 4'b0000,

d, e, f, g, h, i, j, dp,

an);

endmodule

**CODE CONVERTER – 7 SEGMENT DISPLAY OUPUT( CONSTRAINTS)**

# Clock signal

set\_property PACKAGE\_PIN W5 [get\_ports clock]

set\_property IOSTANDARD LVCMOS33 [get\_ports clock]

create\_clock -add -name sys\_clk\_pin -period 10.00 -waveform {0 5} [get\_ports clock]

#SWITCHES

set\_property PACKAGE\_PIN V17 [get\_ports {c}]

set\_property IOSTANDARD LVCMOS33 [get\_ports {c}]

set\_property PACKAGE\_PIN V16 [get\_ports {b}]

set\_property IOSTANDARD LVCMOS33 [get\_ports {b}]

set\_property PACKAGE\_PIN W16 [get\_ports {a}]

set\_property IOSTANDARD LVCMOS33 [get\_ports {a}]

# LEDs

set\_property PACKAGE\_PIN U16 [get\_ports {out[0]}]

set\_property IOSTANDARD LVCMOS33 [get\_ports {out[0]}]

set\_property PACKAGE\_PIN E19 [get\_ports {out[1]}]

set\_property IOSTANDARD LVCMOS33 [get\_ports {out[1]}]

set\_property PACKAGE\_PIN U19 [get\_ports {out[2]}]

set\_property IOSTANDARD LVCMOS33 [get\_ports {out[2]}]

set\_property PACKAGE\_PIN V19 [get\_ports {out[3]}]

set\_property IOSTANDARD LVCMOS33 [get\_ports {out[3]}]

#7 segment display

set\_property PACKAGE\_PIN W7 [get\_ports {d}]

set\_property IOSTANDARD LVCMOS33 [get\_ports {d}]

set\_property PACKAGE\_PIN W6 [get\_ports {e}]

set\_property IOSTANDARD LVCMOS33 [get\_ports {e}]

set\_property PACKAGE\_PIN U8 [get\_ports {f}]

set\_property IOSTANDARD LVCMOS33 [get\_ports {f}]

set\_property PACKAGE\_PIN V8 [get\_ports {g}]

set\_property IOSTANDARD LVCMOS33 [get\_ports {g}]

set\_property PACKAGE\_PIN U5 [get\_ports {h}]

set\_property IOSTANDARD LVCMOS33 [get\_ports {h}]

set\_property PACKAGE\_PIN V5 [get\_ports {i}]

set\_property IOSTANDARD LVCMOS33 [get\_ports {i}]

set\_property PACKAGE\_PIN U7 [get\_ports {j}]

set\_property IOSTANDARD LVCMOS33 [get\_ports {j}]

set\_property PACKAGE\_PIN V7 [get\_ports dp]

set\_property IOSTANDARD LVCMOS33 [get\_ports dp]

set\_property PACKAGE\_PIN U2 [get\_ports {an[0]}]

set\_property IOSTANDARD LVCMOS33 [get\_ports {an[0]}]

set\_property PACKAGE\_PIN U4 [get\_ports {an[1]}]

set\_property IOSTANDARD LVCMOS33 [get\_ports {an[1]}]

set\_property PACKAGE\_PIN V4 [get\_ports {an[2]}]

set\_property IOSTANDARD LVCMOS33 [get\_ports {an[2]}]

set\_property PACKAGE\_PIN W4 [get\_ports {an[3]}]

set\_property IOSTANDARD LVCMOS33 [get\_ports {an[3]}]