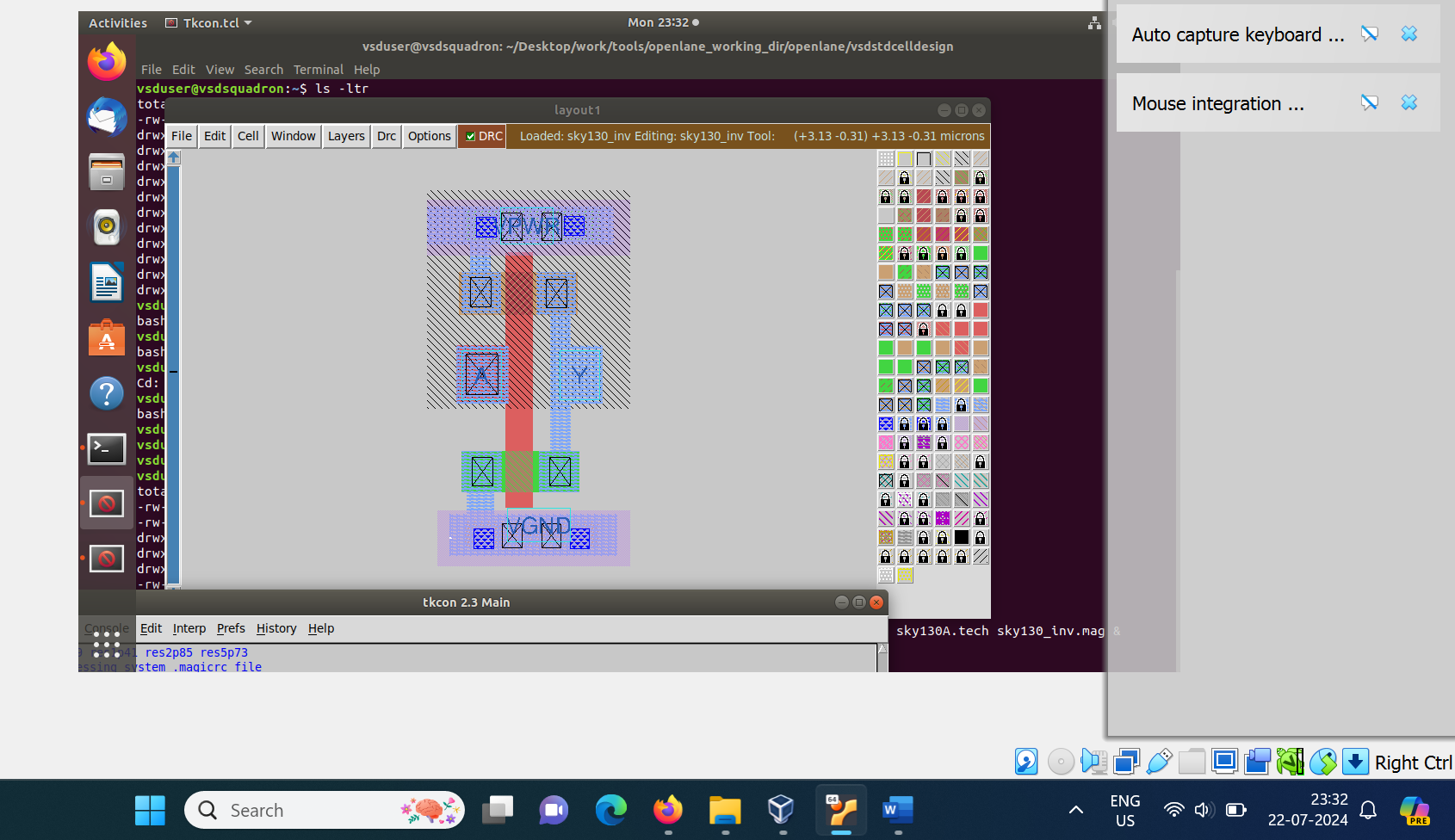
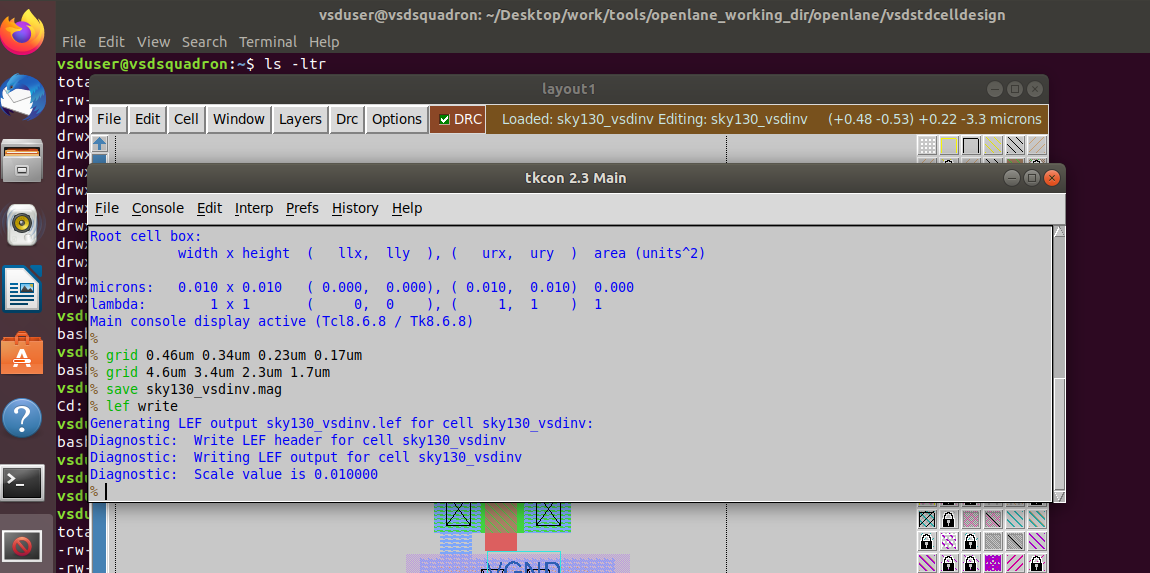
**LAB #4 : Pre-layout timing analysis ( vsdstdcelldesign of inverter to be synthesized in picorv32a design and check for floorplane, placement )**

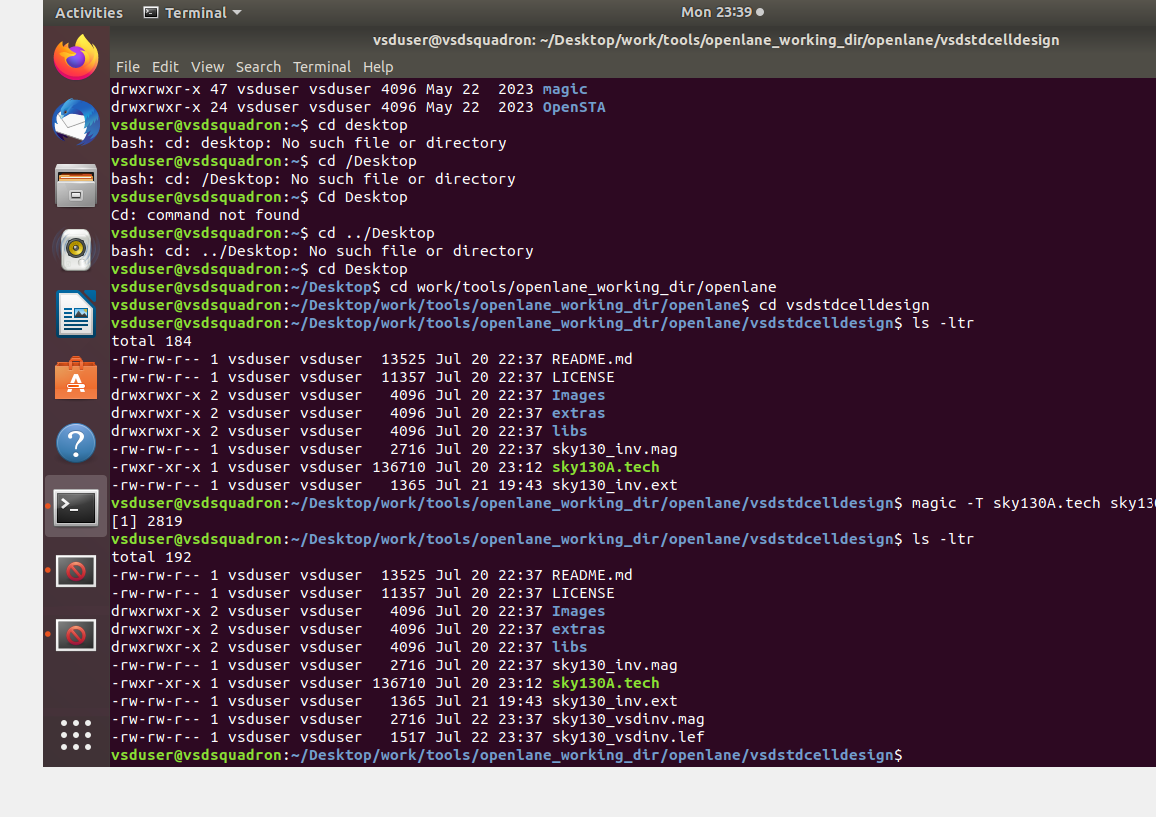
1. Custom layout of inverter
2. Commands:



1. Creating sky130\_vsdinv.mag

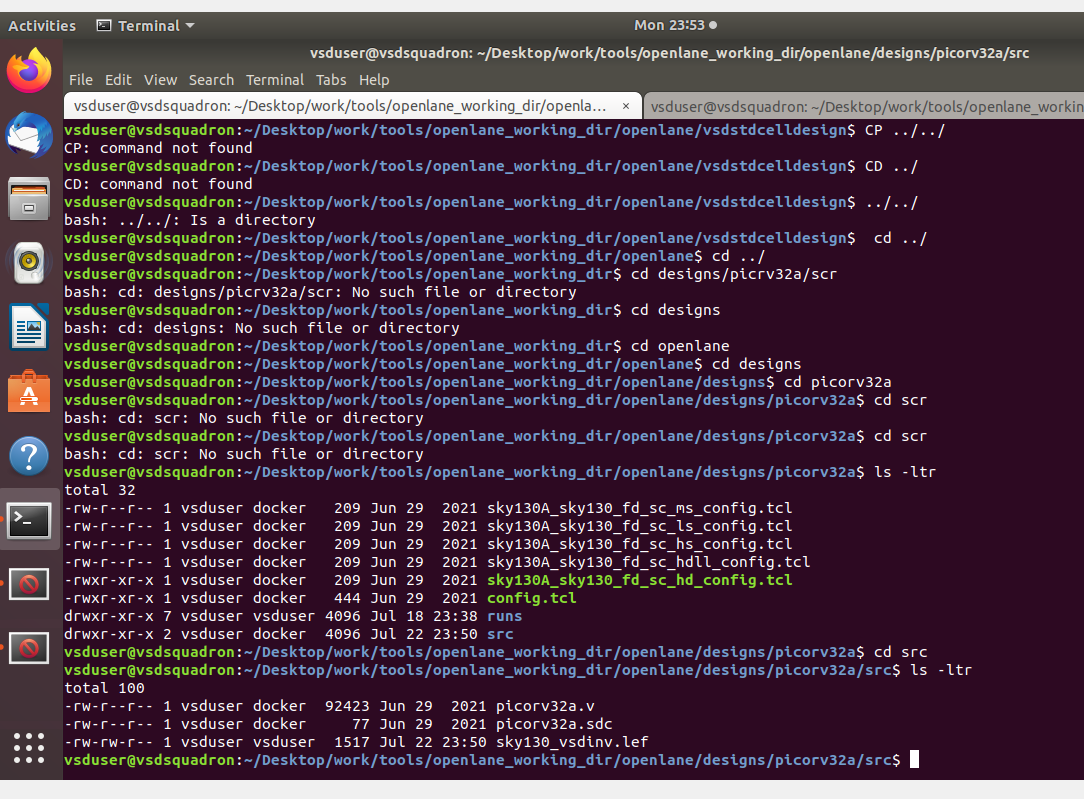


1. Check for file sky130\_vsdinv.mag in the folder vsdstdcelldesign

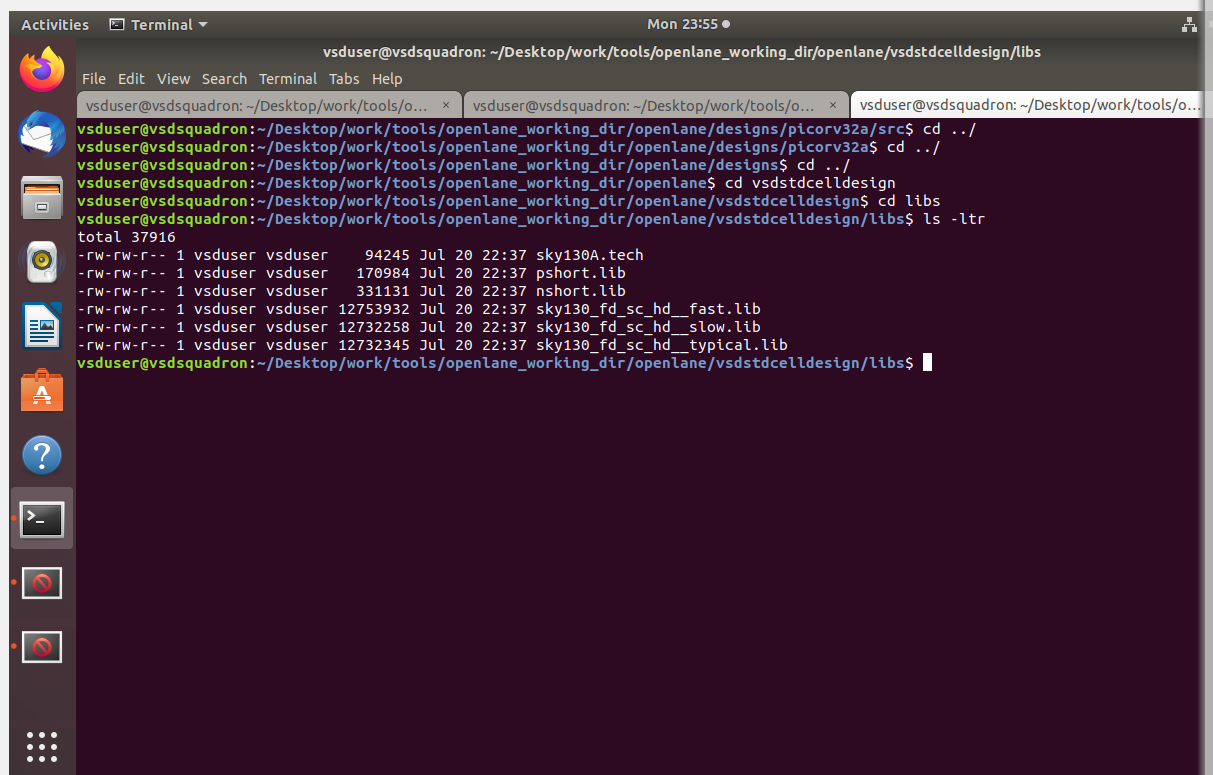


1. Editing config.tcl

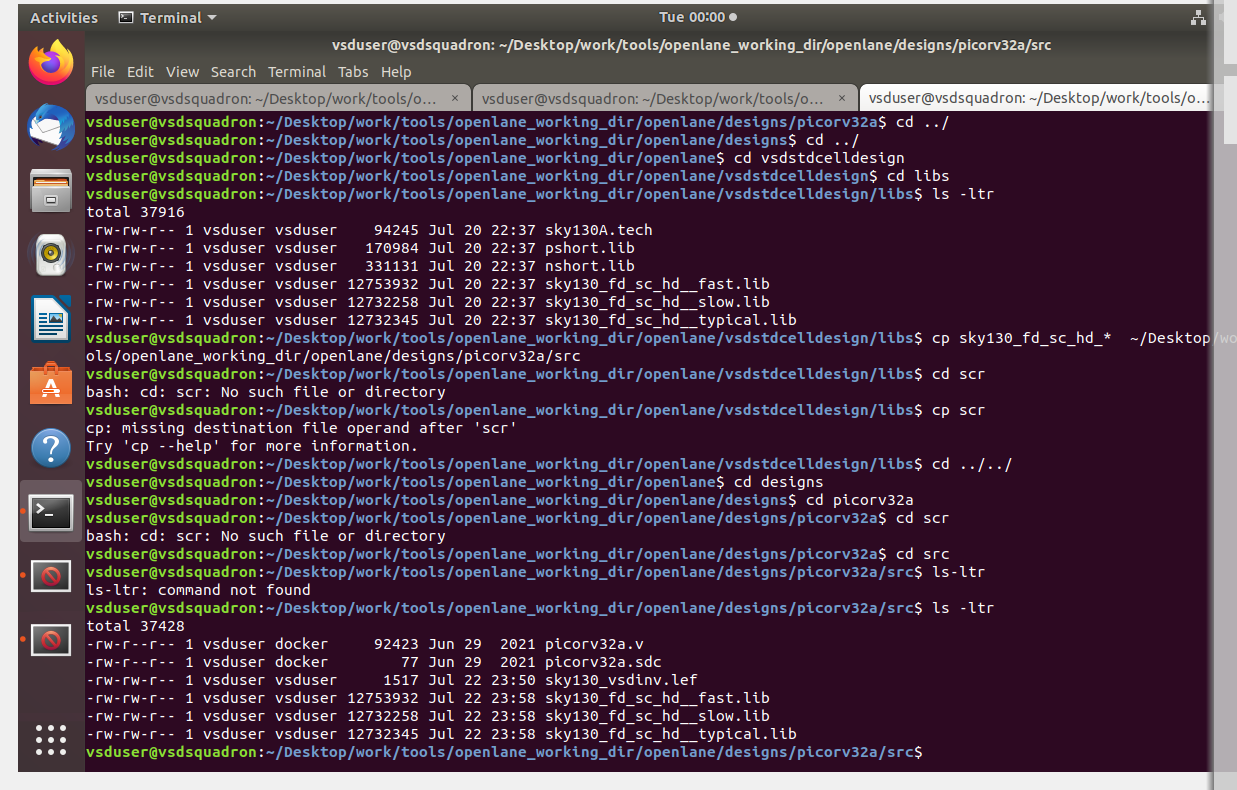
To add extra lef file



1. Segregating all lib files under src

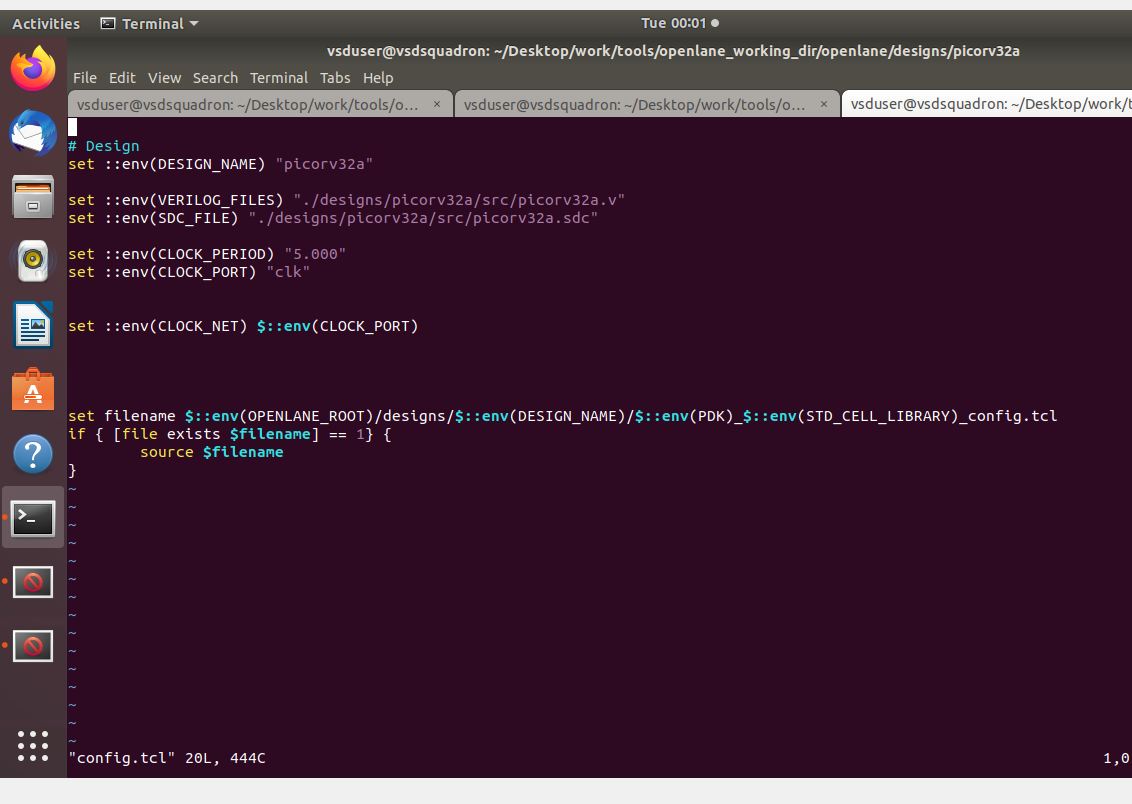


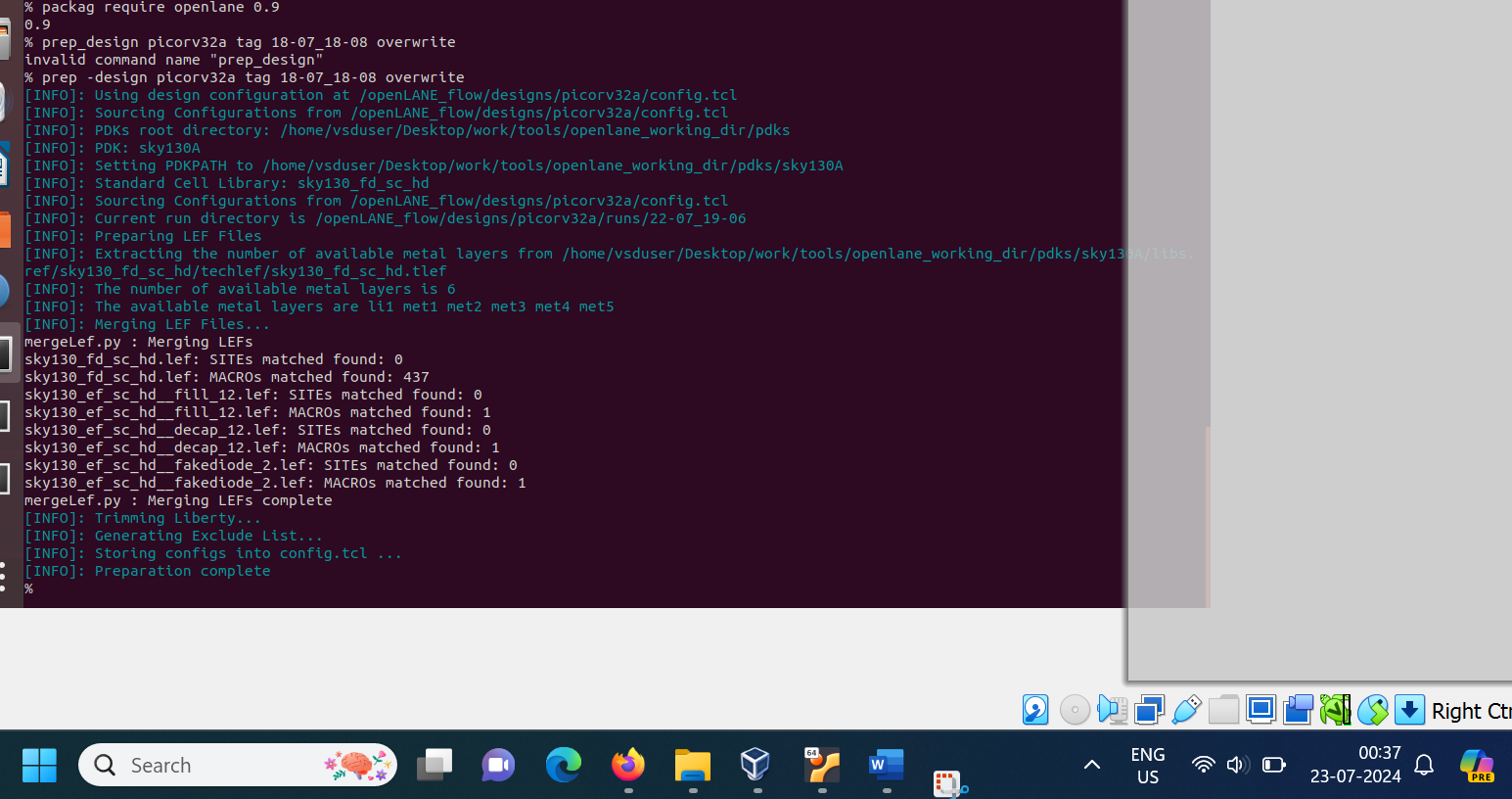
1. Copy the last 3 .lib files to scr



1. Modify the configuration file.

Original config.tcl file



1. % prep -design with recent dir
2. 
3. Synthesis with custom design
4. 