IMPLEMENTATION AND ANALYSIS OF 6-TRANSISTOR SRAM CELL

A PROJECT REPORT
Submitted in partial fulfillment of the requirements
for the award of

BACHELOR OF TECHNOLOGY

in

ELECTRONICS & COMMUNICATION ENGINEERING

by

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Under the Guidance of
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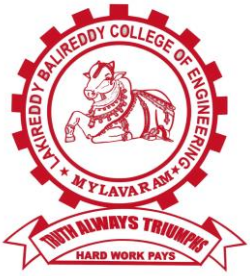

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CERTIFICATE

This is to certify that project work entitled "**IMPLEMENTATION AND ANALYSIS OF 6 -TRANSISTOR SRAM CELL"** is a bonafide work done and submitted by **CH. MALLIKHARJUN REDDY (20761A0476)** in partial fulfillment of requirement for the award of Bachelor of Technology in Electronics and Communication Engineering in Lakireddy Bali Reddy College of Engineering, Mylavaram during the academic year 2023-2024.

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DECLARATION

I hereby declare that the project entitled "**IMPLEMENTATION AND ANALYSIS OF 6-TRANSISTOR SRAM CELL**" submitted for the award of B. Tech. in Electronics and Communication Engineering is our original work and the project has not submitted to any other institution or University for the award of any degree.

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Date:

ACKNOWLEDGEMENT

The Satisfaction that accompanies that the successful completion of any task would be incomplete without the mention of people whose ceaseless co-operation made it possible, whose constant guidance and encouragement crown all efforts with success.

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ABSTRACT

Static Random-Access Memory (SRAM) stands as a vital component, offering swift and efficient on-chip data storage. It is made up of six transistors that are placed in a precise way to achieve stability and the capacity to read and write data. This 6-transistor SRAM cell plays a vital role, particularly in high-performance memory applications like cache memory. The main objective of this project is to focus on examining the performance, stability, and energy efficiency of the 6T SRAM cell. Extensive simulations are helpful to evaluate key performance parameters such as access time, write time, and power consumption. The primary aim is to identify any design limitations or flaws and propose potential enhancements. Factors like noise tolerance, resistance to data corruption during read operations, and ease of writing data should be analysing under different conditions. As power consumption is a critical concern in modern semiconductor devices, we assess the energy efficiency of the 6T SRAM cell. This includes analysing the dynamic power under different operating scenarios. We will analyse its layouts and in addition to characterizing the 6T SRAM cell, we compare its performance and energy efficiency with other popular SRAM cell designs, such as 4T and 8T cells, to identify trade-offs and advantages.

Key Words: Static Random-Access Memory (SRAM), power consumption, layouts, energy efficiency, cache memory.

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CHAPTER – 1

INTRODUCTION

1.1 INTRODUCTION

The 6-transistor (6T) static random-access memory (SRAM) cell is like a tiny storage unit inside computers. It's known for being super reliable and fast, and it's used in all sorts of devices, from your phone to powerful computers. With just six tiny switches called transistors, the 6T SRAM cell can hold onto a piece of information for a long time without needing to refresh it. This little cell is all about speed and reliability. It can quickly fetch and store data, which helps your computer run smoothly and respond fast to the commands. Plus, it doesn't need to constantly check or update its stored information, so it's always ready to go whenever the computer needs it [1][6]. Despite its small size, the 6T SRAM cell packs a punch in terms of efficiency. Designers carefully choose the size of each transistor and how they're arranged to make sure the cell works well while taking up as little space as possible. This means more room for other important stuff on the computer chip and less wasted energy.

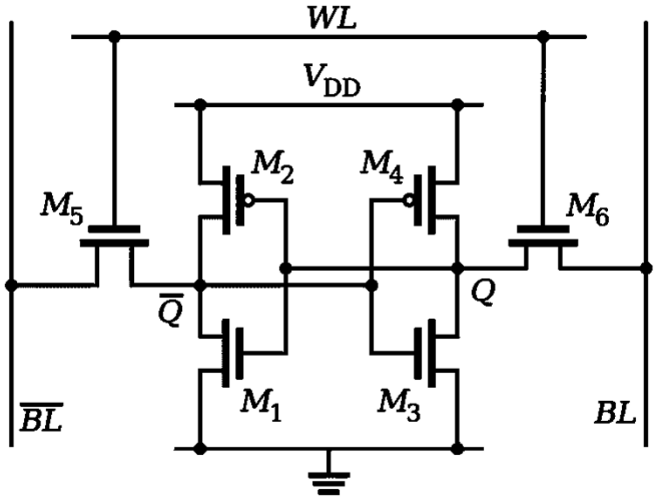

Fig 1.1: 6 Transistor Standard SRAM Cell

In the world of computer memory, the 6T SRAM cell is like a superhero, speeding up the computer and keeping the data safe and ready whenever we need it. It's vital part of making sure the devices run smoothly and quickly, no matter what we are using them for. A 6-transistor (6T) SRAM cell design is a cleverly simple but securely functioning device made up of six metal-oxide-semiconductor field-effect transistors (MOSFETs) placed in a certain arrangement. The two cross-coupled inverters that are joined by two access transistors make up the fundamental components of the 6T SRAM cell as in Fig 1.1. One NMOS (n-channel) and one PMOS (p-channel) complementary MOSFET, coupled in series between the cell's bitline and its complimentary bitline, make up the first inverter. The second inverter is identical to the first. By connecting the output of each inverter to the input of the other, feedback connections allow for cross-coupling and the creation of a latch-like structure. This configuration keeps the SRAM cell in constant logic states ('0' or '1') in the absence of external disturbances, allowing it to store a single bit of data. The access transistors, which usually appear at the top and bottom of the cell, control the data flow between the cell and external circuitry to enable read and write operations. All things considered, the 6T SRAM cell's natural simplicity hides its crucial function in memory systems, offering dependable and quick data storage in a small and effective form. The word line is a control signal that enables the read and write operations by activating the access transistors. When the word line is high, the access transistors connect the cell to the bitlines, allowing data to be read from or written into the cell. Conversely, when the word line is low, the access transistors disconnect the cell from the bitlines, preserving the stored data.

1.2 PROBLEM DEFINITION

The project aims to design a 6-transistor (6T) static random-access memory (SRAM) cell and assess its power consumption, delay characteristics, and area requirements through comprehensive circuit-level simulations and calculations. The 6T SRAM cell, a fundamental building block of memory systems, plays a crucial role in modern computing devices due to its stability and ability to retain data. The project's main components include the design of the 6T SRAM cell, power consumption analysis, delay characterization, and area estimation. In the initial stages

of the project, the focus is on creating a schematic representation of the 6T SRAM cell using industry-standard CAD tools such as Cadence Virtuoso. The schematic design encompasses the arrangement of six MOSFET transistors configured to form two cross-coupled inverters along with access transistors for data read and write operations. This schematic serves as the basis for subsequent layout design.

Following the schematic design, the layout implementation of the 6T SRAM cell is carried out. Layout design involves translating the schematic into a physical representation adhering to layout design rules and optimizing transistor sizes and placement for minimum area occupancy. Layout CAD tools are employed to ensure proper routing and connectivity while minimizing parasitic capacitance and resistance. Various simulation scenarios are considered, including read and write operations under different operating conditions and data access patterns. Additionally, delay characterization is performed to determine the access time, read/write cycle time, and other timing parameters of the 6T SRAM cell. This involves simulating the cell's response to input signals and measuring the propagation delays to assess its performance. Factors such as transistor sizing, and process variations are considered in analysing delay performance.

Simultaneously, the area estimation of the SRAM cell layout is conducted to quantify the silicon area occupied by the design. Layout CAD tools are utilized to extract area metrics and optimize layout parameters for area efficiency while ensuring compliance with design rules and specifications. Throughout the project, careful documentation of the design process, simulation results, and analysis findings is maintained. Final reports detailing power consumption analysis, delay characterization results, and area estimation are prepared, accompanied by recommendations for design optimization to improve power, performance, and area efficiency of the 6T SRAM cell.

1.3 HARDWARE SPECIFICATIONS

The hardware specifications for a 6-transistor (6T) SRAM cell design are crucial for its successful implementation and performance optimization within memory systems. Table. 1.1 shows These specifications encompass several key

aspects that define the characteristics and behavior of the SRAM cell. Firstly, the choice of transistor type (pmos1v and nmos1v) and size (2:1 ratio), typically CMOS technology, along with specific dimensions, influences the cell's footprint on the integrated circuit (IC) chip and its performance. The supply voltage levels must be defined to ensure reliable operation, both under nominal conditions and at maximum allowable levels. In 45 nm technology we use 1.lV supply voltage. Access times for reading and writing data, along with retention time for maintaining stored data integrity, are critical parameters influencing the cell's performance and reliability. Cell density, determined by the number of cells per unit area, impacts memory capacity and chip area utilization. Process technology, such as CMOS (90nm or 45nm) or FinFET, influences transistor performance and overall SRAM cell characteristics. By adhering to these hardware specifications, designers can ensure the successful integration and optimization of 6T SRAM cell designs within memory systems, meeting performance, power, and reliability requirements.

Tabel 1.1: Specifications of The 6 Transistor Sram

SNO	TECHNOLOGY (nm)	VOLTAGE		TRANSISTOR SIZE		SPECIFICATIONS	
1	90	V1(BL)	1.8	ACCESS TRANSISTORS	240n	DC VOLTAGE	1.1 V
						PERIOD	40n s
		V2(BL)	0			DELAY TIME	1p s
						RISE TIME	1p s
		V1(BLB)	0	CROSS CUPLED INVERTERS	120n	FALL TIME	1p s
						PULSE WIDTH	20n s
		V2(BLB)	1.8				
2	45	V1(BL)	1.1	ACCESS TRANSISTORS	240n	DC VOLTAGE	1.1 V
						PERIOD	40n s
		V2(BL)	0			DELAY TIME	1p s
						RISE TIME	1p s
		V1(BLB)	0	CROSS CUPLED INVERTERS	120n	FALL TIME	1p s
		V2(BLB)	1.1			PULSE WIDTH	20n s

1.4 SOFTWARE SPECIFICATION

- **CAD Tool Selection:** Choose appropriate Cadence software tools for schematic design, layout implementation, simulation, and verification. Commonly used tools include Cadence Virtuoso for schematic capture and layout design, Spectre for circuit simulation, and Assura for design rule checking (DRC) and layout versus schematic (LVS) verification.
- **Version Compatibility:** Ensure compatibility between different Cadence software tools and their respective versions to avoid compatibility issues during the design process. Verify that all tools within the Cadence ecosystem are compatible and support seamless data exchange between different stages of the design flow.
- **Design Flow Configuration:** Define the specific design flow configuration within the Cadence environment, including the sequence of design tasks such as schematic design, layout implementation, simulation, and verification. Customize the design flow according to project requirements and design constraints.
- **Library and Component Selection:** Utilize Cadence's extensive library of pre-designed components and standard cell libraries for building blocks such as transistors, inverters, and access transistors. Select appropriate components from the library and ensure compatibility with the chosen process technology.
- **Schematic Design Guidelines:** Follow established schematic design guidelines and best practices for creating the schematic representation of the 6T SRAM cell. Ensure proper transistor connectivity, labelling, and hierarchical organization to facilitate layout implementation and simulation.
- **Layout Design Constraints:** Define layout design constraints such as design rules, routing guidelines, and physical dimensions for the SRAM cell layout. Adhere to foundry-specific design rules and process requirements to ensure manufacturability and reliability of the layout.
- **Simulation Setup:** Configure simulation setups using Cadence Spectre for analyzing the electrical behaviour of the SRAM cell. Define simulation parameters such as operating conditions, stimulus signals, and simulation modes (e.g., transient, DC, AC) to accurately model the cell's performance under different scenarios.

- **Post-simulation Analysis:** Analyse simulation results using Cadence tools for waveform viewing, data extraction, and performance analysis. Extract key performance metrics such as access time, power consumption, and delay characteristics from simulation waveforms for further optimization.
- **Verification and Validation:** Perform design rule checking (DRC) and layout versus schematic (LVS) verification using Cadence Assura to ensure layout correctness and compliance with design rules. Verify the integrity of the layout design and its correspondence with the schematic representation.

1.5 MOTIVATION FOR THE PROJECT

The reason for working on the 6-transistor SRAM cell project could be to make memory storage in electronics better. We want to make accessing data faster, use less power, and make the most of the space on the chip. Also, as technology improves, people want smaller, faster, and more efficient devices, so we're exploring new SRAM designs like the 6-transistor cell. Another reason could be to solve problems with making transistors smaller and reducing power loss in modern technology. Overall, the aim of the project is to create memory solutions that work better and meet the changing needs of different electronic devices.

1.6 OBJECTIVES FOR THE PROJECT

- **Performance Enhancement:** Improve the speed and efficiency of data access and storage operations compared to existing SRAM designs.
- **Power Efficiency:** Reduce power consumption while maintaining reliable operation, making it suitable for energy-efficient devices.
- **Area Optimization:** Minimize the physical footprint of the SRAM cell on the semiconductor chip to maximize integration density.
- **Process Compatibility:** Ensure compatibility with the 45nm CMOS technology node for seamless integration into modern semiconductor manufacturing processes.

CHAPTER – 2

LITERATURE SURVEY

2.1 EXISTING SYSTEM

In the existing system of the 6-transistor SRAM cell, there are two access transistors and one memory unit, which consists of two cross-coupled inverters. All six transistors have the same width, and their total width is 120 nanometers. Table 2.1 focus of the existing system is on power consumption, rise time, and fall time. The power consumption of this system is approximately 30 nanowatts. However, the system does not include the design of layout, area observations, or post-layout simulations for the 6-transistor SRAM cell. It completely concentrates on power consumption and pre-layout simulations [6].

Table 2.1: Power Analysis For Existing 6t Sram Cell In Different Technologies

Technology (nm)	Power (nano watt)
180	519.7
90	59.580
45	30.68

They focused on observing power in Cadence Virtuoso using three different technologies 180nm, 90nm, and 45nm. The power consumption of the 6-transistor SRAM cell was measured with a finger width and the total width of 120 nanometers. In 180nm technology, the power consumption was found to be 519.7 nanowatts. In 90nm technology, it was 59.580 nanowatts, and in 45nm technology, it was 30.68 nano watts.

2.2 LITERATURE SURVEY

M. Ali, A. Jaiswal, S. Kodge, A. Agrawal, I. Chakraborty and K. Roy, "IMAC: In-Memory Multi-Bit Multiplication and Accumulation in 6T SRAM Array," in IEEE Transactions on Circuits and Systems I: Regular Papers, vol. 67, no. 8, pp. 2521-2531, Aug. 2020, doi: 10.1109/TCSI.2020.2981901 [1]. As a revolutionary computing paradigm to alleviate the well-known memory bottleneck, in-memory computing is currently undergoing extensive exploration. With the help of this new paradigm, data will no longer need to be frequently and expensively moved between the compute unit and the storage memory by incorporating some computations inside the memory array. Several memory bit-cells have been used to investigate in-memory computing in relation to silicon memories. Since the six transistor (6T) SRAM array is the most used type of on-chip memory, it is particularly interesting to integrate computation within this architecture. The in-memory multiplication followed by accumulation technique that we offer in this research may perform parallel dot products within 6T SRAM without requiring any modifications to the standard bitcell. We additionally examine how circuit non-idealities and process variances impact the accuracy of the LeNet-5 and VGG neural network architectures, respectively, using the MNIST and CIFAR-10 datasets. Regarding the CIFAR-10 and MNIST, the suggested in-memory dot-product technique achieves 88.8% and 99% accuracy, respectively. The suggested system has a 6.24× improvement in energy usage and a 9.42× improvement in delay when compared to the regular von Neumann system.

G. Torrens, B. Alorda, S. Bota and J. Segura, "Analysis of radiation-hardening techniques for 6T SRAMs with structured layouts," 2009 IEEE International Reliability Physics Symposium, Montreal, QC, Canada, 2009, pp. 791-795, doi: 10.1109/IRPS.2009.5173351 [2]. In order to make 6T SRAM memories compatible with structured architectures, we examine two complimentary radiation-hardening strategies. Choosing the threshold voltage independently for each of the four transistors that make up the cross-coupled inverters of the SRAM cell is one method. An alternative approach involves altering the widths of all PMOS or all NMOS transistors within the cell. This method leaves the cell arrangement unchanged. This second one raises the minimum width of all NMOS by a factor cn and the minimum width of all PMOS by a factor cp. This enables organized layouts by preventing the

creation of diffusion bends. Enhancement of SEU resilience is achieved by both methods.

S. Barua, U. H. Irin, M. M. Azmir, M. M. A. Bappy and S. Alam, "In 12nm FinFET Technology, performance analysis of low power 6T SRAM layout designs with two different topologies," 2022 IEEE 31st Microelectronics Design & Test Symposium (MDTS), Albany, NY, USA, 2022, pp. 1-5, doi: 10.1109/MDTS54894.2022.9826987 [3]. A model for a 6T SRAM cell was built using 12nm FinFET implementation. There are two custom layout bit cell designs created with Cadence Virtuoso software. These two layout models are compared in terms of power consumption, read and write performance, layout space, and stability. Static Noise Margin (SNM) analysis is used to estimate the stability of the SRAM cell. Using these designs, the 16-bit arrays are constructed and the unit layout plans are shown. Relatively speaking, Layout Type 1's unit cell and array have less delay than Layout Type 2 and dissipate the least amount of electricity (9–12%). A bit-cell area drop of about 10% is present in the Layout Type 2 nevertheless. The 6T SRAM cell was designed with Cadence Tool, and 0.8 volts was utilized as the supply voltage for all simulations that used 12nm CMOS technology, Hspice, and Spectre.

Satyanarayana, B.V.M. and Prakash, D.M., 2019. Design, implementation and power analysis of low voltage heterojunction tunnel field effect transistor based basic 6T SRAM Cell. International Journal of Innovative Technology and Exploring Engineering (IJITEE) ISSN., 8(11), pp.2278-3075 [4]. MOSFETs' subthreshold swing and lower than 60 mV/dec for extremely few energy applications restricted the energy process in battery-powered mobile devices. In order to compare the effectiveness of HETT subthreshold swing reduction, prolonged Miller potential, and full-on presence of a mobile electronic device, this research presents the layout and implementation of a MOSFET gate oxide blending on source that can enhance channel tunneling. Utilizing low band offset devices and small power products of metals like Ge or SiGe can improve transistor line by reducing the impact of Miller capacitance. Transistor efficiency features get stronger as a result. NHETT and PHETT production as well as an efficiency study of both NHETT and PHETT are included in the suggested design and implementation of HETT. Regarding the basic and skeleton differences between MOSFET and HETT in order to encourage the use of MOSFET rather than HETT,

the advantages and limitations of NHETT and PHETT have been discussed in detail. While it is appropriate for the MOS technique scheme and suitable for transportable motorized applications, the construction approach used by HETT is by no means unique. A regular SRAM cell was used to examine the output of the 6T SRAM cell electricity evaluation provided by HETT. We acquire and compare the SRAM's average power, maximum power, and minimum power utilizing both MOSFET and HETT. Because there aren't many differences between the mask layers used in HETT and MOSFET manufacturing, HETT fabrication can be facilitated by CMOS MOSFET manufacture. Future applications will combine CMOS MOSFET and HETT technology, using CMOS for digital logic and HETT for semiconductor memory applications.

Y. Hong, Y. Choi and C. Shin, "NCFET-Based 6-T SRAM: Yield Estimation Based on Variation-Aware Sensitivity," in IEEE Journal of the Electron Devices Society, vol. 8, pp. 182-188, 2020, doi: 10.1109/JEDS.2020.2973966 [5]. Sub-threshold slope (SS) <; 60 mV/decade at 300 K is the major characteristic of the negative capacitance field effect transistor (NCFET). The present study examines the switching speed (SS) of the n-type NCFET, which is also known as the pull-down (PD) and passgate (PG) transistor in a six-transistor (6T) SRAM bit-cell. It finds that the SS of the p-type NCFET, which is also known as the pull-up (PU) transistor in the 6T SRAM bit-cell, is 58.96 mV/decade. Metrics measuring read (hold)-stability and write-ability (write-ability current (lw) and read static noise margin (SNM) respectively are used to compare the NCFET-based SRAM cell to the standard SRAM cell using conventional planar bulk MOSFETs. Afterwards, the lw and SNM sensitivities are retrieved under process-induced random variation. Lastly, the cell-sigma method is used to quantitatively assess the yield of NCFET-based SRAM array (in comparison to conventional SRAM array).

Rath, S. and Panda, S., 2017. Analysis of 6T SRAM cell in different technologies. Circulation in Computer Science, pp.7-10. Rath, S. and Panda, S., 2017. An examination of 6T SRAM cells across several technologies [6]. A Journal of Computer Science, Volume 7, Issues 7–10. The study uses the Cadence Virtuoso tool to offer a thorough analysis of a 6T SRAM cell at 180nm, 90nm, and 45nm technology nodes. This encompasses the planning, execution, and assessment of the

SRAM cell's functionality concerning velocity, power consumption, and static noise floor. The data shows how technological scaling results in faster processing, shorter reaction times, and less power use. A significant contribution to our understanding of SRAM cell performance across various technology nodes is made by the paper's discussion of relevant studies in the field.

Shivaprakash, G. and Suresh, D.S., 2016. Design of low power 6T-SRAM cell and analysis for high-speed application. Indian Journal of Science and Technology, 9(46), pp.1-10 [7]. The design and analysis of a low power 6T-SRAM cell employing 90nm technology for high-speed applications are covered in this study. Static Noise Margin, Data Retention Voltage, Read Margin, Write Margin, and other subjects are covered. Graphs and tables illustrating the relationships between different parameters are included. Based on the study's findings, the 6T-SRAM cell's performance may be better understood and a higher Static Noise Margin can be obtained by sacrificing transistor space. There are also references to relevant studies conducted in the topic in the text.

Nigam, A.K., Singh, S. and Tiwari, A., 2015. 6T SRAM Cell: Design and Analysis. Intl J Engg Sci Adv Research, 1(2), pp.27-29 [8]. The performance of a 6T SRAM cell in 45nm and 180nm technologies is thoroughly examined in this work, with particular attention paid to power consumption, latency, and SNM. It gives a thorough description of how the cell works and gives simulation results for both technologies. In the end, the need of balancing various performance metrics is emphasized, and future research possibilities for innovative SRAM cell designs are proposed. A list of references for further reading is also included in the paper.

Lakshmi, T.V. and Kamaraju, M., 2021, February. Implementation of high performance 6T-SRAM cell. In Journal of Physics: Conference Series (Vol. 1804, No. 1, p. 012185) [9]. Publishers IOP. This study covers power reduction strategies in SRAM analysis, low power VLSI circuit design, CMOS integrated circuit design, and cell technology. It evaluates how CMOS, Gated VDD, and MTCMOS approaches affect power consumption and delay performance and focuses on designing a high-performance 6T-SRAM cell with low power VLSI techniques. The findings demonstrate that, although Gated VDD also significantly reduces power consumption,

MTCMOS provides high speed with reduced power usage. According to the study, these techniques can optimize the performance of SRAM cells.

Singh, S., Arora, N., Suthar, M. and Gupta, N., 2012. Performance evaluation of different SRAM cell structures at different technologies. International Journal of VLSI Design and Communication Systems, 3(1), p.97 [10]. This research investigates the usage of static random-access memory (SRAM) and the need for low-power devices in VLSI circuits. After comparing the performance of several SRAM cell structures at various technological nodes, it is discovered that the 10T SRAM cell at 32nm and the 10T Modified SRAM cell at 90nm and 45nm exhibit better speed and power consumption. These findings were obtained by the investigation using Tanner EDA tool simulation.

Balanarasimhulu, P. and Reddy, G.K., 2014. A Comparative Analysis of 6 Transistor SRAM and 6T ROM Embedded SRAM [11]. In order to compare power consumption, the article compares several SRAM cell architectures, such as 6T SRAM, 6T RSRAM, and 8T RSRAM. To mitigate write stability difficulties, it presents an 8T ROM Embedded SRAM design and provides improved ROM embedded SRAM cells with the goal of lowering power consumption and space. A list of relevant scholarly works is provided in the paper, and the simulations are carried out with LT SPICE software.

Adiseshaiah, M., Rao, D.S.B. and Reddy, V.V.T., 2012. Implementation and desing of 6T-SRAM with read and write assists circuits. International Journal of Research in Engineering & Applied Sciences, 2, pp.36-50 [12]. The paper presents a comparison of 65nm technology with 120nm technology, as well as the development of read and write assist circuits for SRAM cells. This section covers 32-bit SRAM power dissipation, circuit layouts, schematics, and simulation results. The effectiveness of the assist circuitry in controlling power dissipation is examined, along with issues like power savings and challenges in VLSI circuit design. The architecture and components of the SRAM chip are detailed in depth, along with the operation of the NOR decoder and the behavior of the SRAM cell in the event of a read failure. Conclusion of the paper includes references and future scope of the project.

Khan, Q.M., Perdriau, R., Ramdani, M. and Koohestani, M., 2022. A comparative performance analysis of 6T and 9T SRAM integrated circuits: SOI vs. bulk. IEEE Letters on Electromagnetic Compatibility Practice and Applications, 4(2), pp.25-30 [13]. In silicon-on-insulator (SOI) and bulk CMOS technologies, the research compares the performance of 6T and 9T static random access memory (SRAM) cells. Resilience to process and temperature fluctuations, power metrics, and data stability are assessed. According to the findings, SRAM cells built using SOI had better data stability, less write ability, less leakage current, less static power dissipation, increased sensitivity to process changes, and increased resistance to temperature variations when compared to bulk technology. For the design and application of SRAM cells in various technologies, the study offers insightful information.

Mishra, V.K. and Chauhan, R.K., 2018. Efficient layout design of junction less transistor based 6-T SRAM cell using SOI technology. ECS Journal of Solid State Science and Technology, 7(9), p.P456 [14]. This paper uses a Junctionless SOI MOS transistor to propose a unique 6-T SRAM configuration. Reducing the device's space consumption is the main concept behind the suggested structure, which aims to enhance its functionality. When compared to double gate junctionless transistors reported in the literature, the junctionless SOI n- and p-MOS transistor shows higher Ion to Ioff ratio and lower off-state current. In the suggested 6-T SRAM cell layout construction, a latch circuit was first set up, and then a compact SRAM layout configuration was created by cascading two n-transistors back-to-back. Consequently, the area used by the suggested construction is almost half that of the traditional junctionless 6-T SRAM layout. The read/write delay time is also improved in the suggested architecture. Using Sentaurus and the Cogenda device simulator, the suggested structures were created and simulated.

Jain, S., 2023. A Survey on Layout Implementation and Analysis of Different SRAM Cell Topologies. International Journal of Advanced Computer Technology, 12(1), pp.6-10 [15]. The main objective of electronics is to produce low-power devices because powered widgets are widely used. Memory cell design is now heavily interested in memory cell functioning with low voltage consumption due to its potential in low-energy computing. The only essential component for the success of

low-voltage SRAM design is the steady operation of SRAM due to specification changes in scaled approaches. Although it offers quick and high-density differential sensing, the conventional SRAM cell has read-risk and semi-selective problems. According to the simulation findings, the suggested design offers the fastest read operation and optimizes the power delay product overall. While the reading disruption problem can be resolved with a typical SRAM cell in comparison to the present topologies of 6T, 8T, and 10T, earlier approaches to address these issues have failed because of low efficiency, data-dependent leakage, and excessive energy consumption per connection. Reducing the space and power of the proposed design cell work, as well as improving read performance, are our main objectives. The micro-wind tool has been used to implement the suggested leakage reduction design circuit. The performance of memory cells is significantly influenced by delay and power consumption. The development of a low-power SRAM cell is the main objective of this project.

M Praveen, K.N. and Shivaleelavathi, B.G., 2015. SRAM Memory Layout Design in 180nm Technology. International Journal of Engineering Research & Technology (IJERT), 4(8) [16]. This article describes a complete custom memory layout design for a 1KB SRAM, together with physical verification checks (DRC and LVS) to confirm the implemented layouts. The layout design techniques, which include symmetry, half-cell, device matching, and route matching, have all been meticulously adhered to. CADENCE EDA was utilized to implement the layouts, while the Virtuoso platform was employed for the design of the schematic and layout. To validate the layout designs, the Assura physical verification environment was utilized. The gpdk 180nm and 45nm technology nodes are utilized. It was successful to develop the entire bespoke layout of the 1KB SRAM architecture.

Gupta, R. and Gill, S.S., 2022. AN EFFICIENT NOVEL 6T SRAM CELL WITH OPTIMIZED LAYOUT AND DESIGN METRICS IN 45NM TECHNOLOGY. ICTACT Journal on Microelectronics, 8(2), pp. 1350-1357 [17]. The quick performance, high density, and low power consumption of a unique 6T SRAM (Static Random Access Memory) cell are proposed in this work. The features of the transmission gate transistor for a quick and power-efficient structure and the feedback cutting transistor for effective and stable bit storage have been fully utilized

in the suggested arrangement. The inclusion of more PMOS (P-Channel Metal-Oxide Semiconductor) transistors than NMOS (N-Channel Metal-Oxide Semiconductor) transistors in the suggested configuration results in a somewhat more area-efficient construction without compromising performance. Effective circuit design has been proven to be significantly impacted by the appropriate management of transistor blocks. Compared to the typical 6T cell and earlier configurations, the SRAM cell that is being shown uses less power, is faster, and requires comparatively less read and write time. The data fragments within the cell are stable and effectively stored. Compared to the conventional 6T SRAM construction, the new SRAM cell is 24.17% more compact. Comparing the suggested cell to similar recent research that included more expensive and sophisticated technologies like FINFETs (Fin Field-Effect Transistor), simulation results show that the suggested cell has significantly improved performance characteristics such as reduction in leakage current, power consumption, and delay (range of 8.66% to 77.7%). With the Cadence Virtuoso tool, the suggested 6T structure is simulated in a 45nm technology node.

Sharma, N., 2015. Comparative analysis of power reduction in SRAM 6T and 4T. IJARSE, 4(1), pp.1325-1334 [18]. Scaling SRAM is limited by intrinsic fluctuations and difficult leakage control in today's bulk-Si MOSFETs. This study presents design tradeoffs for four- and six-transistor (4-T) SRAM cells. Significant improvements in the cell static noise margin (SNM) without area penalty are achieved by 6-T and 4-T FinFET-based SRAM cells constructed with built-in feedback. Six-T FinFET based SRAM cells can produce up to a 2-fold improvement in SNM. SRAM cells based on 4-T FinFETs with integrated feedback are appealing for low-power, low-voltage applications because they can achieve sub-100pA standby current per cell and provide comparable improvements in SNM to 6-T cells with feedback.

Ezeogu, A., 2019. Performance Analysis of 6T and 9T SRAM. arXiv preprint arXiv:1905.08624 [19]. In order to assess stability, leakage, and process changes, this study analyzes the performance of 6T and 9T SRAM memory cells in 45nm CMOS technology. It presents the N-curve metric for measuring stability and shows that, in comparison to the 6T SRAM design, the 9T SRAM design has stronger immunity to process fluctuations, lower leakage, and higher stability. The article contains links to

relevant research as well as simulation data for write ability, read stability, and static noise margin.

2.3 PROPOSED SYSTEM

The proposed system of the 6-transistor SRAM is like the existing one, comprising 6 transistors. We modified the finger width and total width of the 6-transistor SRAM transistors in a 2:1 ratio to reduce power consumption. We ensured that the width of access transistors is greater than that of the inner memory unit. To analyse pre-layout simulations, we additionally designed a sense amplifier to observe the outputs of BL and BLB. We added precharged capacitors to enhance read and write operations. Our focus is on the output graphs, both pre-layout and post-layout simulations, overall power consumption of the 6-transistor SRAM cell, propagation delay from input to output, analysis of parameters, and temperature's influence on SRAM performance. We are also considering layout design and area optimization. Initially we planned to design one bit SRAM and then move on to the 16-bit SRAM cell. The proposed SRAM system will decrease the power consumption of the circuit.

2.4 FEASIBILITY STUDY

The proposed project plan for the design and implementation of a 6-transistor SRAM (6T SRAM) cell begins with project initiation, where objectives, scope, and team roles are defined. Following this, the research phase involves gathering requirements and conducting a literature review on 6T SRAM design principles. In the schematic design phase, the 6T SRAM cell is represented schematically, ensuring the arrangement of six MOSFET transistors and access transistors for read/write operations. This schematic serves as the basis for the layout design phase, where the physical layout is created, adhering to design rules, and optimizing for minimum area occupancy. Subsequently, in the simulation and analysis phase, various scenarios are simulated to evaluate performance, power consumption, and timing parameters under different conditions. The validation and verification phase involves rigorous testing to ensure compliance with design specifications and performance requirements. Documentation and reporting are integral throughout the project, ensuring clear documentation of the design process, simulation results, and analysis findings.

Finally, presentation, review, closure, and post-project evaluation complete the project lifecycle, ensuring successful completion and incorporation of lessons learned for future projects.

2.4.1 APPLICATIONS

- **Microprocessors and Microcontrollers:** 6T SRAM cells are commonly used as cache memory in microprocessors and microcontrollers. They provide fast access times and low power consumption, making them ideal for storing frequently accessed data and instructions.
- **Embedded Systems:** Embedded systems often require fast, reliable memory for data storage and processing. 6T SRAM cells are well-suited for use in embedded systems due to their low latency and high-speed operation, making them suitable for tasks such as buffering, caching, and data storage.
- **Graphics Processing Units (GPUS):** GPUs require fast and efficient memory to handle large amounts of data in real-time graphics rendering and processing tasks. 6T SRAM cells can be used in GPU memory subsystems to provide high-speed access to texture data, frame buffers, and other graphics-related data.
- **Networking Equipment:** Networking devices such as routers, switches, and network processors require fast memory to handle packet processing and routing tasks. 6T SRAM cells are commonly used in these devices to store routing tables, packet headers, and other critical networking data.
- **Consumer Electronics:** Consumer electronics devices such as smartphones, tablets, and digital cameras rely on fast and energy-efficient memory for storing and accessing user data. 6T SRAM cells can be found in these devices' memory subsystems, providing high-speed access to frequently accessed data and improving overall performance.
- **Automotive Electronics:** In automotive applications, 6T SRAM cells are used in electronic control units (ECUs), infotainment systems, and advanced driver-assistance systems (ADAS). They provide fast and reliable memory for storing sensor data, control algorithms, and other critical information used in automotive applications.

- **Medical Devices:** Medical devices such as implantable devices, patient monitors, and diagnostic equipment require fast and reliable memory for storing patient data and processing sensor readings. 6T SRAM cells are well-suited for these applications due to their low power consumption and high reliability.
- **Aerospace And Defense:** Aerospace and defense systems require rugged and reliable memory solutions for mission-critical applications such as avionics, guidance systems, and radar systems. 6T SRAM cells can withstand harsh environmental conditions and provide fast access to data in these demanding applications.

2.4.2 ADVANTAGES

- **High Speed:** 6T SRAM cells provide fast read and write access times, making them suitable for applications requiring quick data retrieval and processing. The symmetrically designed cross-coupled inverters enable rapid switching between memory states, resulting in high-speed operation.
- **Low Power Consumption:** Compared to other memory technologies like DRAM (Dynamic Random-Access Memory), 6T SRAM cells consume less power during standby and active modes. This low-power characteristic makes them ideal for battery-powered devices and energy-efficient electronics, helping to extend battery life.
- **Non-Volatile Storage:** 6T SRAM cells are non-volatile, meaning they retain stored data even when power is removed. This property eliminates the need for constant power supply to maintain data integrity, making them suitable for applications requiring persistent memory storage.
- **High Reliability:** The stable latch-based storage mechanism of 6T SRAM cells ensures robust and reliable data retention. They are less susceptible to data loss due to disturbances such as noise, making them suitable for critical applications where data integrity is paramount.
- **Ease Of Integration:** 6T SRAM cells are relatively easy to integrate into integrated circuit designs due to their simple structure and standard CMOS fabrication process compatibility. They can be seamlessly integrated with other circuit components, facilitating the design of complex integrated systems.

- **Reduced Refresh Overhead:** Unlike DRAM, which requires periodic refresh cycles to maintain data integrity, 6T SRAM cells do not require refresh operations. This reduces the overhead associated with memory management and simplifies system design.
- **High Density:** 6T SRAM cells can achieve high memory density within a small footprint on the integrated circuit layout. This high-density characteristic makes them suitable for applications requiring large memory arrays while conserving silicon area.
- **Improved Noise Immunity:** The differential nature of the read and write operations in 6T SRAM cells provides inherent noise immunity, enabling reliable operation in noisy environments or applications with high electromagnetic interference (EMI).

2.4.3 DISADVANTAGES

- **High Area Requirement:** Compared to other memory technologies like DRAM (Dynamic Random-Access Memory), 6T SRAM cells require a relatively large silicon area per cell. This can limit their use in applications where space is a constraint, especially in large memory arrays.
- **Complexity Of Design:** Designing and optimizing a 6T SRAM cell requires careful consideration of various parameters such as transistor sizes, layout, and operating conditions. Achieving optimal performance while minimizing area and power consumption can be challenging and may require sophisticated design techniques.
- **Power Consumption In Standby Mode:** While 6T SRAM cells consume less power during active operation compared to DRAM, they still consume power in standby mode to maintain data integrity. This standby power consumption can be significant in applications where power efficiency is critical, such as battery-powered devices.
- **Susceptibility To Process Variations:** 6T SRAM cells are sensitive to process variations during fabrication, which can result in variations in performance and reliability across different devices. This sensitivity to process variations may

require additional design margins or calibration techniques to ensure consistent operation.

- **Limited Scalability:** As semiconductor technology advances and feature sizes shrink, the scalability of 6T SRAM cells becomes increasingly challenging. Achieving higher densities while maintaining performance and reliability becomes more difficult as feature sizes approach physical limits.
- **Read And Write Disturbances:** 6T SRAM cells are susceptible to read and write disturbances, where accessing one cell can unintentionally affect neighboring cells due to coupling effects. This can lead to data corruption and reliability issues, especially in high-density memory arrays.
- **Higher Manufacturing Cost:** Fabricating integrated circuits with 6T SRAM cells can be more expensive compared to alternative memory technologies, primarily due to the larger silicon area requirement and complexity of the manufacturing process.
- **Limited Retention Time:** While 6T SRAM cells are non-volatile and do not require periodic refresh cycles like DRAM, they may still have limited retention time for storing data without power. Retention time can degrade over time due to factors such as leakage currents and radiation effects, potentially leading to data loss in long-term storage applications.

CHAPTER – 3

SYSTEM ANALYSIS & DESIGN METHODOLOGY

3.1 REQUIREMENT SPECIFICATION

3.1.1 FUNCTIONAL REQUIREMENTS

- **Data Storage:** The SRAM cell must be capable of storing one bit of binary data reliably.
- **Read And Write Operations:** It should support read and write operations to retrieve and modify stored data.
- **Stability:** The cell must maintain the stored data indefinitely as long as power is supplied to the system.

3.1.2 PERFORMANCE REQUIREMENTS

- **Access Time:** The SRAM cell should provide fast access times for both read and write operations to ensure efficient data retrieval and storage.
- **Delay Characteristics:** It must exhibit minimal propagation delay and latency to enable high-speed operation within the memory system.
- **Power Consumption:** The SRAM cell should consume minimal power during standby mode and low-power operation to optimize energy efficiency.

3.1.3 ELECTRICAL SPECIFICATIONS

- **Operating Voltage:** Specify the required voltage levels for proper operation of the SRAM cell.
- **Power Supply Current:** Define the maximum and typical current consumption of the SRAM cell under various operating conditions.
- **Signal Levels:** Specify the voltage levels for logic high and logic low states, ensuring compatibility with system-level interfaces.

3.1.4 PHYSICAL REQUIREMENTS

- **Layout Area:** Define the allowable footprint for the SRAM cell layout on the integrated circuit (IC) chip, considering area constraints and chip density.
- **Transistor Sizes:** Specify the sizes of individual transistors within the SRAM cell layout to achieve desired performance and area efficiency.
- **Interconnect Density:** Define routing and interconnect requirements to minimize parasitic effects and optimize signal integrity.

3.1.5 MANUFACTURING AND PROCESS REQUIREMENTS

- **Process Technology:** Specify the semiconductor fabrication process technology (e.g., CMOS, FinFET) used for manufacturing the SRAM cell.
- **Design Rules:** Define design rules and constraints imposed by the chosen process technology to ensure manufacturability and yield.

3.1.6 COMPATIBILITY AND INTERFACE REQUIREMENTS

- **System Interface:** Specify compatibility requirements with system-level interfaces and protocols for seamless integration into memory subsystems.
- **Pin Configuration:** Define the pinout and interface configuration of the SRAM cell for connection to external circuits and devices.

3.2 FLOWCHARTS

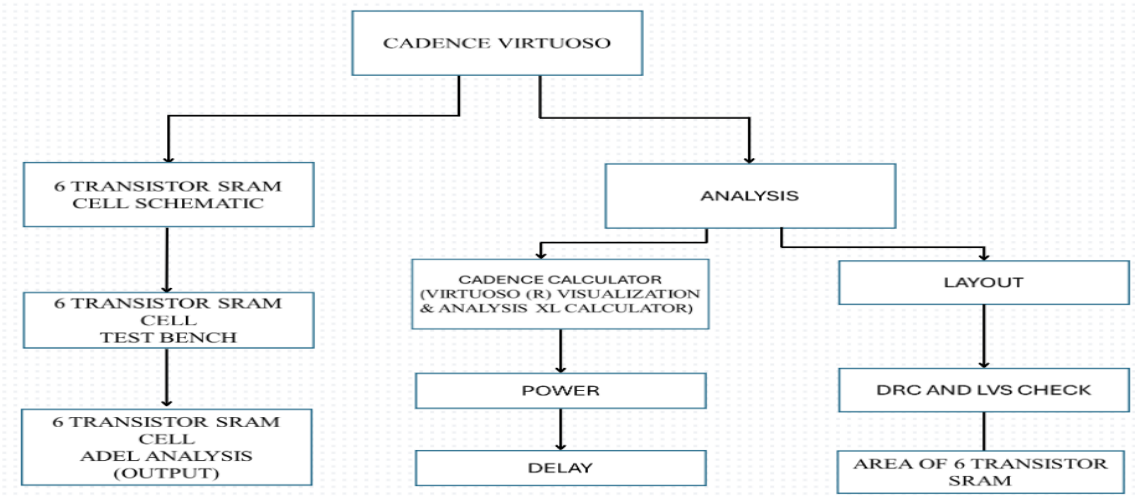

Fig 3.1: Flow Diagram of Cadence Tool

3.2.1 SCHEMATIC CAPTURE

- Launch Cadence Virtuoso and create a new design library and cell view.
- Draw the schematic of the 6T SRAM cell using MOSFET transistors and interconnections.
- Ensure proper connectivity between transistors, including cross-coupled inverters and access transistors.
- Verify the schematic for correctness and completeness, addressing any errors or warnings.

3.2.2 TEST BENCH

- **Test Bench Architecture:** Define the overall architecture of the test bench, including the test stimulus generation, data monitoring, and verification components.
- **Test Vector Generation:** Develop a test vector generator to create input stimuli for the SRAM cell. This can involve generating random or predefined sequences of read and write operations to exercise different memory states.
- **Error Detection and Reporting:** Implement error detection mechanisms to identify discrepancies between expected and observed data. Generate test bench reports summarizing simulation results and highlighting any detected errors or failures.
- **Debugging and Optimization:** Debug any issues identified during simulation by analyzing waveforms, adjusting test vectors, or modifying the test bench setup. Optimize the test bench configuration and test vectors to improve coverage and efficiency of the test process.

3.2.3 ADEL VERIFICATION IN CADENCE

- **Setup Adel Environment:** Launch the Cadence Virtuoso layout and schematic editor and ensure that the Adel environment is set up and accessible. You may need to configure the ADE window to include Adel commands and tools.
- **Simulation Setup:** Within your Adel scripts, configure simulation setups using commands to specify simulation types (e.g., transient, AC, DC), simulation

parameters (e.g., time step, stop time), and analysis types (e.g., waveform, operating point).

- **Test Stimuli Generation:** Define test stimuli for your analog or mixed-signal circuits using Adel commands. This may involve generating input waveforms, setting initial conditions, or applying stimulus sources to circuit elements.
- **Results Analysis:** After simulation completion, use Adel commands to analyze simulation results. This may involve plotting waveforms, extracting data from simulation outputs, performing statistical analysis, or comparing simulation results against expected behavior.

3.2.4 LAYOUT IMPLEMENTATION

- Generate a layout view for the SRAM cell based on the schematic design.
- Place and route the MOSFET transistors according to layout design rules and guidelines.
- Optimize transistor sizes, spacing, and routing to minimize area and parasitic effects.
- Ensure proper alignment and symmetry of the layout components for optimal performance.
- Perform layout verification checks, including design rule checking (DRC) and layout versus schematic (LVS) verification.

3.2.5 SIMULATION SETUP

- Configure simulation environments using Cadence Spectre for electrical characterization.
- Define simulation parameters such as operating conditions, input signals, and analysis types.
- Simulate the SRAM cell for read and write operations, verifying functionality and performance.
- Analyse simulation results to extract key metrics such as access time, power consumption, and delay characteristics.

3.2.6 POST-SIMULATION ANALYSIS

- Analyse post-simulation waveforms and data to verify design functionality and performance.
- Evaluate power consumption, delay characteristics, and other key metrics against design requirements.
- Identify areas for further optimization or refinement based on simulation results and analysis.
- **Specification Gathering:** Define the requirements and specifications of the 6T SRAM cell, including functionality, performance, and electrical characteristics.

3.3 DESIGN AND TEST STEPS

3.3.1 SCHEMATIC DESIGN

- Use Cadence Virtuoso or a similar tool to create a schematic representation of the 6T SRAM cell.
- Design the cross-coupled inverters and access transistors based on the cell's functionality requirements.

3.3.2 LAYOUT IMPLEMENTATION

- Translate the schematic design into a physical layout using layout design tools.
- Optimize transistor placement and routing to minimize area and parasitic effects.

3.3.3 DRC AND LVS CHECKS

- Perform design rule checks (DRC) and layout versus schematic (LVS) verification to ensure layout correctness and compliance with design rules.

3.3.4 SIMULATION SETUP

- Configure simulation setups using Cadence Spectre or similar tools.
- Define simulation parameters such as operating conditions, input stimuli, and analysis types.

3.3.5 PERFORMANCE CHARACTERIZATION

- Conduct simulations to characterize the performance of the SRAM cell.

3.3.6 POWER CONSUMPTION ANALYSIS

- Evaluate power efficiency under different operating scenarios.

3.3.7 AREA ESTIMATION

- Extract layout metrics and analyse area utilization of the SRAM cell layout.
- Optimize layout parameters for area efficiency while ensuring compliance with design rules.

3.4 TESTING PROCESS

After designing the test bench and verifying it, we launch Adel for output analysis in terms of graphs, power, and delay. First, we open the Adel window and select outputs from the test bench design. Then, we analyse and set the transient simulation stop time to 200 nanoseconds and check the "conservative" option before applying the settings shown in Fig 3.2. Next, we set the model library by going to setup, selecting "model library," and choosing the technology as gpdk45, then saving the settings shown in Fig 3.4.

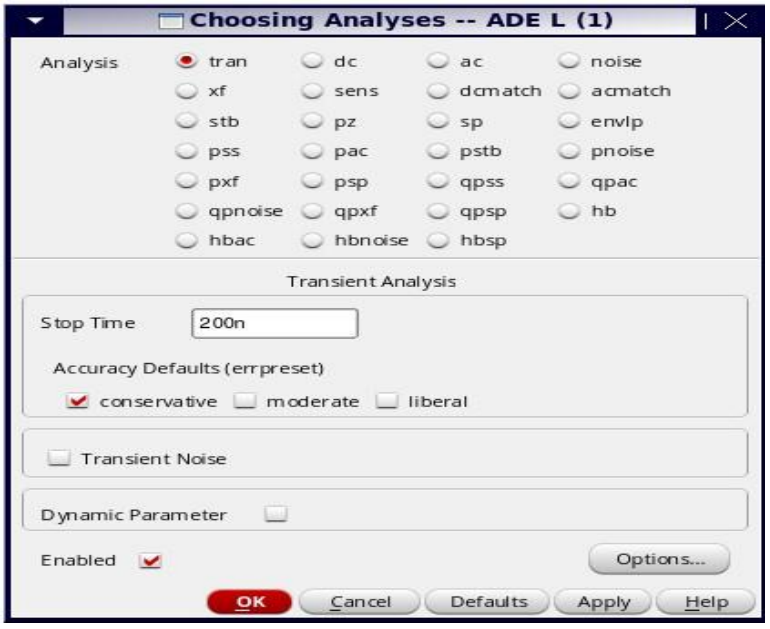

Fig 3.2: Choising Analysis

To obtain the power of the 6-transistor SRAM, we use a calculator. We navigate to the outputs in the Adel window, choose "save all," and in the Save Options dialog box, select "all" for output signals and "all" for power signals before saving and applying the settings shown in fig 3.3.

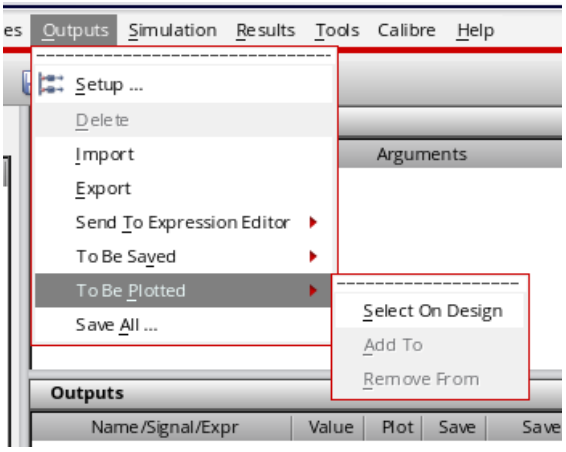

Fig 3.3: Outputs Selection

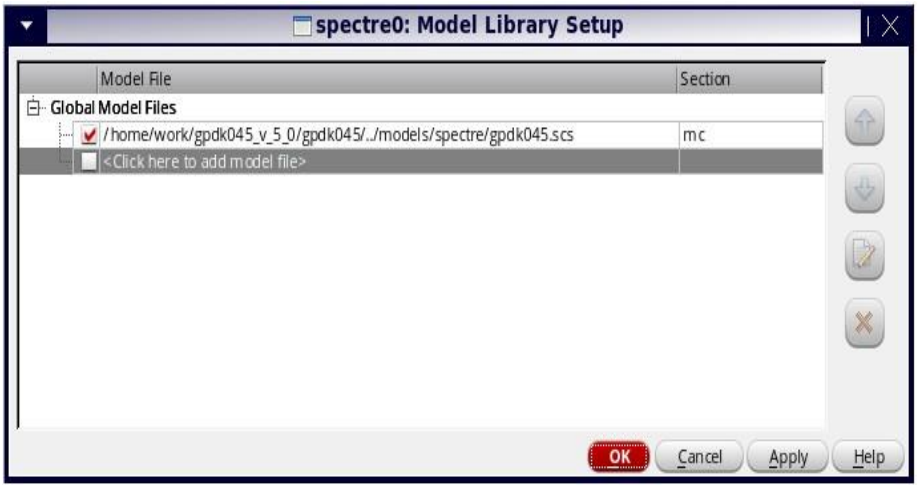

Fig 3.4: Model Library Setup

We run the simulation again in Adel and go to the results option in the browser. Then, we pulse the PSF, select "pwr" (power), and choose the power output in the results. For delay analysis, we select the delay option in the special functions, choose "signal1" (input) and "signal2" (output), and add the threshold values as half of the input voltage. After applying the settings, we use the Cadence calculator, select the average function in the special functions, and choose the Excel option for further analysis.

CHAPTER – 4

IMPLEMENTATION

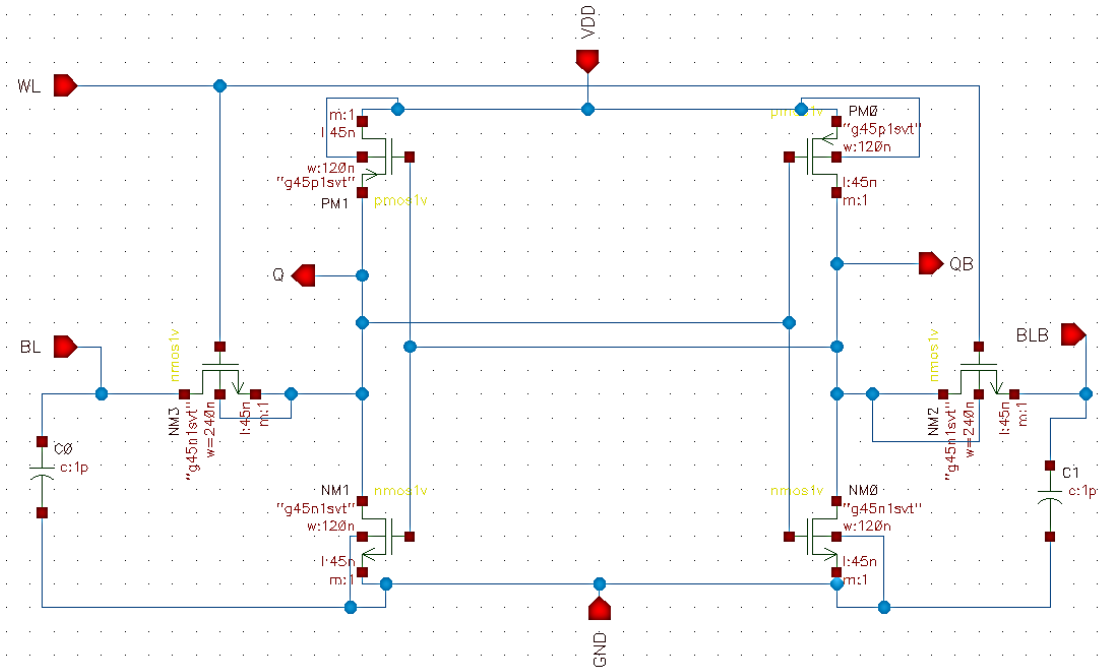

Fig 4.1: Schematic Of 6 Transistor SRAM

To implement the 6-transistor SRAM cell, we need the Cadence tool for designing the schematic and test bench. Initially, we create a library and attach it to the existing gpdk45 library, which is the 45nm technology library. Then, we create the cell view to design the schematic of the 6T SRAM shown in Fig 4.1.

Firstly, we launch an instance and access the gpdk45 library to select PMOS and NMOS transistors with a width of 120 nanometers. We place these transistors according to our proposed design of the 6T cell. Then, we create ports for inputs and outputs, naming them as BL, BLB, WL, VDD, and GND for inputs, and Q and QB for outputs. Precharged capacitors are placed on BL and BLB.

After placing all components, we connect them according to the proposed design. The memory unit, which stores data, consists of two inverters cross-coupled together. The input of the first inverter connects to the output of the second inverter, creating a feedback loop to store data during read and write operations.

Two access transistors, with a width of 240 nanometers, act as inputs during write operations and outputs during read operations. They are connected to WL, BL, and BLB for read and write operations. WL controls the access transistors if WL is 1, both access transistors are on, allowing access to BL and BLB for reading or writing data. If WL is 0, both access transistors are off, and the memory remains in a hold state.

VDD and GND connections are also established. After schematic checking, we create a symbol for the schematic to facilitate connections in the test bench shown in Fig 4.2. In the test bench, inputs such as BL (pulse), BLB (pulse), WL (DC power), VDD (DC power supply), and GND are provided, with ports created for outputs Q and QB shown in Fig 4.3 and Table 4.1.

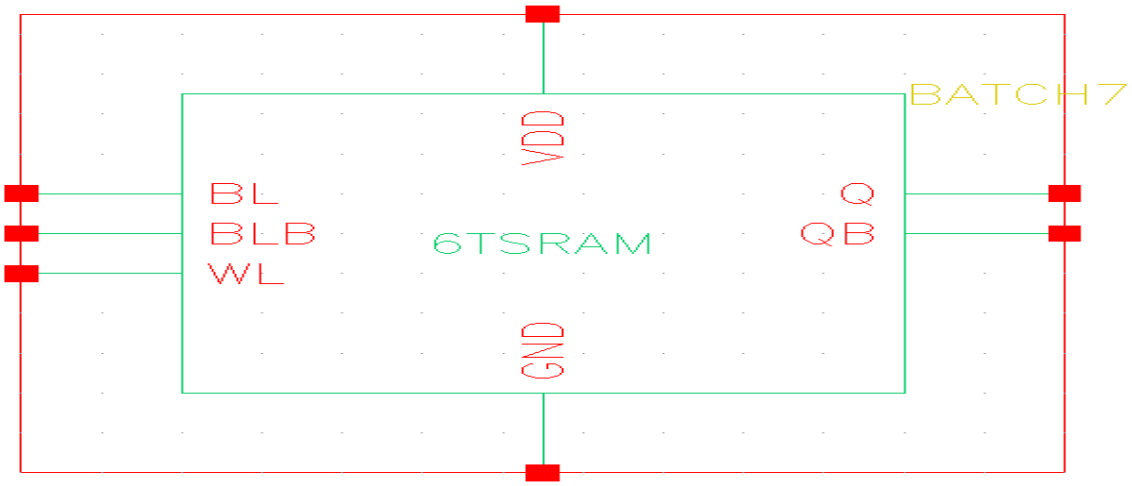

Fig 4.2: Symbol of 6 Transistor SRAM

For the pulse generator, we assign DC voltages and set parameters for BL and BLB. After configuring all details, we launch the Adel window for verification purposes. Post pre-layout simulations, we move on to layout designing.

In the layout design stage, we go from schematic to layout XL for designing. Connectivity is generated from the source with a minimum separation of 0.12, and routing is done accordingly. After completing layout designing, we move to Assura for DRC and LVS checks. To find the area of the layout, we select the PR boundary and access properties.

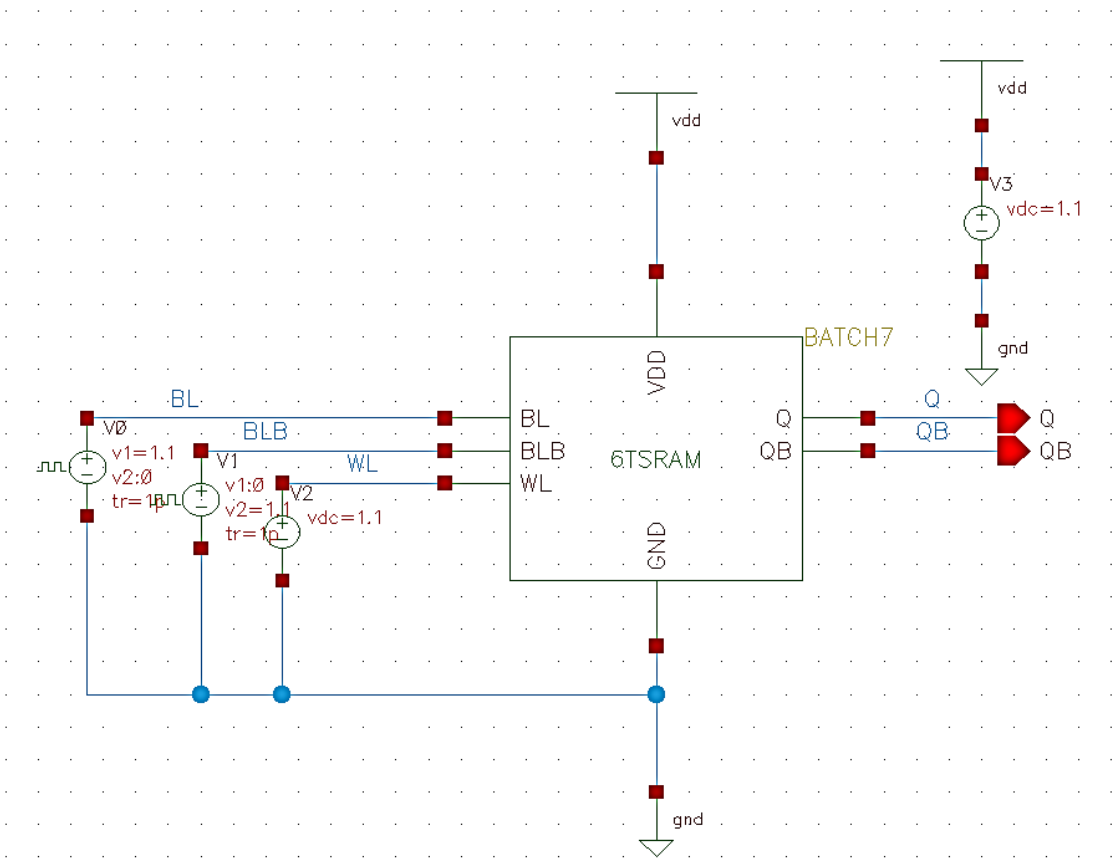

Fig 4.3: Test Bench For 6 Transistor Sram Schematic

The schematic can be represented with the two NOT gates acting as the memory unit shown in Fig 4.4. The inverter is essentially a NOT gate, so we can replace the two cross-coupled inverters with the NOT gates that invert the inputs.

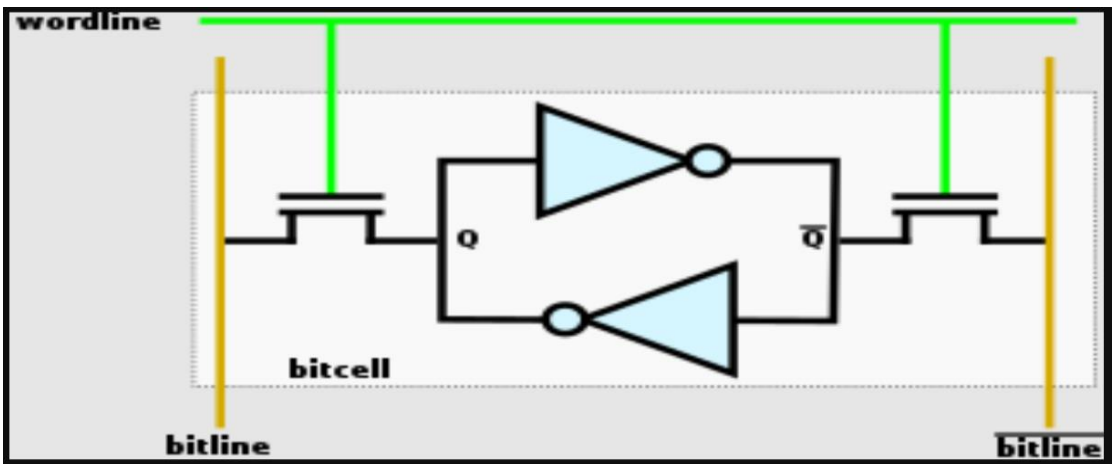

Fig 4.4: Simplified Version Of 6 Transistor Sram Schematic

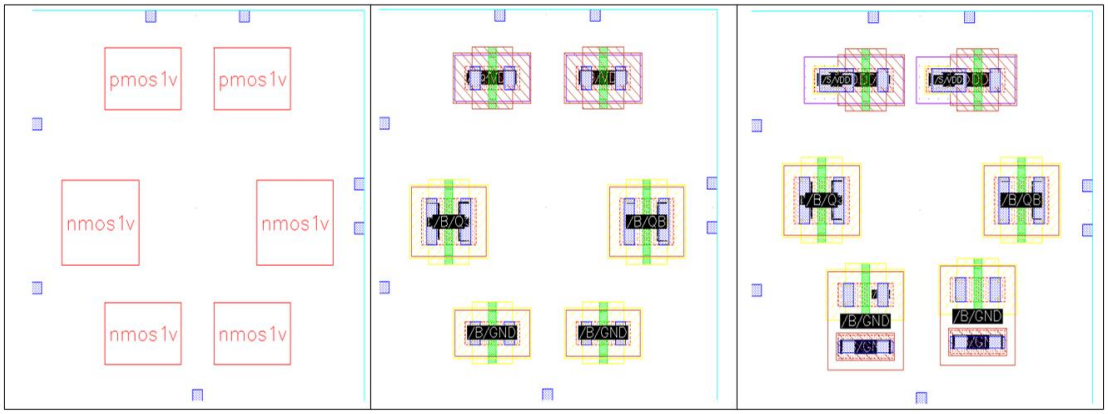

Fig 4.5: Blocks Of 6t SRAM Layout

After the pre-layout simulations, we proceed to post-layout by designing the layout in Layout XL shown in Fig 4.5 and Fig 4.6. Subsequently, we obtain the area for the layout design of the 6-transistor SRAM.

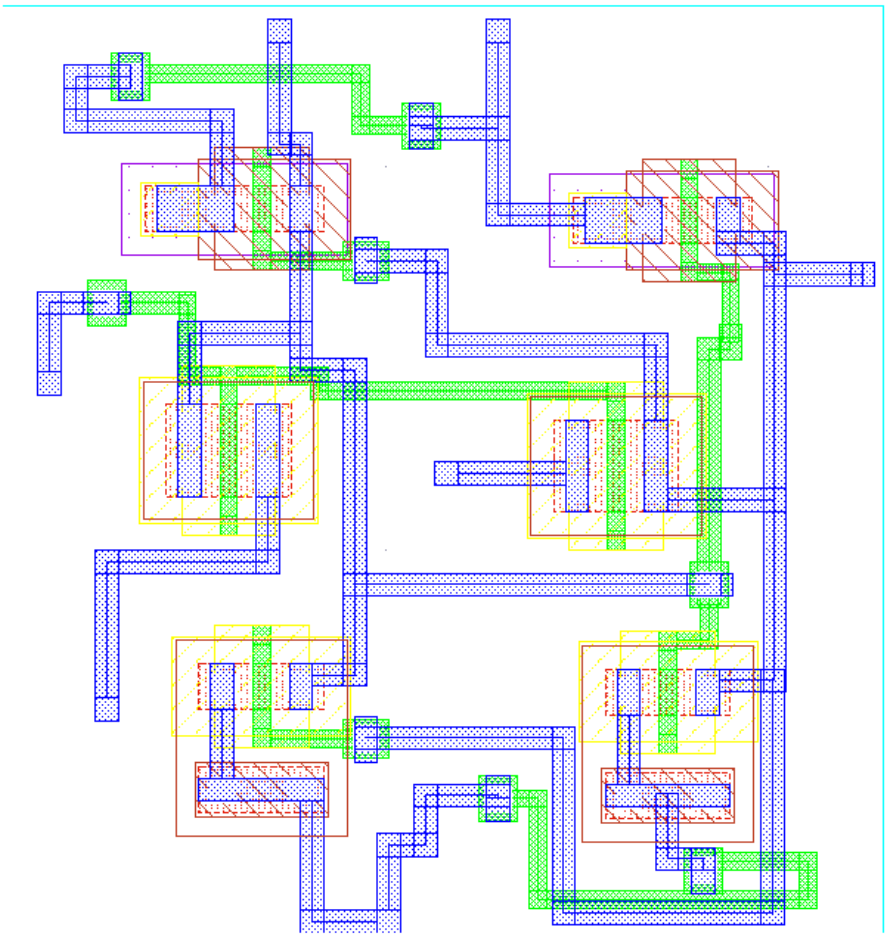

Fig 4.6: Layout For 6 Transistor SRAM Cell

Table 4.1: Specifications For Test Bench

SNO	TRANSISTOR/PORT	SPECIFICATIONS
1	**P1, P2**	WIDTH = **120N**
2	**N1, N2**	WIDTH = **120N**
3	**N3, N4**	WIDTH = **240N**
4	**BL** (V PULSE) (V1=1.1V, V2=0V)	DC VOLTAGE = **1.1v** PERIOD = **40ns** DELAY TIME = **1ps** RISE TIME = **1ps** FALL TIME = **1ps** PULSE WIDTH = **20ns**
5	**BLB**(V PULSE) (V1=0V, V2=1.1V)	
6	WL (**VDC**)	DC VOLTAGE = **1.1v**

Fig 4.7: DRC and LVS Check

After completing the layout design, the next step is to perform DRC (Design Rule Check) and LVS (Layout vs. Schematic) checks. To do this, we navigate to Assura and select the appropriate technology file, such as gpdk45 [home/buet/cadence/gpdk90 v4.6/assura_tech.lib]. Then, we initiate the DRC and LVS checks to ensure that the layout adheres to design rules and matches the schematic representation. This step helps identify any potential errors or discrepancies between the layout and the intended design, allowing for corrections before proceeding further.

DRC (Design Rule Check) and LVS (Layout vs. Schematic) are essential verification processes in integrated circuit (IC) design to ensure the manufacturability and functionality of the layout shown in Fig 4.7. DRC verifies whether the layout adheres to the design rules specified by the foundry or design team. These rules define constraints on various aspects of the layout, such as minimum feature size, spacing between features, and layer-specific requirements. DRC ensures that the layout meets these rules to prevent manufacturing defects and ensure proper functionality of the IC.

LVS compares the layout with the corresponding schematic to ensure they match accurately. It checks for consistency between the physical layout and the intended circuit design. LVS verifies that all components and connections in the layout correspond to their counterparts in the schematic, detecting any discrepancies or errors that could affect the functionality of the IC. Both DRC and LVS are critical steps in the design verification process, helping designers identify and rectify potential issues before sending the layout for fabrication. By ensuring compliance with design rules and verifying the correctness of the layout relative to the schematic, DRC and LVS contribute to the successful fabrication and functionality of the final IC.

CHAPTER – 5

RESULTS / OUTPUTS

We have analysed the outputs of the 6-transistor SRAM in 45nm technology. We obtained the outputs of the 6T SRAM read operations, including BL, BLB, Q, and QB, and we have submitted these outputs shown in Fig 5.1. Additionally, we have calculated the overall power consumption of the 6T SRAM cell in 45nm technology, which is approximately 28n watts.

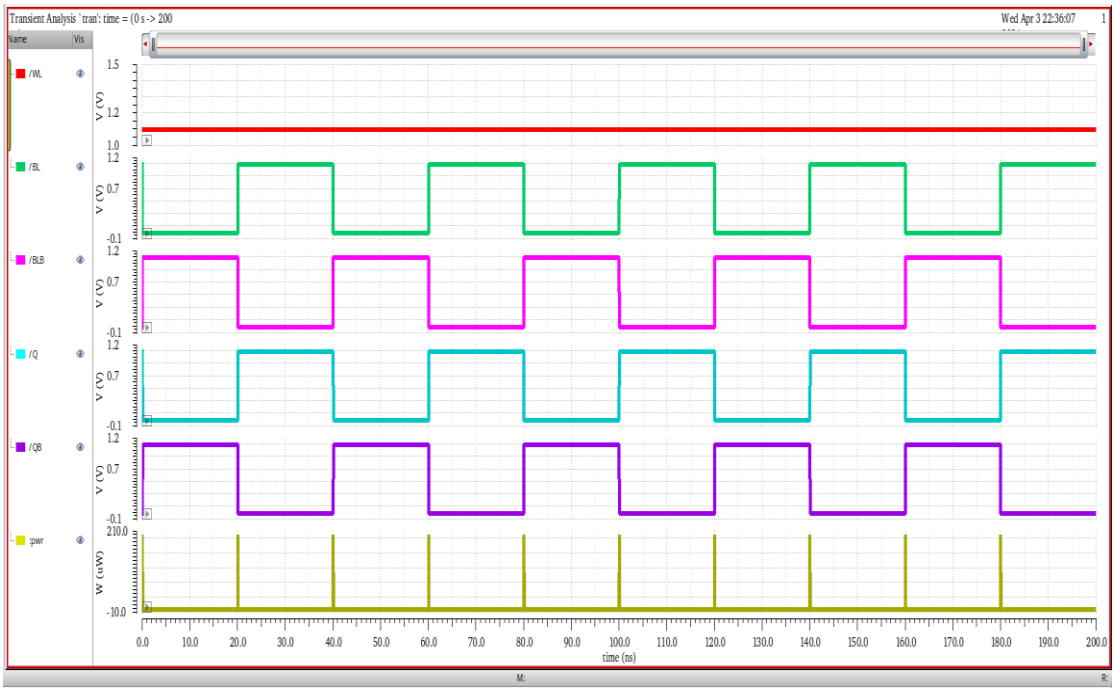

Fig 5.1: Simulation Results of 6t SRAM

We have analysed the outputs of the 6-transistor SRAM in 45nm technology. The outputs obtained from the 6T SRAM read operations include BL, BLB, Q, and QB, which we have submitted for further evaluation. Additionally, we calculated the overall power consumption of the 6T SRAM cell in 45nm technology, which amounts to approximately 28nano watts. Furthermore, we determined the area occupied by the 6-transistor SRAM cell to be 11.155 (sq. nm).

We stimulated the SRAM in different parameters, obtaining different power values for each stimulation.

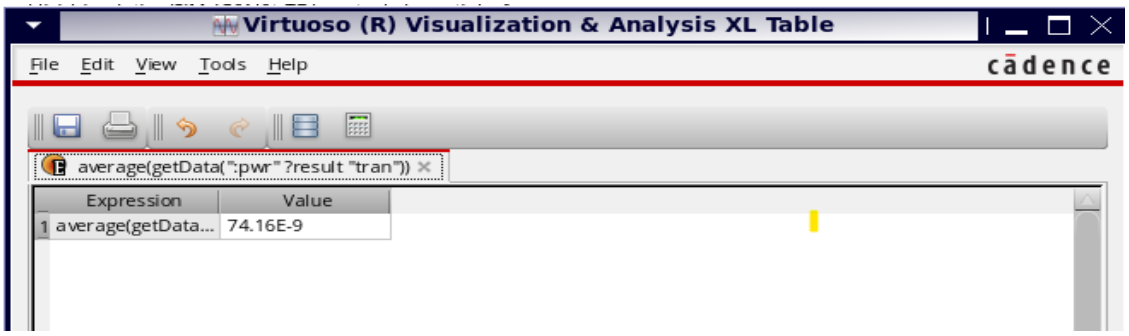

Fig 5.2: finger width and total width of access transistors as 120n and for inner cross-coupled inverters, as 240n.

First, we took the Finger Width and Total Width of Access transistors as 120n and for inner cross-coupled inverters, which act as the Memory unit, as 240n. Then, we obtained the power value for the 6T SRAM as 74.169 nano watts Shown in Fig 5.2.

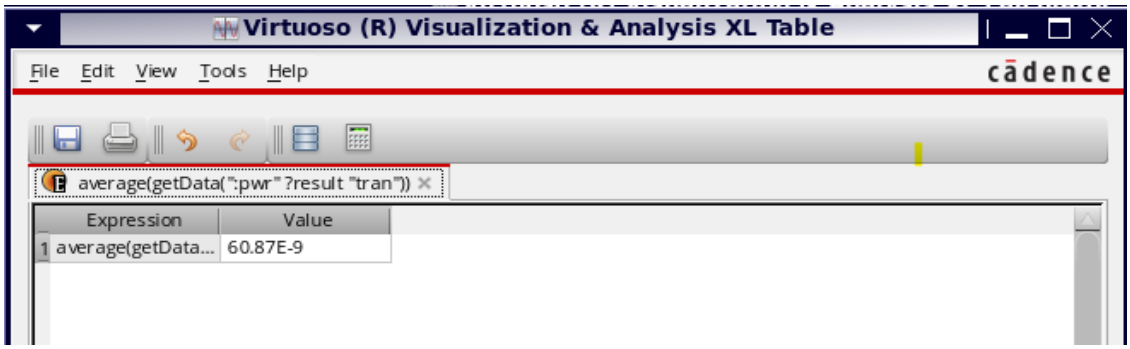

Fig 5.3: finger width and total width of access transistors and for inner cross-coupled inverters, as 240n.

Following the initial simulation, adjustments were made to the parameters, increasing the Finger Width and Total Width of Access transistors to 240n, and setting the same values for the inner cross-coupled inverters acting as the Memory unit. Subsequently, the power value for the 6T SRAM was determined to be 60.87 nano watts shown in Fig 5.3.

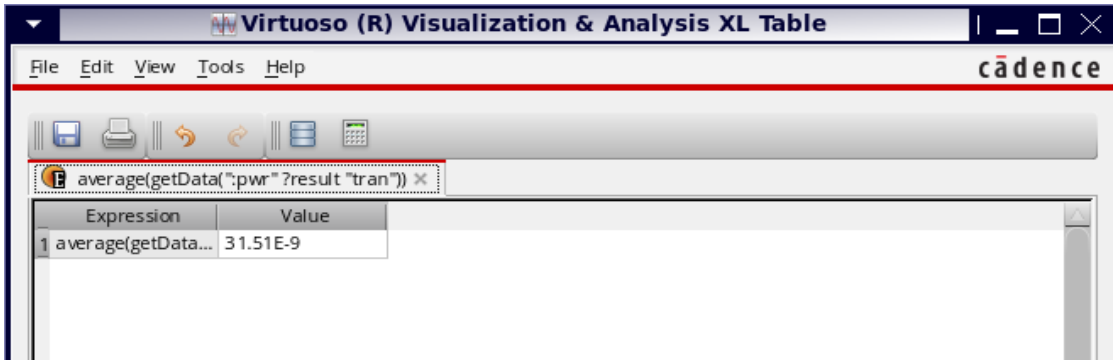

Fig 5.4: finger width and total width of access transistors and for inner cross-coupled inverters, as 120n.

Following the completion of the first and second simulations, adjustments were made to set the Finger Width and Total Width of Access transistors to 120n, along with the inner cross-coupled inverters acting as the Memory unit, also set to 120n. Subsequently, the power value for the 6T SRAM was determined to be 31.51 nano watts shown in Fig 5.4.

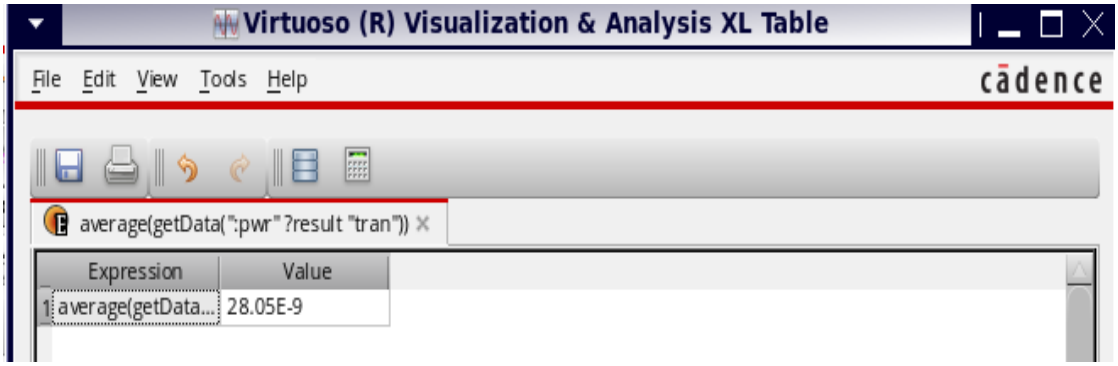

Fig 5.5: Finger Width and Total Width Of Access Transistors As 240n And For Inner Cross-Coupled Inverters, As 120n

Following three simulations, we adjusted the parameters to set the Finger Width and Total Width of Access transistors to 240n, while the inner cross-coupled inverters, acting as the Memory unit, were set to 120n. Subsequently, the power value for the 6T SRAM was determined to be 28.05 nano watts shown in Fig 5.5.

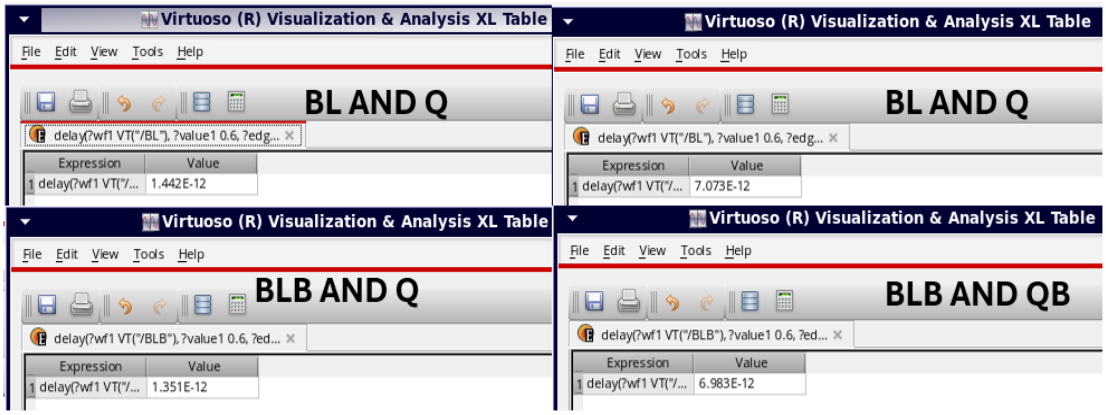

Fig 5.6: Propagation Delay

We obtained the delay values for different signal pairs in the 6-transistor SRAM, including BL vs Q (1.442n s), BL vs QB (7.073n s), BLB vs Q (1.351E-12 s), and BLB vs QB (6.983n s). These measurements provide insights into the propagation delays of the SRAM cell shown in Fig 5.6.

The previous results obtained from various simulations of the 6-transistor SRAM schematic design, we found that the power consumption varied across different parameter settings. In earlier simulations, power values such as 74.169 nano watts, 60.87 nano watts, and 31.51 nano watts were observed. However, after adjusting the parameters in subsequent simulations, particularly setting the Finger Width and Total Width of Access transistors to 240n and the inner cross-coupled inverters to 120n, the power consumption decreased to 28.05n watts. This signifies a notable reduction in power usage compared to earlier simulations. Therefore, considering the 28.05 nano watts power consumption as the lowest among all simulations indicates an improvement in power efficiency for the 6T SRAM design under the specified parameter configuration. The obtained delay values for various signal pairs in the 6-transistor SRAM, such as BL vs Q (1.442n s), BL vs QB (7.073n s), BLB vs Q (1.351n s), and BLB vs QB (6.983n s), we conducted a delay analysis. This analysis provides insights into the time taken for data access operations within the SRAM cell. By comparing these delay values, we can evaluate the speed and efficiency of the SRAM cell in responding to read and write requests.

Based on the schematic design, we also drew the layout for the 6-transistor SRAM cell and obtained the results of the area required for the layout.

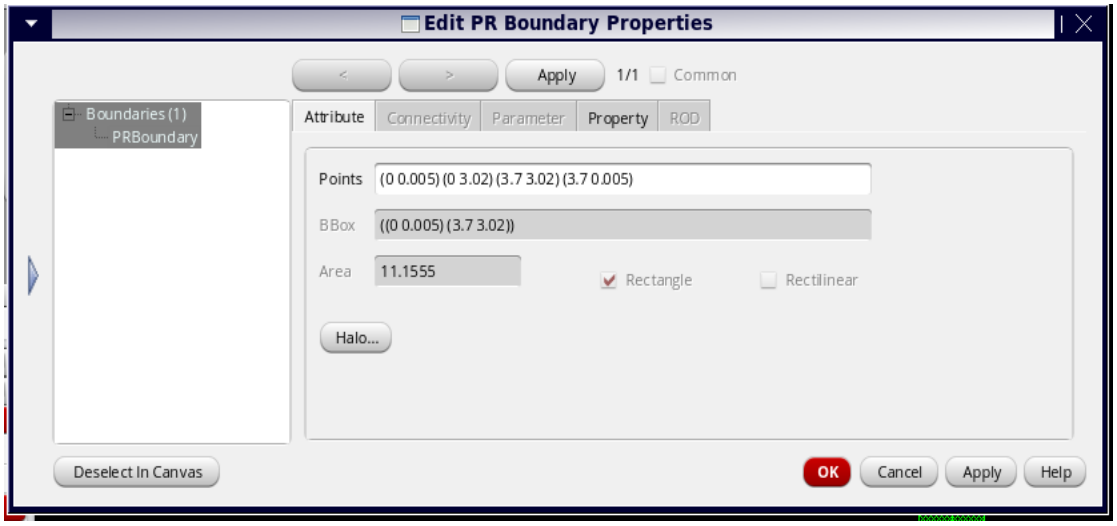

Fig 5.7: Area of 6t SRAM Layout

Fig 5.7 shows The area obtained by the layout for the 6-transistor SRAM cell is 11.155 square nanometers.

Table 5.1: Final Results Of 6 Transistor Sram Cell In 45 Nano Meter Technology

SNO	PARAMETER	VALUE		TECHNOLOGY
1	POWER (**nano watts**)	28.05		**45nm**
2	DELAY (**nano seconds**)	BL vs Q	1.442	
		BL vs QB	7.073	
		BLB vs Q	1.351	
		BLB vs QB	6.983	
3	AREA (**square nanometres**)	11.155		

CHAPTER – 6

FUTURE SCOPE AND CONCLUSION

6.1 FUTURE SCOPE

The future of 6-transistor SRAM (6T SRAM) cells holds significant potential for advancements in semiconductor technology and memory applications. With ongoing research and development efforts, there is a clear trajectory for further scaling down the size of 6T SRAM cells to advanced technologies, enabling higher-density memory arrays and improved performance in future integrated circuits. Additionally, there is a growing demand for energy-efficient electronics, driving the need for optimization of 6T SRAM cells to reduce power consumption. As research continues into new SRAM cell architectures and their integration with system-on-chip designs, the future of 6T SRAM cells remains bright, with potential applications spanning across various industries and domains.

6.2 CONCLUSION

In conclusion, the analysis of the 6-transistor SRAM using Cadence software in the 45-nanometer technology generation reveals important insights into its performance characteristics. The power consumption of the SRAM cell varied between 28.05n watts and 74.169n watts across different simulations and parameter configurations. Notably, the lowest power consumption observed was 28.05n watts, indicating improved power efficiency under specific parameter settings. Additionally, delay characterization provided valuable information on the timing behavior of the SRAM cell, with delay values ranging from 1.442 nanoseconds to 7.073 nanoseconds for different signal pairs. These measurements offer insights into the speed and efficiency of data access operations within the SRAM cell. Furthermore, the layout design of the SRAM cell, conducted using Cadence Layout XL, resulted in an area requirement of 11.155 square nanometers. This comprehensive analysis underscores the importance of optimizing design parameters to achieve a balance between power efficiency, performance, and layout area in 45-nanometer technology for 6-transistor SRAM designs.

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IMPLEMENTATION AND ANALYSIS OF 6-TRANSISTOR SRAM CELL

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