HDM ASSIGNMENT 1

SUBMITTED BY:

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QUESTION 1:Implement 4 bit ripple carry adder. Optimize the adder for speed. Assume load capacitance to be 50 pF, VDD = 3.3 V. You may assume input capacitance to be 2 pF (for the input A [3:0], B [3:0] and Cin) if required in the calculation.

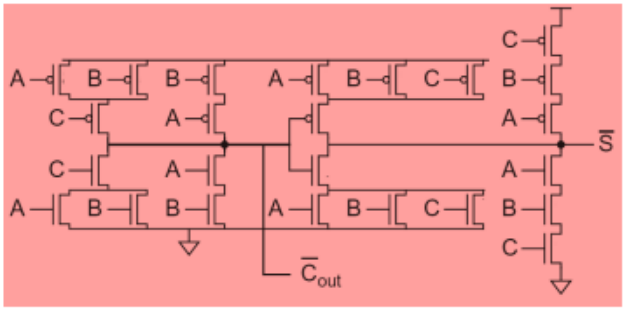


Fig.1 Basic Full adder with complementary output

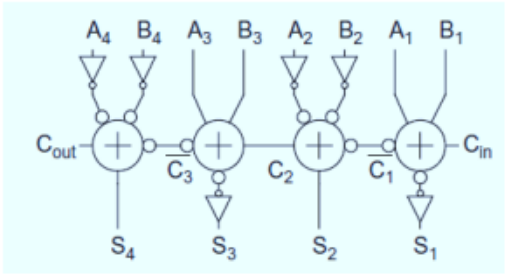
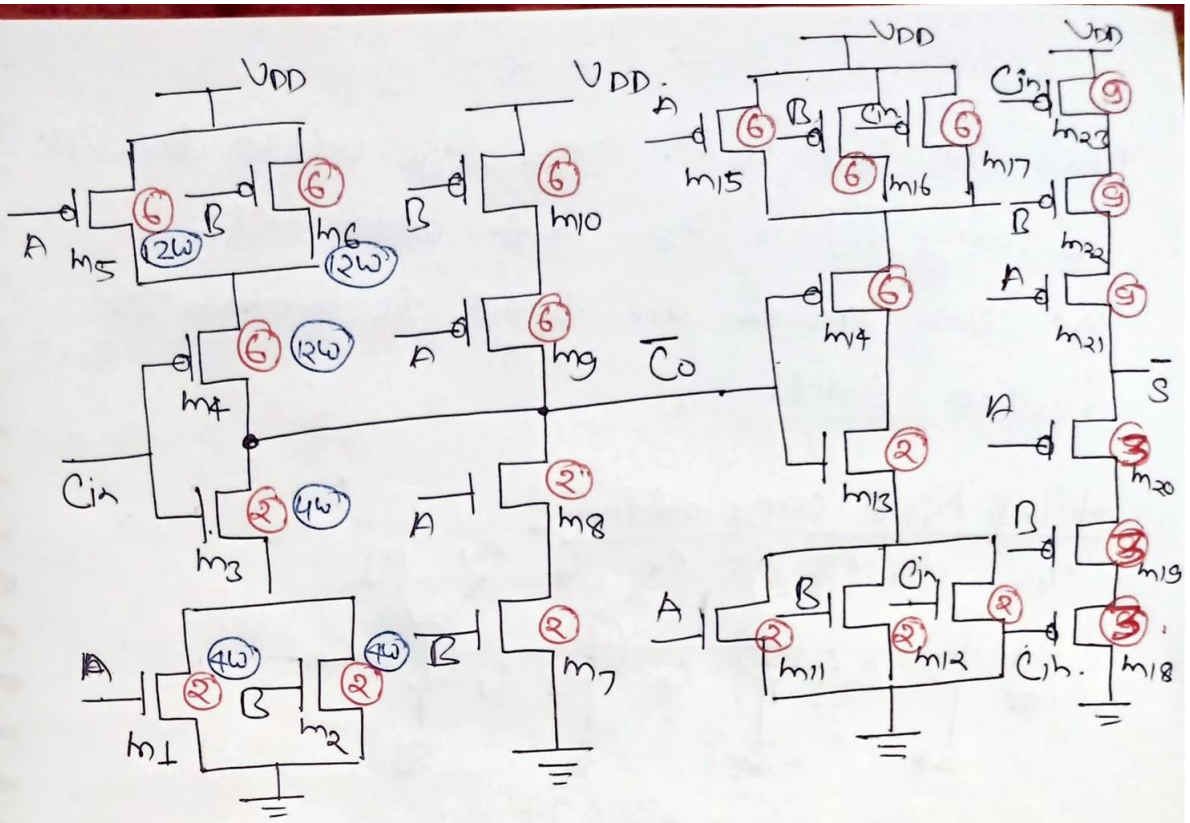


Fig.2 4 bit ripple carry adder using Fig.1

(A)Detailed calculation and sizing of transistor

For 1-bit adder



From the MOS model,

$$\gamma = \frac{\mu_n}{\mu_p} = \frac{666}{210} = 3.14 \simeq 3.$$

$$\therefore (W/L)_p = 4(W/L)_n$$

If the carry ckt is symmetrically sized, then its I/P has a logical effort of 2.

The optimal stage is 4 (FO4) for minimum delay.

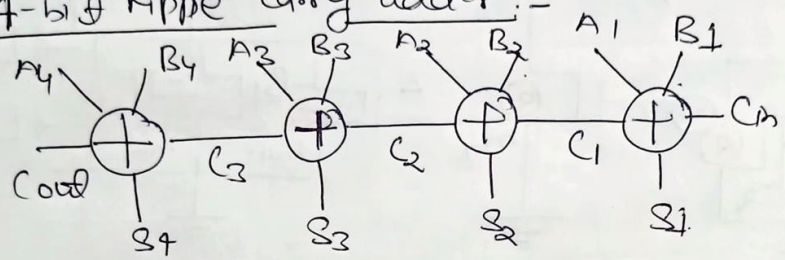
$$f = gh \Rightarrow 4 = gh \Rightarrow \therefore h = \frac{4}{2} = 2$$

$$h \text{ (for a stage)} = \frac{\text{Cout of carry stage}}{C_{in}} = 2$$

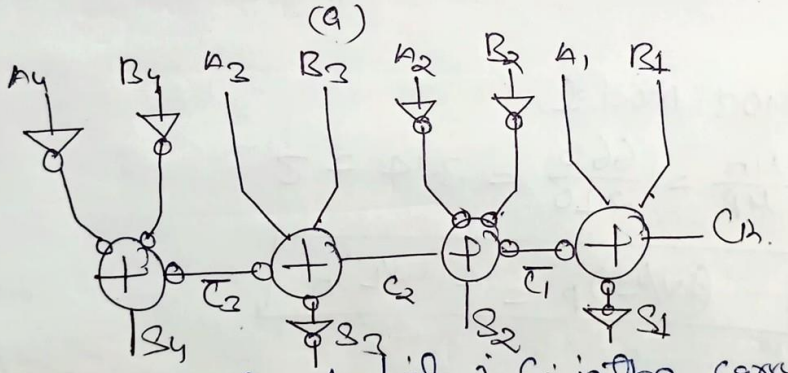
∴ optimal fanout is 2.

Now, the cout of the carry stage will be the I/P (or carry in) for the next adder cell. The sum gates are sized to minimize to reduce load.

4-bit Ripple carry adder :-



(a)



The carry out of bit i, C_i, is the carry-in to bit (i+1). This carry is said to have twice the weight of the sum S_i. The delay of the adder is set by the time for the carries to ripple through the N-stages, so the $t_{c \to cout}$ delay should be minimized

$$\therefore M_1 = M_2 = M_3 = 2\left(\frac{W}{L}\right)_n = 2 \times 2\left(\frac{W}{L}\right) = 4\left(\frac{W}{L}\right)$$

$$= \frac{4\mu m}{1\mu m}.$$

$M_4 = M_5 = M_6 = 2\left(\frac{W}{L}\right)_p = 2 \times 6\left(\frac{W}{L}\right) = 12\left(\frac{W}{L}\right)$

$= \frac{12\mu m}{1\mu m}$.

Resd ale the x-sistrs. sizing are same by maintaing the ratio of $M_n : M_p = 3:1$.

$M_7 = M_8 = 2\left(\frac{W}{L}\right)_n = \frac{2\mu m}{1\mu m}$

$M_9 = M_{10} = 6\left(\frac{W}{L}\right)_p = \frac{6\mu m}{1\mu m}$

2μm Stage :-

$M_{11} = M_{12} = M_{13} = 2\left(\frac{W}{L}\right)_n = \frac{2\mu m}{1\mu m}$

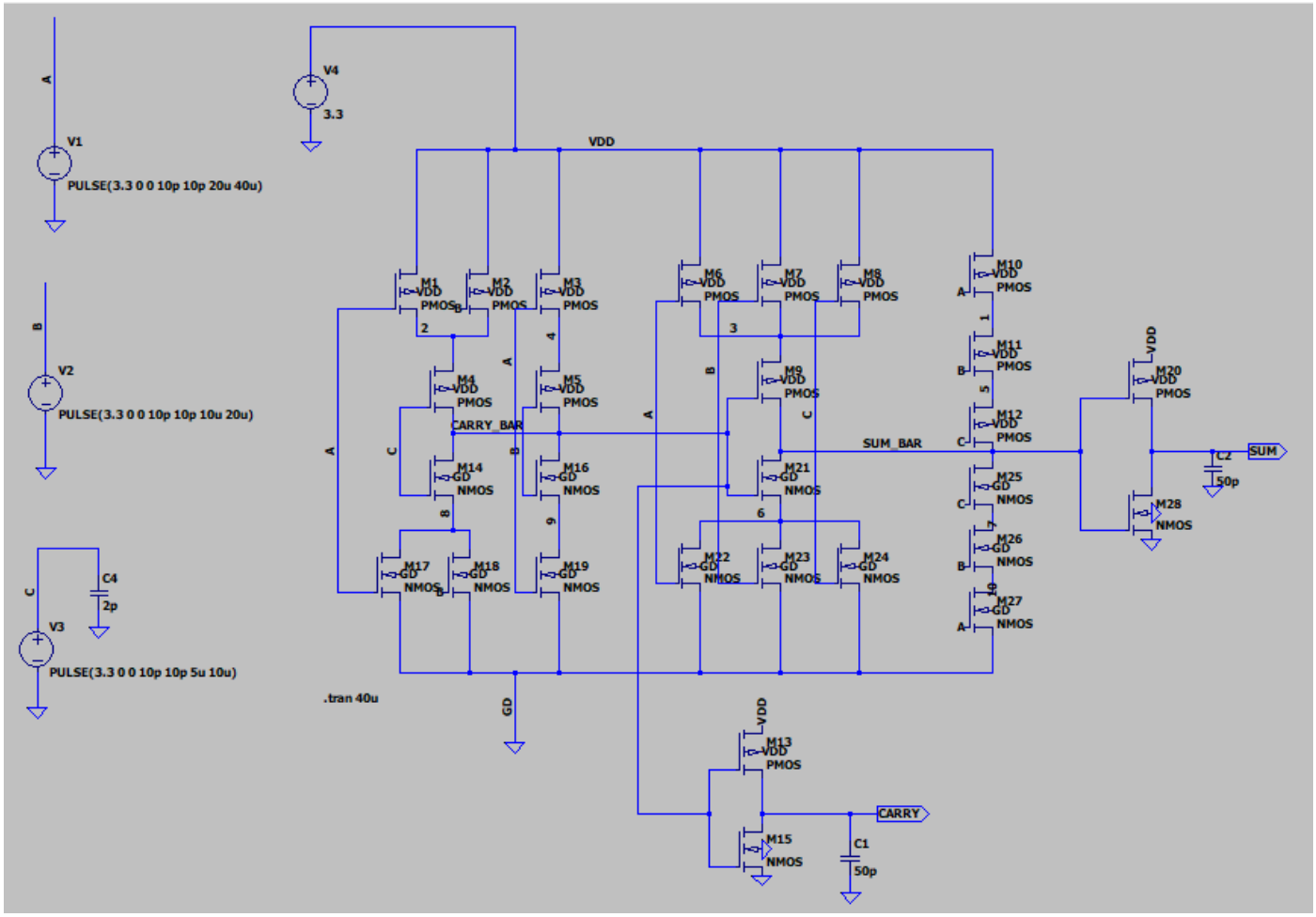
$M_{14} = M_{15} = M_{16} = 6\left(\frac{W}{L}\right)_p = \frac{6\mu m}{1\mu m}$

$M_{18} = M_{19} = M_{20} = 3\left(\frac{W}{L}\right)_n = \frac{9\mu m}{1\mu m}$ $\frac{3\mu m}{1\mu m}$

$M_{21} = M_{22} = M_{23} = 9\left(\frac{W}{L}\right)_p = \frac{9\mu m}{1\mu m}$.

(B)Schematic and spice netlist

- Without optimisation




```
M1 VDD A 2 VDD PMOS l=1u w=12u
M2 VDD B 2 VDD PMOS l=1u w=12u
M3 VDD A 4 VDD PMOS l=1u w=6u
M4 2 C CARRY_BAR VDD PMOS l=1u w=12u
M5 4 B CARRY_BAR VDD PMOS l=1u w=6u
M6 VDD A 3 VDD PMOS l=1u w=6u
M7 VDD B 3 VDD PMOS l=1u w=6u
M8 VDD C 3 VDD PMOS l=1u w=6u
M9 3 CARRY_BAR SUM_BAR VDD PMOS l=1u w=6u
M10 VDD A 1 VDD PMOS l=1u w=9u
M11 1 B 5 VDD PMOS l=1u w=9u
M12 5 C SUM_BAR VDD PMOS l=1u w=9u
M14 CARRY_BAR C 8 0 NMOS l=1u w=4u
M16 CARRY_BAR B 9 0 NMOS l=1u w=2u
M17 8 A 0 0 NMOS l=1u w=4u
M18 8 B 0 0 NMOS l=1u w=4u
M19 9 A 0 0 NMOS l=1u w=2u
M21 SUM_BAR CARRY_BAR 6 0 NMOS l=1u w=2u
M22 6 A 0 0 NMOS l=1u w=2u
M23 6 B 0 0 NMOS l=1u w=2u
M24 6 C 0 0 NMOS l=1u w=2u
M25 SUM_BAR C 7 0 NMOS l=1u w=3u
M26 7 B 10 0 NMOS l=1u w=3u
M27 10 A 0 0 NMOS l=1u w=3u
```

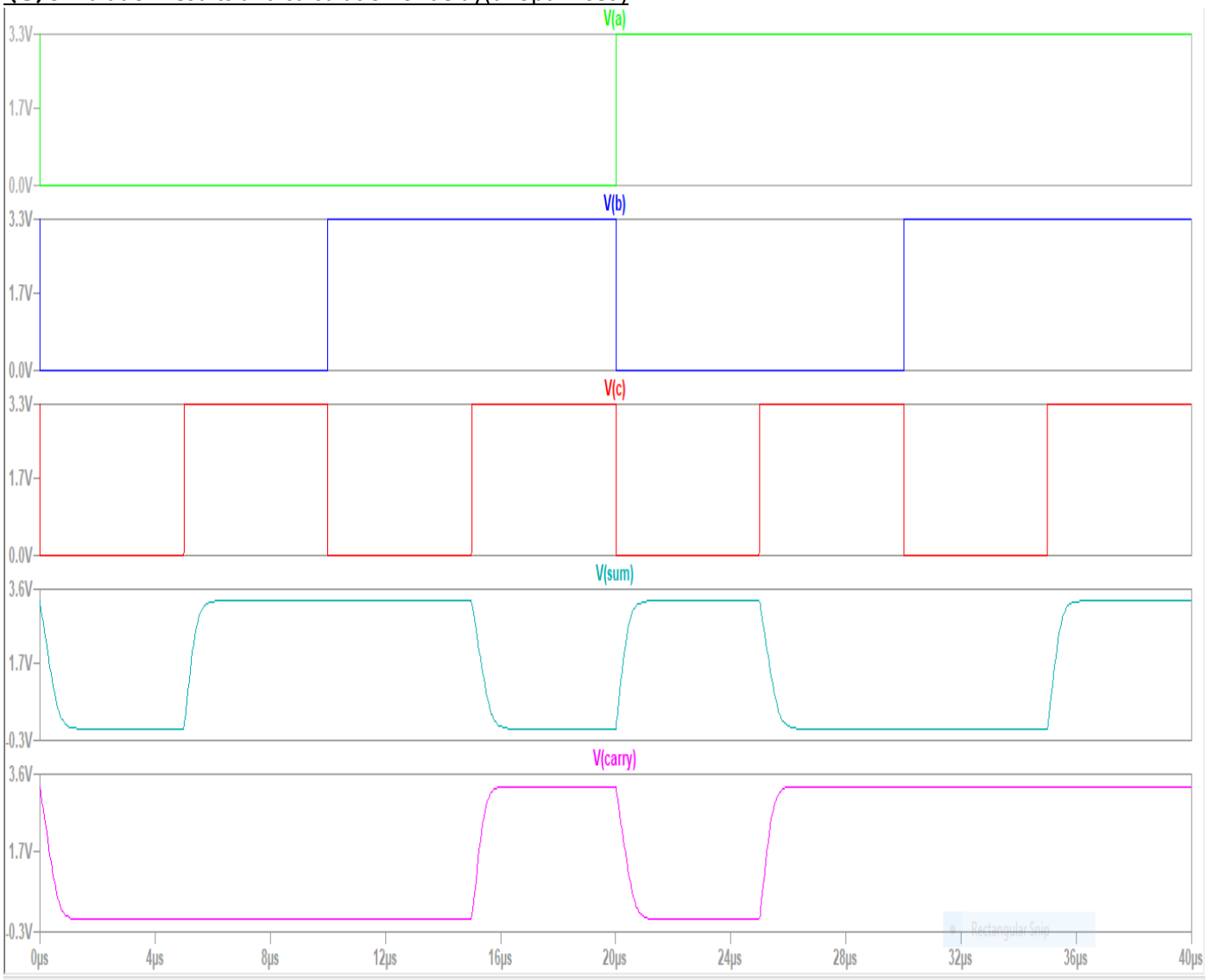
```
V1 A 0 PULSE(3.3 0 0 10p 10p 20u 40u)
V2 B 0 PULSE(3.3 0 0 10p 10p 10u 20u)
V3 C 0 PULSE(3.3 0 0 10p 10p 5u 10u)
V4 VDD 0 3.3
C4 C 0 2p

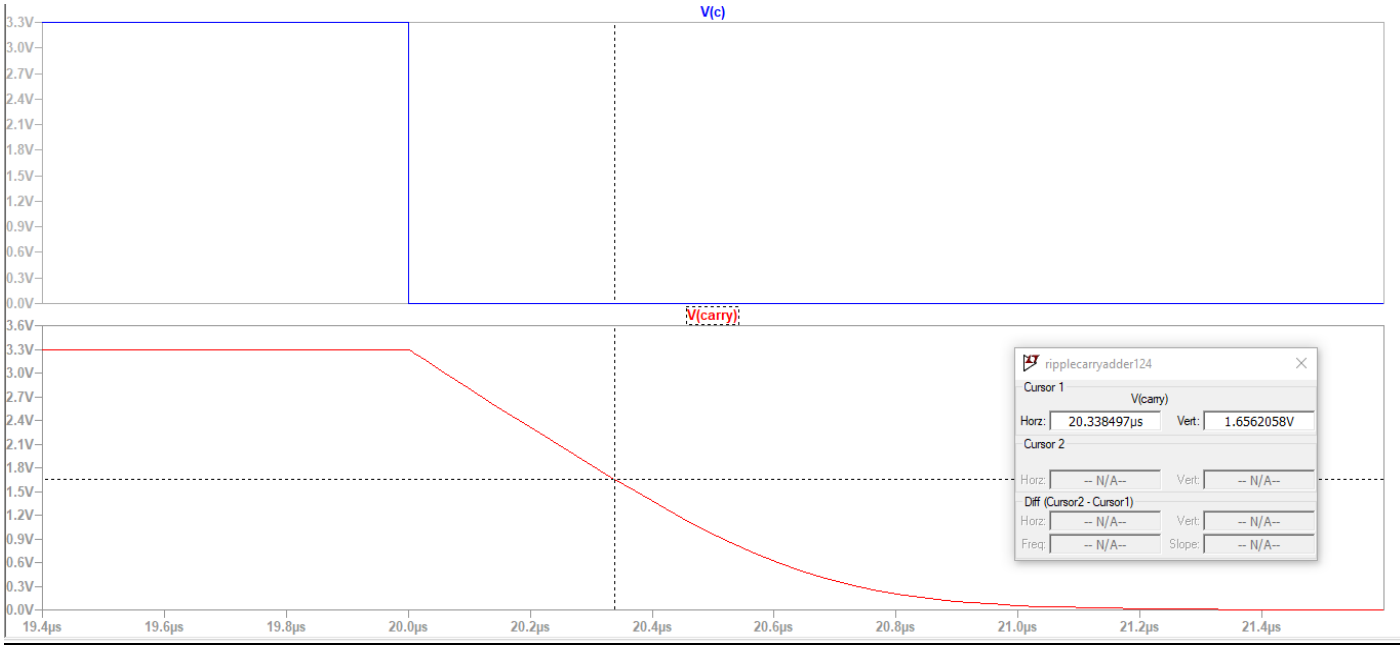
M13 VDD CARRY_BAR CARRY VDD PMOS l=1u w=3u
M15 CARRY CARRY_BAR 0 0 NMOS l=1u w=1u
C1 CARRY 0 50p

M20 VDD SUM_BAR SUM VDD PMOS l=1u w=3u
M28 SUM SUM_BAR 0 0 NMOS l=1u w=1u
C2 SUM 0 50p

.model NMOS NMOS
.model PMOS PMOS
.tran 40u
```

(c) Simulation results and calculation of delay(unoptimised)

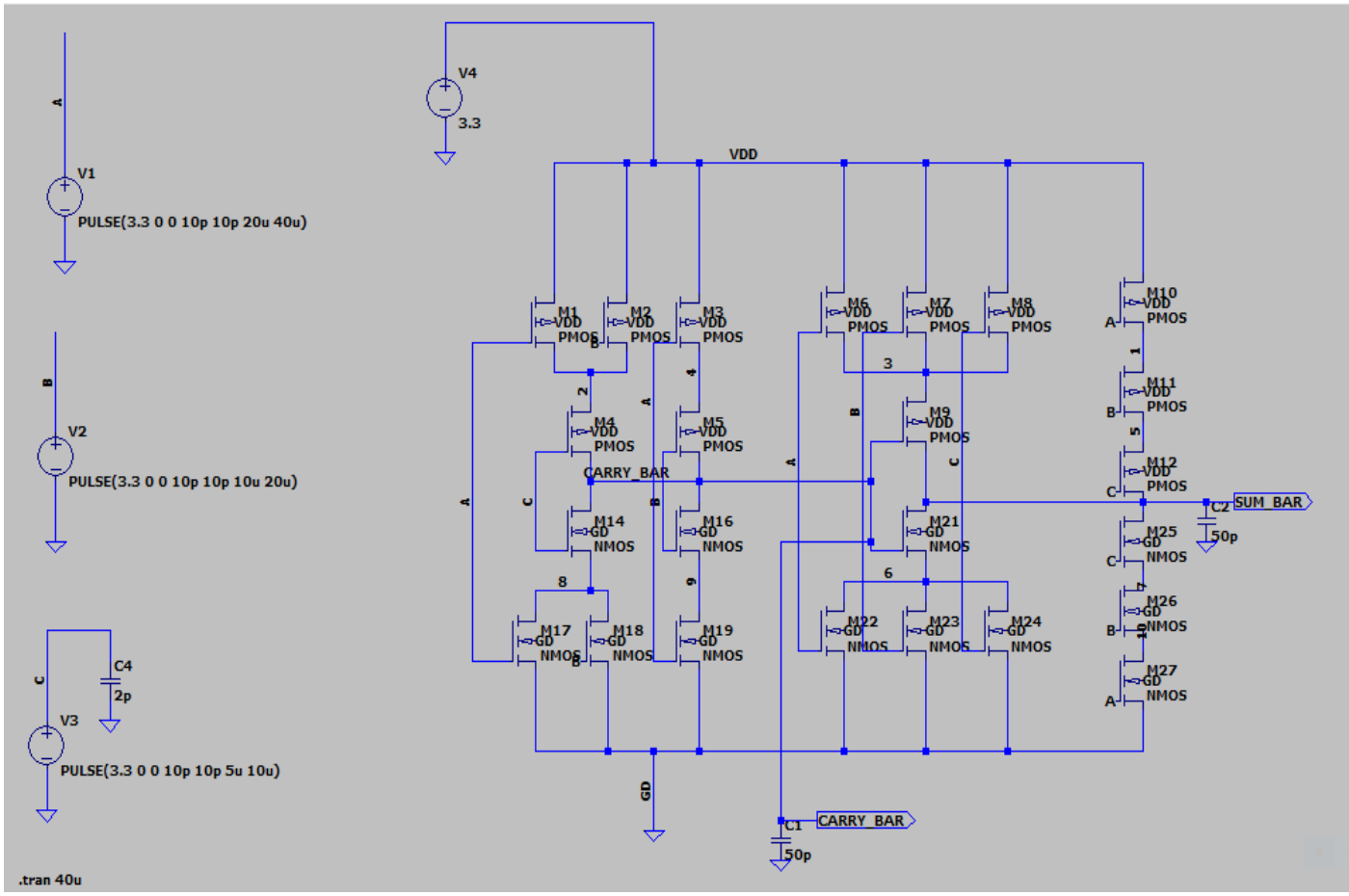




Unoptimized carry fall delay=338ns
Unoptimized carry rise delay=247ns

(B) Schematic and spice netlist

- **Optimised**



```
M1 VDD A 2 VDD PMOS l=1u w=21u
M2 VDD B 2 VDD PMOS l=1u w=21u
M3 VDD A 4 VDD PMOS l=1u w=6u
M4 2 C CARRY_BAR VDD PMOS l=1u w=21u
M5 4 B CARRY_BAR VDD PMOS l=1u w=6u
M6 VDD A 3 VDD PMOS l=1u w=6u
M7 VDD B 3 VDD PMOS l=1u w=6u
M8 VDD C 3 VDD PMOS l=1u w=6u
M9 3 CARRY_BAR SUM_BAR VDD PMOS l=1u w=6u
M10 VDD A 1 VDD PMOS l=1u w=9u
M11 1 B 5 VDD PMOS l=1u w=9u
M12 5 C SUM_BAR VDD PMOS l=1u w=9u
M14 CARRY_BAR C 8 0 NMOS l=1u w=7u
M16 CARRY_BAR B 9 0 NMOS l=1u w=2u
M17 8 A 0 0 NMOS l=1u w=7u
M18 8 B 0 0 NMOS l=1u w=7u
M19 9 A 0 0 NMOS l=1u w=2u
M21 SUM_BAR CARRY_BAR 6 0 NMOS l=1u w=2u
M22 6 A 0 0 NMOS l=1u w=2u
M23 6 B 0 0 NMOS l=1u w=2u
M24 6 C 0 0 NMOS l=1u w=2u
M25 SUM_BAR C 7 0 NMOS l=1u w=3u
M26 7 B 10 0 NMOS l=1u w=3u
M27 10 A 0 0 NMOS l=1u w=3u

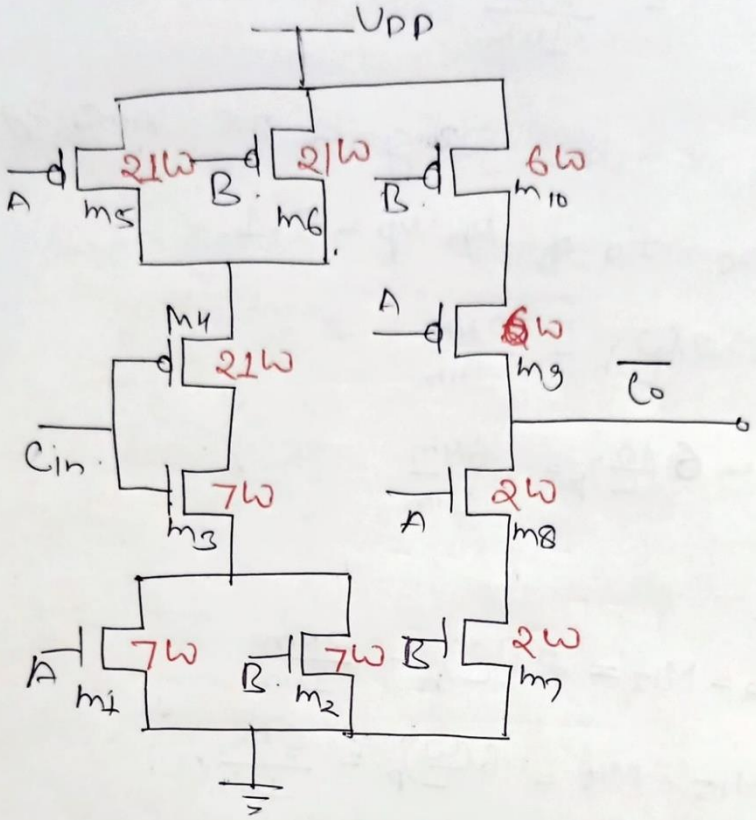
V1 A 0 PULSE(3.3 0 0 10p 10p 20u 40u)
V2 B 0 PULSE(3.3 0 0 10p 10p 10u 20u)
V3 C 0 PULSE(3.3 0 0 10p 10p 5u 10u)
V4 VDD 0 3.3

C4 C 0 2p
C1 CARRY_BAR 0 50p
C2 SUM_BAR 0 50p

.model NMOS NMOS
.model PMOS PMOS

.tran 40u
```

Delay Calculation :-



Carry stage:

The delay can be reduced by omitting the inverters on the O/Ps. Bcz addition is a self dual function (i.e. the function of complementary I/P is the complementary of the fun.), an inverting full adder receiving complementary I/P produces true O/Ps. Every other stage operates on complementary data. The delay inverting the adder I/Ps & sum O/Ps is off the critical ripple carry path.

$C_L = 50pf$

$C_{in} = 2pf$

$C_{\overline{cout}}$ = (6W + 2W) + (6W + 2W) + (9W + 3W).

cap. at node Cout = 8W + 8W + 12W

$$\boxed{C_{\overline{cout}} = 28W}$$

∵ optimal fanout is 2 → $\therefore \frac{C_{\overline{cout}}}{C_{ci}} = 2$

$$\therefore \boxed{C_{\overline{cout}} = 2C_{ci}}$$

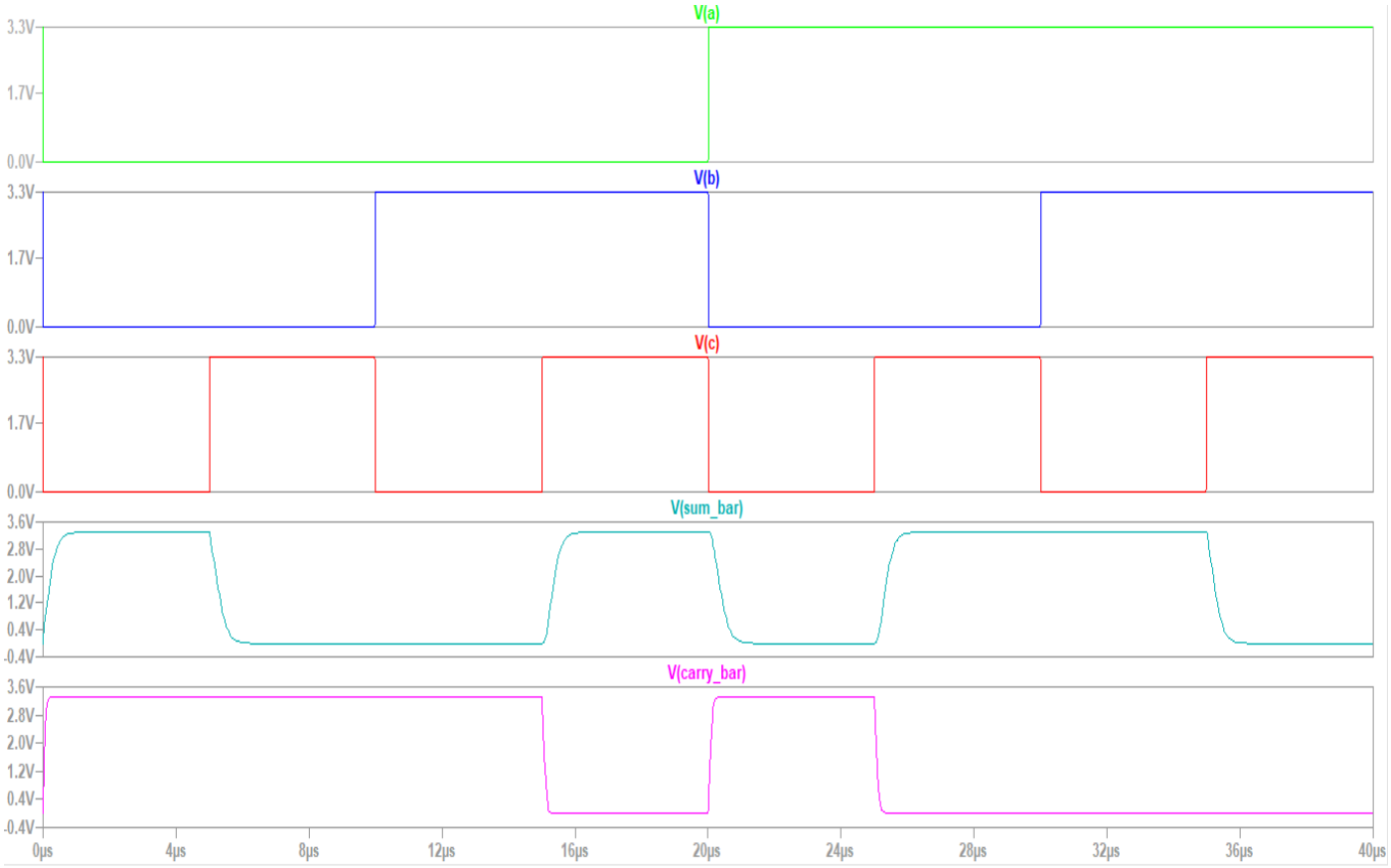
$$\left.\begin{aligned} C_{\overline{cout}} &= 2C_{ci} \\ C_{\overline{cout}} &= 28W + C_{ci} \end{aligned}\right\} \therefore C_{ci} = 28W$$

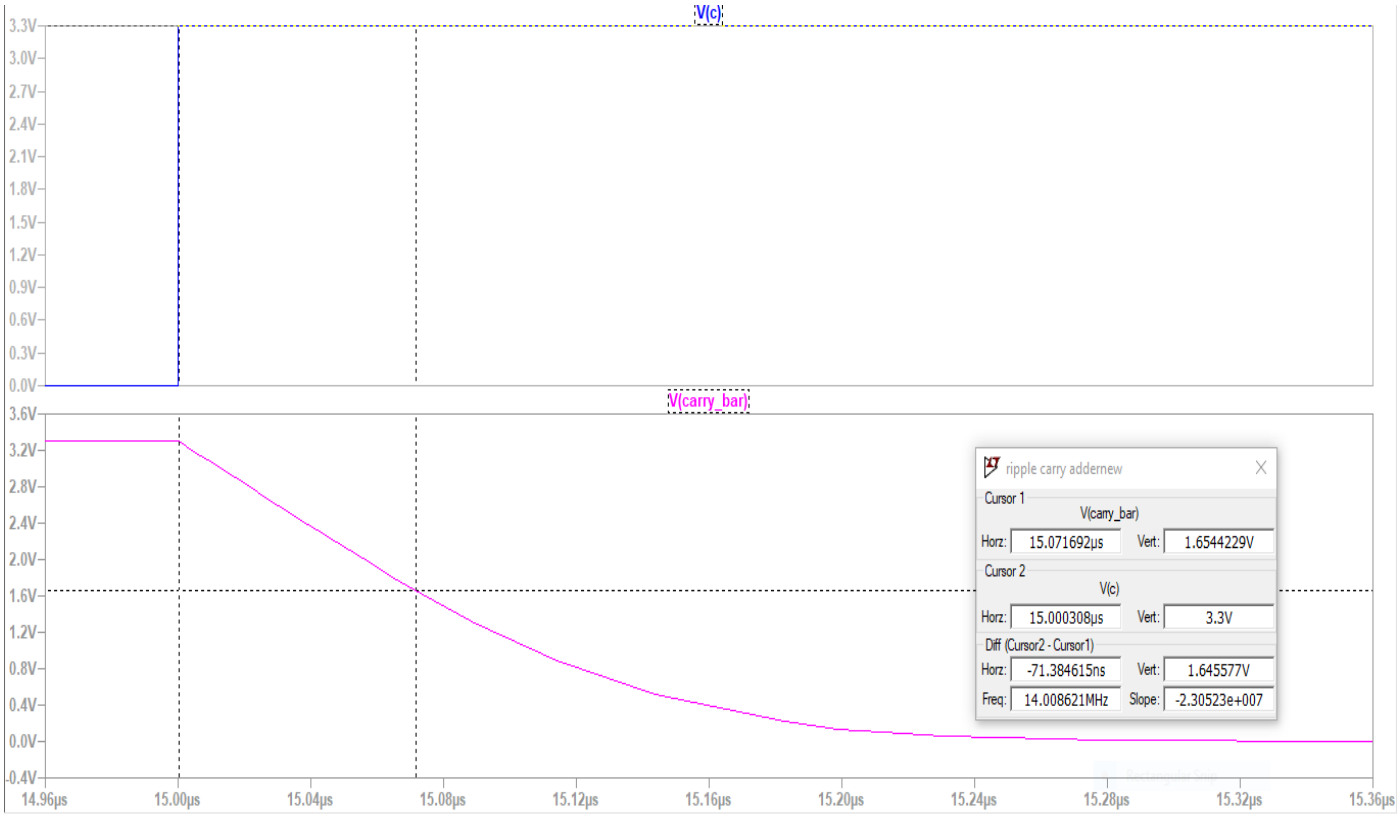
∴ The driving transistors ($M_1, M_2, \ldots M_6$) can be sized as:

$$\boxed{M_1 = M_2 = M_3 = 7W = \frac{7\mu m}{1\mu m}}$$

$$\boxed{M_4 = M_5 = M_6 = 7W_p = 7(3W) = 21W = \frac{21\mu m}{1\mu m}}$$

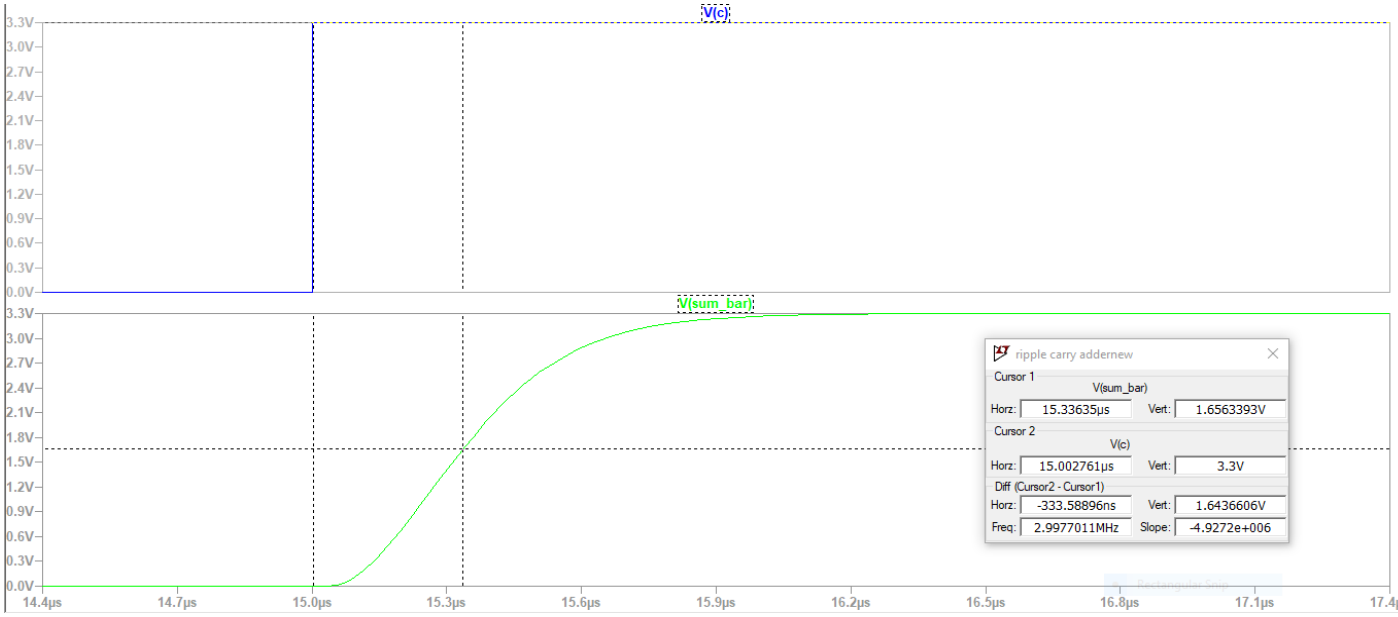
(C)Simulation results and calculation of delay(optimised)





Optimised fall delay of carry_bar=71ns

Optimised rise delay of carry_bar=63ns



Optimised rise delay of sum_bar=333ns

Optimised fall delay of sum_bar=364ns

BY THE METHOD OF LOGICAL EFFORT

By the method of Logical effort :-

For carry stage,

$$F = G_1 B H_1$$

$$= \left(\frac{28W}{4W}\right) \times 1 \times \left(\frac{50pf}{2pf}\right)$$

$$= 7 \times 25$$

$$\boxed{F = 175}$$

For optimum no. of stages,

$$N = \log_4 F$$

$$= \log_4 (175).$$

No. of optimum stages,

$$\boxed{N = 3.72}$$

At $N = 4$:

delay, $d = NF^{1/N} + P$. — (1)

Parasitic Delay of Inverter.

parasitic delay of carry stage $= \frac{(6W+2W)+(6W+2W)}{4W}$

$$= \frac{16RC}{4RC}$$

$$= 4 P_{inv}.$$

From (1), we have

$$d = 4(175)^{1/4} + 4.$$

$$\boxed{d = 18.547}$$

If N = 3:-

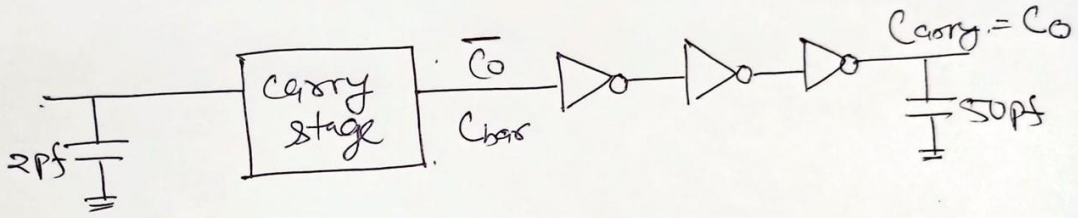
$$d = N(F)^{1/N} + P$$

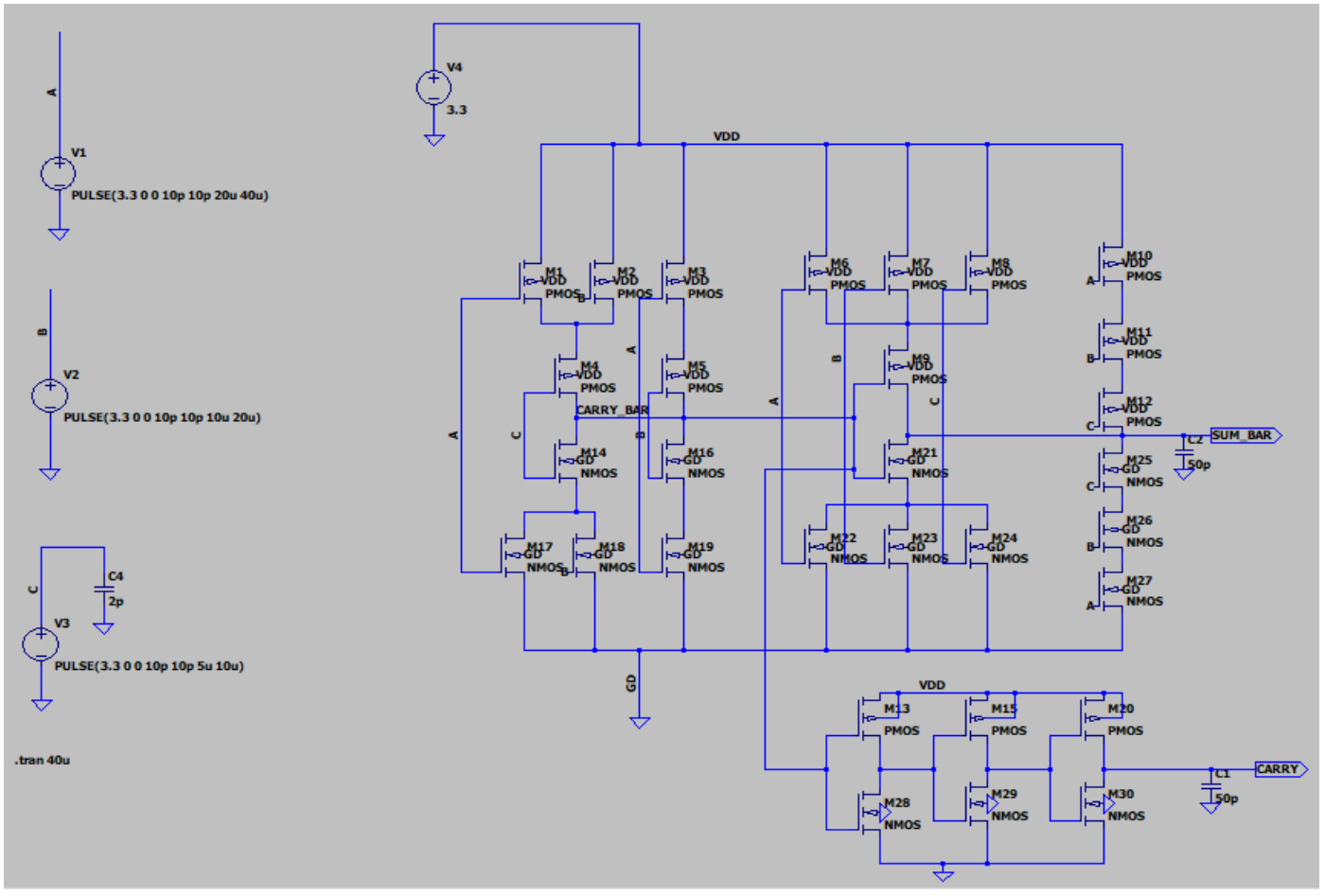
$$= 3(17.3)^{1/3} + 3$$

$$\boxed{d = 19.78\ \tau}$$

∴ Delay is least at $\boxed{N = 4}$

∴ We have to add 3 extra ~~inverter~~ inverter as carry stage already occupied 1 stage.

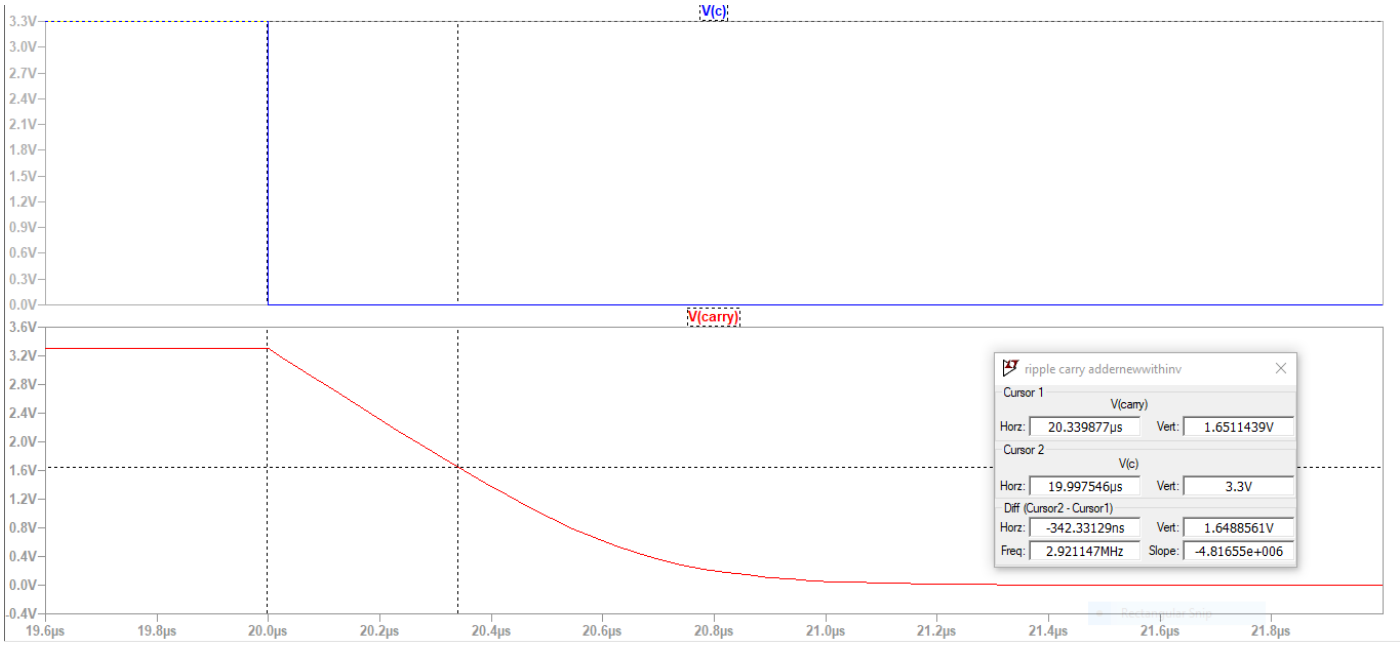




ADDITION OF INVERTERS

```
M13 VDD CARRY_BAR N011 VDD PMOS l=1u w=3u
M15 VDD 11 12 VDD PMOS l=1u w=3u
M20 VDD 12 CARRY VDD PMOS l=1u w=3u
M28 11 CARRY_BAR 0 0 NMOS l=1u w=1u
M29 12 11 0 0 NMOS l=1u w=1u
M30 CARRY 12 0 0 NMOS l=1u w=1u
```

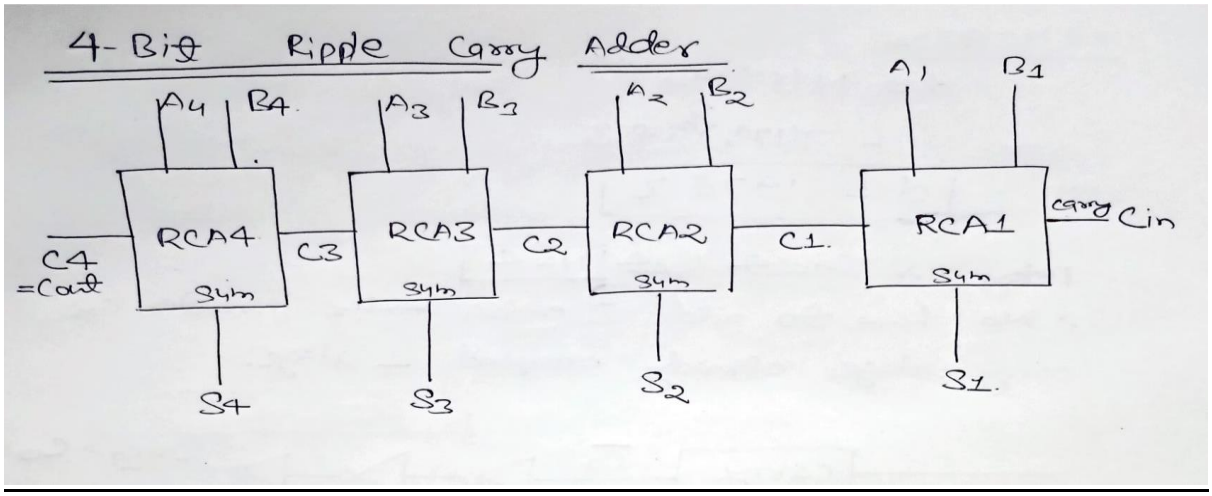
DELAY CALCULATION



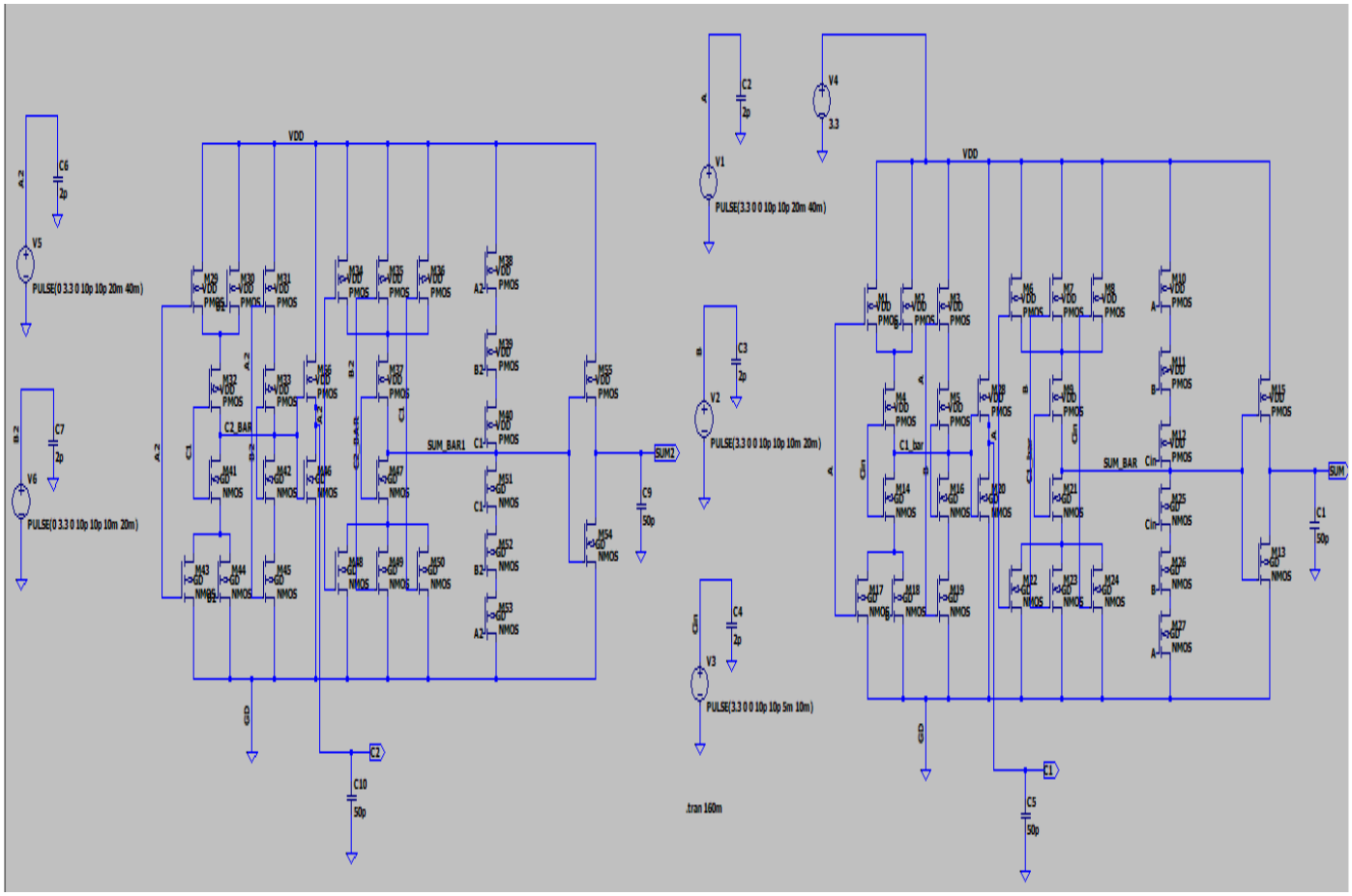
FALL DELAY=342ns

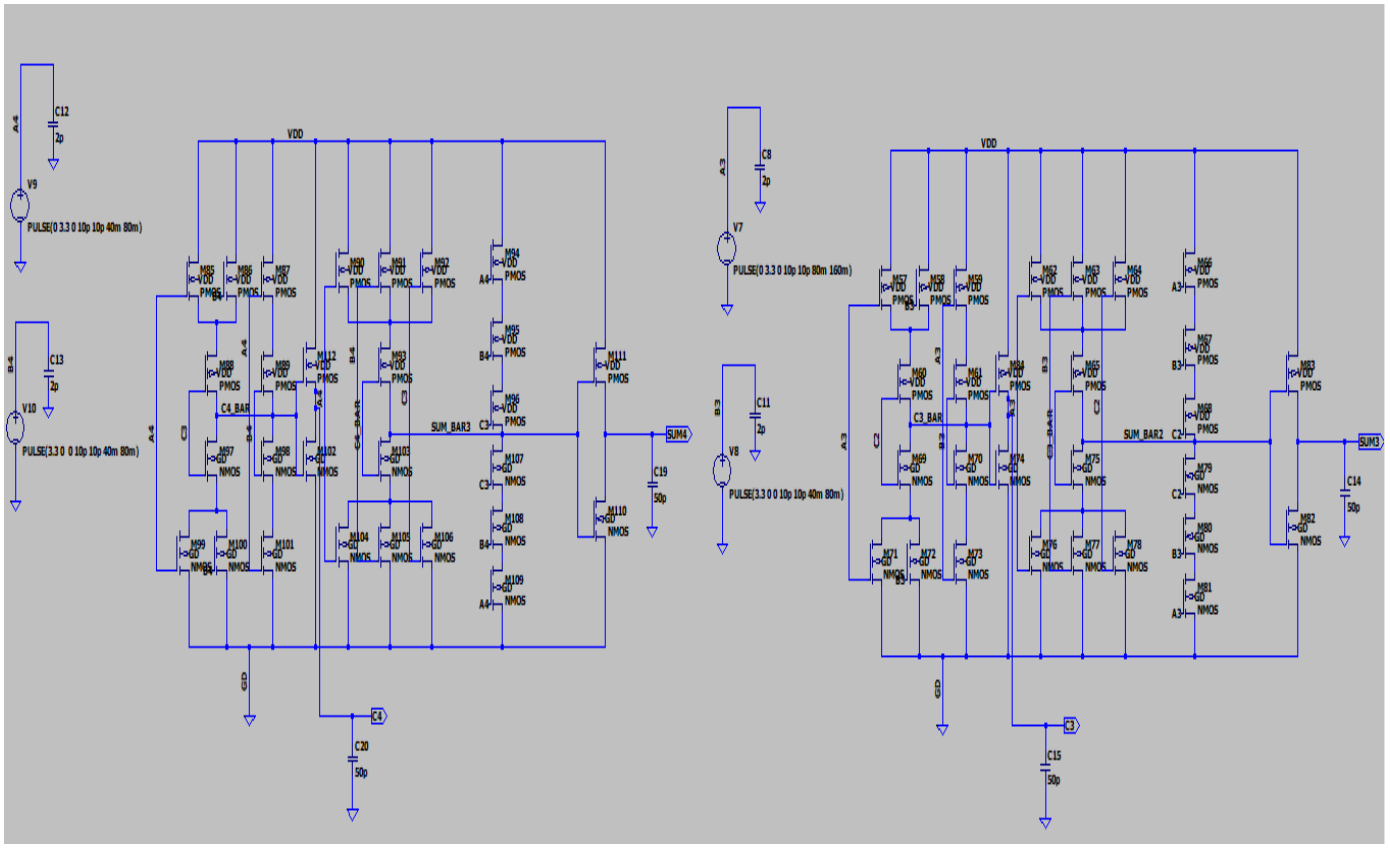
RISE DELAY=247ns

4-bit Ripple Carry Adder



(a)Schematic and spice netlist





```
M1 VDD A N013 VDD PMOS l=1u w=6u
M2 VDD B N013 VDD PMOS l=1u w=6u
M3 VDD A N017 VDD PMOS l=1u w=6u
M4 N013 Cin C1_bar VDD PMOS l=1u w=6u
M5 N017 B C1_bar VDD PMOS l=1u w=6u
M6 VDD A N014 VDD PMOS l=1u w=6u
M7 VDD B N014 VDD PMOS l=1u w=6u
M8 VDD Cin N014 VDD PMOS l=1u w=6u
M9 N014 C1_bar SUM_BAR VDD PMOS l=1u w=6u
M10 VDD A N011 VDD PMOS l=1u w=9u
M11 N011 B N020 VDD PMOS l=1u w=9u
M12 N020 Cin SUM_BAR VDD PMOS l=1u w=9u
M14 C1_bar Cin N035 0 NMOS l=1u w=2u
M16 C1_bar B N037 0 NMOS l=1u w=2u
M17 N035 A 0 0 NMOS l=1u w=2u
M18 N035 B 0 0 NMOS l=1u w=2u
M19 N037 A 0 0 NMOS l=1u w=2u
M20 C1 C1_bar 0 0 NMOS l=1u w=1u
M21 SUM_BAR C1_bar N032 0 NMOS l=1u w=2u
M22 N032 A 0 0 NMOS l=1u w=2u
M23 N032 B 0 0 NMOS l=1u w=2u
M24 N032 Cin 0 0 NMOS l=1u w=2u
M25 SUM_BAR Cin N033 0 NMOS l=1u w=3u
M26 N033 B N040 0 NMOS l=1u w=3u
M27 N040 A 0 0 NMOS l=1u w=3u
M13 SUM SUM_BAR 0 0 NMOS l=1u w=1u
M15 VDD SUM_BAR SUM VDD PMOS l=1u w=3u
M28 VDD C1_bar C1 VDD PMOS l=1u w=3u
V1 A 0 PULSE(3.3 0 0 10p 10p 20m 40m)
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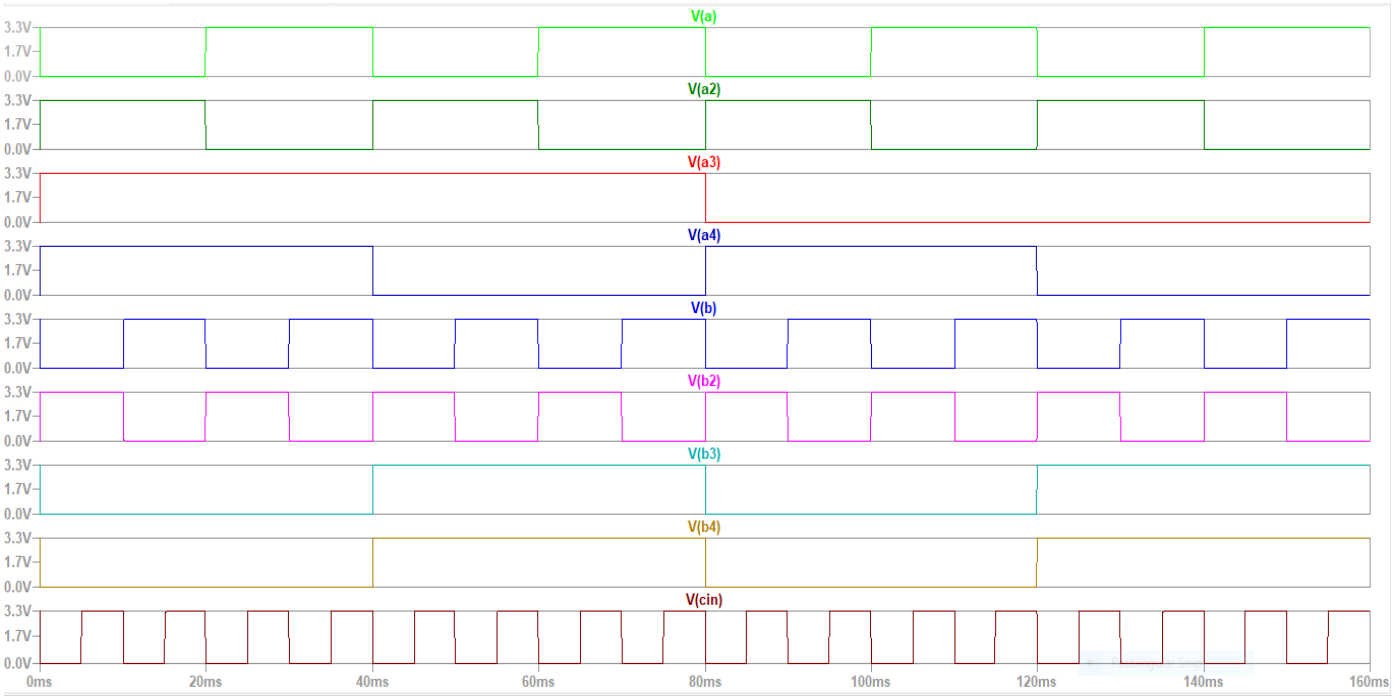
```
V2 B 0 PULSE(3.3 0 0 10p 10p 10m 20m)
V3 Cin 0 PULSE(3.3 0 0 10p 10p 5m 10m)
V4 VDD 0 3.3
C2 A 0 2p
C3 B 0 2p
C4 Cin 0 2p
C1 SUM 0 50p
C5 C1 0 50p
M29 VDD A2 N008 VDD PMOS l=1u w=6u
M30 VDD B2 N008 VDD PMOS l=1u w=6u
M31 VDD A2 N015 VDD PMOS l=1u w=6u
M32 N008 C1 C2_BAR VDD PMOS l=1u w=6u
M33 N015 B2 C2_BAR VDD PMOS l=1u w=6u
M34 VDD A2 N009 VDD PMOS l=1u w=6u
M35 VDD B2 N009 VDD PMOS l=1u w=6u
M36 VDD C1 N009 VDD PMOS l=1u w=6u
M37 N009 C2_BAR SUM_BAR1 VDD PMOS l=1u w=6u
M38 VDD A2 N007 VDD PMOS l=1u w=9u
M39 N007 B2 N019 VDD PMOS l=1u w=9u
M40 N019 C1 SUM_BAR1 VDD PMOS l=1u w=9u
M41 C2_BAR C1 N030 0 NMOS l=1u w=2u
M42 C2_BAR B2 N034 0 NMOS l=1u w=2u
M43 N030 A2 0 0 NMOS l=1u w=2u
M44 N030 B2 0 0 NMOS l=1u w=2u
M45 N034 A2 0 0 NMOS l=1u w=2u
M46 C2 C2_BAR 0 0 NMOS l=1u w=1u
M47 SUM_BAR1 C2_BAR N027 0 NMOS l=1u w=2u
M48 N027 A2 0 0 NMOS l=1u w=2u
M49 N027 B2 0 0 NMOS l=1u w=2u
M50 N027 C1 0 0 NMOS l=1u w=2u
```

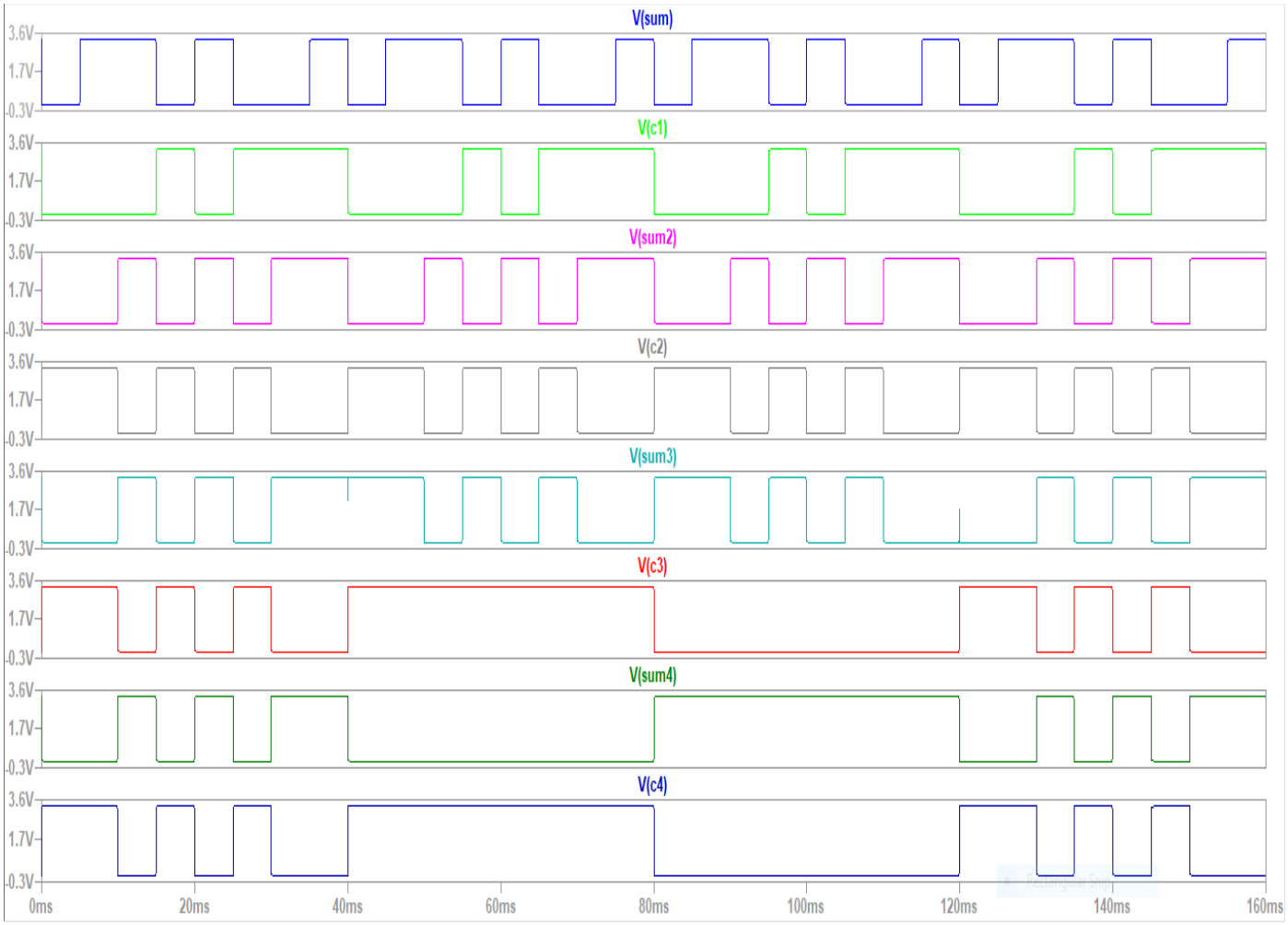
```
M51 SUM_BAR1 C1 N028 0 NMOS l=1u w=3u
M52 N028 B2 N039 0 NMOS l=1u w=3u
M53 N039 A2 0 0 NMOS l=1u w=3u
M54 SUM2 SUM_BAR1 0 0 NMOS l=1u w=1u
M55 VDD SUM_BAR1 SUM2 VDD PMOS l=1u w=3u
M56 VDD C2_BAR C2 VDD PMOS l=1u w=3u
C9 SUM2 0 50p
C10 C2 0 50p
M57 VDD A3 N005 VDD PMOS l=1u w=6u
M58 VDD B3 N005 VDD PMOS l=1u w=6u
M59 VDD A3 N012 VDD PMOS l=1u w=6u
M60 N005 C2 C3_BAR VDD PMOS l=1u w=6u
M61 N012 B3 C3_BAR VDD PMOS l=1u w=6u
M62 VDD A3 N006 VDD PMOS l=1u w=6u
M63 VDD B3 N006 VDD PMOS l=1u w=6u
M64 VDD C2 N006 VDD PMOS l=1u w=6u
M65 N006 C3_BAR SUM_BAR2 VDD PMOS l=1u w=6u
M66 VDD A3 N004 VDD PMOS l=1u w=9u
M67 N004 B3 N018 VDD PMOS l=1u w=9u
M68 N018 C2 SUM_BAR2 VDD PMOS l=1u w=9u
M69 C3_BAR C2 N026 0 NMOS l=1u w=2u
M70 C3_BAR B3 N031 0 NMOS l=1u w=2u
M71 N026 A3 0 0 NMOS l=1u w=2u
M72 N026 B3 0 0 NMOS l=1u w=2u
M73 N031 A3 0 0 NMOS l=1u w=2u
M74 C3 C3_BAR 0 0 NMOS l=1u w=1u
M75 SUM_BAR2 C3_BAR N024 0 NMOS l=1u w=2u
M76 N024 A3 0 0 NMOS l=1u w=2u
M77 N024 B3 0 0 NMOS l=1u w=2u
M78 N024 C2 0 0 NMOS l=1u w=2u
```

```
M79 SUM_BAR2 C2 N025 0 NMOS l=1u w=3u
M80 N025 B3 N038 0 NMOS l=1u w=3u
M81 N038 A3 0 0 NMOS l=1u w=3u
M82 SUM3 SUM_BAR2 0 0 NMOS l=1u w=1u
M83 VDD SUM_BAR2 SUM3 VDD PMOS l=1u w=3u
M84 VDD C3_BAR C3 VDD PMOS l=1u w=3u
C14 SUM3 0 50p
C15 C3 0 50p
M85 VDD A4 N002 VDD PMOS l=1u w=6u
M86 VDD B4 N002 VDD PMOS l=1u w=6u
M87 VDD A4 N010 VDD PMOS l=1u w=6u
M88 N002 C3 C4_BAR VDD PMOS l=1u w=6u
M89 N010 B4 C4_BAR VDD PMOS l=1u w=6u
M90 VDD A4 N003 VDD PMOS l=1u w=6u
M91 VDD B4 N003 VDD PMOS l=1u w=6u
M92 VDD C3 N003 VDD PMOS l=1u w=6u
M93 N003 C4_BAR SUM_BAR3 VDD PMOS l=1u w=6u
M94 VDD A4 N001 VDD PMOS l=1u w=9u
M95 N001 B4 N016 VDD PMOS l=1u w=9u
M96 N016 C3 SUM_BAR3 VDD PMOS l=1u w=9u
M97 C4_BAR C3 N023 0 NMOS l=1u w=2u
M98 C4_BAR B4 N029 0 NMOS l=1u w=2u
M99 N023 A4 0 0 NMOS l=1u w=2u
M100 N023 B4 0 0 NMOS l=1u w=2u
M101 N029 A4 0 0 NMOS l=1u w=2u
M102 C4 C4_BAR 0 0 NMOS l=1u w=1u
M103 SUM_BAR3 C4_BAR N021 0 NMOS l=1u w=2u
M104 N021 A4 0 0 NMOS l=1u w=2u
M105 N021 B4 0 0 NMOS l=1u w=2u
M106 N021 C3 0 0 NMOS l=1u w=2u
```

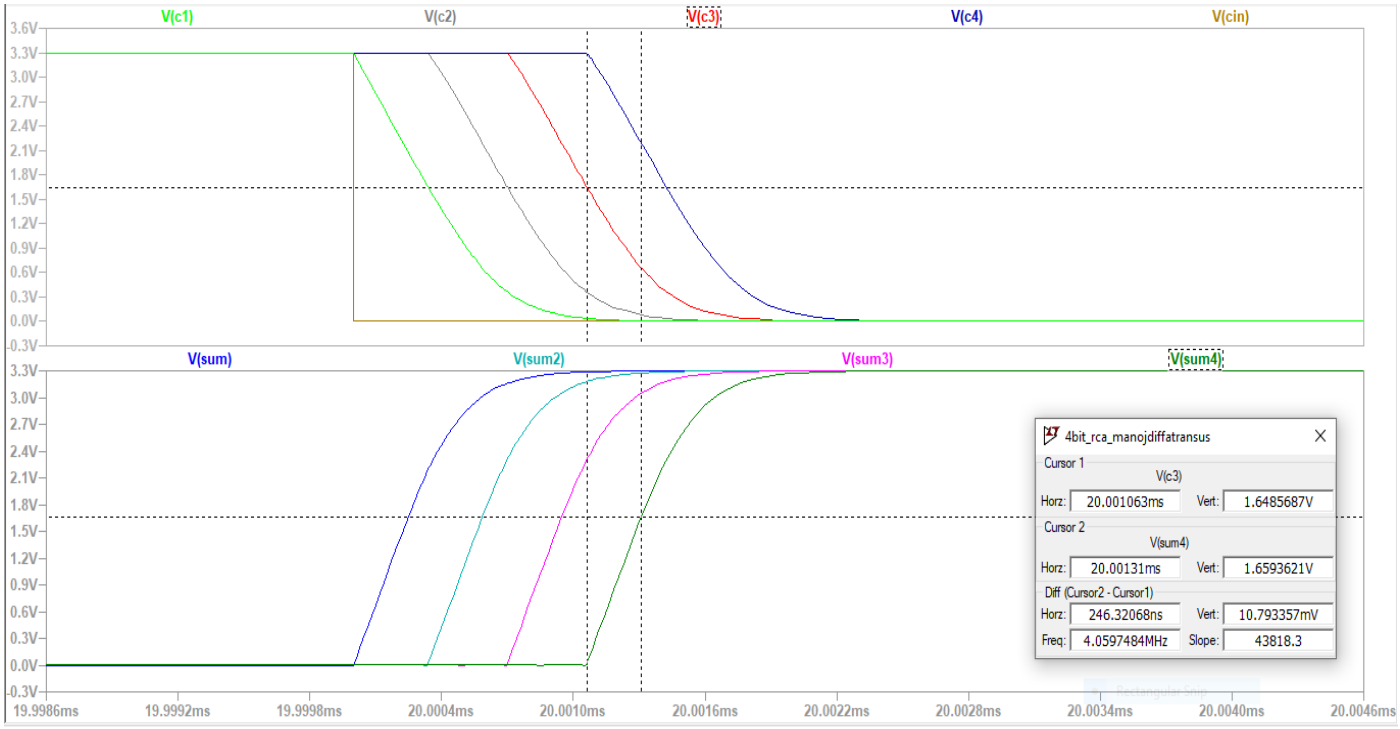
```
M106 N021 C3 0 0 NMOS l=1u w=2u
M107 SUM_BAR3 C3 N022 0 NMOS l=1u w=3u
M108 N022 B4 N036 0 NMOS l=1u w=3u
M109 N036 A4 0 0 NMOS l=1u w=3u
M110 SUM4 SUM_BAR3 0 0 NMOS l=1u w=1u
M111 VDD SUM_BAR3 SUM4 VDD PMOS l=1u w=3u
M112 VDD C4_BAR C4 VDD PMOS l=1u w=3u
C19 SUM4 0 50p
C20 C4 0 50p
V5 A2 0 PULSE(0 3.3 0 10p 10p 20m 40m)
V6 B2 0 PULSE(0 3.3 0 10p 10p 10m 20m)
C6 A2 0 2p
C7 B2 0 2p
V7 A3 0 PULSE(0 3.3 0 10p 10p 80m 160m)
V8 B3 0 PULSE(3.3 0 0 10p 10p 40m 80m)
C8 A3 0 2p
C11 B3 0 2p
V9 A4 0 PULSE(0 3.3 0 10p 10p 40m 80m)
V10 B4 0 PULSE(3.3 0 0 10p 10p 40m 80m)
C12 A4 0 2p
C13 B4 0 2p
.model NMOS NMOS
.model PMOS PMOS
.lib C:\Users\Manoj Kumar Singh\Documents\
.tran 160m
```

(b)simulation results





DELAY



As you can clearly see carry C3 comes before sum4.Similarly Cin,C1,C2,C3 comes before sum1,sum2,sum3 and sum4 respectively.So, our 4 bit ripple carry adder works perfectly.

DELAY IN CARRY C3=1063ns

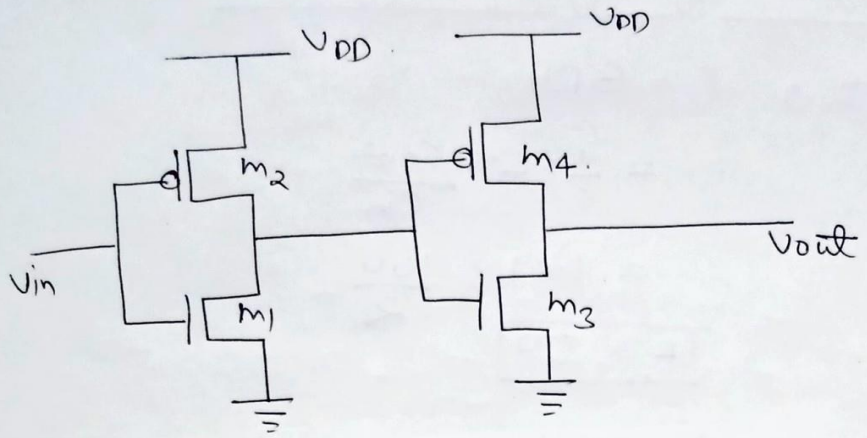
DELAY IN SUM4=1310ns

Example:From 4bit RCA wavefrom , at the starting first edge:

	X4	X3	X2	X1
Cin				0
A	1	1	1	0
B	0	0	1	0
SUM	0	0	0	0
CARRY OUT	1	1	1	0

QUESTION 2: **Design a superbuffer using CMOS inverters to drive a load of 100 fF, assume the input capacitance to be 2 fF.**

(A)Detailed calculation and sizing of transistors



SUPER BUFFER

Regular cmos inverter has pullup & pull down X-sistors which do not have equal charging, discharging times when dealing with O/P capacitor due to inherent carrier mobility. Thus, having an inverter to drive any off-chip large capr (or) some other critical circuitry is not a reliable solution (assymetric rise, fall delays).

In contrast to this super-buffers have good drive strength & provides symmetric driving behaviour (equal rise & fall times.) A super buffer has 4 internal X-sistors whose (W/L) ratios & connections gives better char. of charging/discharging O/P node cap. with symmetrical rise, fall delays.

By the method of Logical Effort :-

Path Effort, $F = GBH$

$= 1 \times 1 \times \frac{C_{out}}{C_{in}}$

$= 1 \times 1 \times \frac{160}{2}$

$\boxed{F = 50}$

Best no. of stages, $\hat{N} = \log_4(F)$

$= \log_4(50)$

$\boxed{\hat{N} = 2.82}$

For $N = 2$,

Delay, $d = NF^{1/N} + P$

$= 2(50)^{1/2} + 2$

$\boxed{d = 16.14 \text{ units}}$

For $N = 3$,

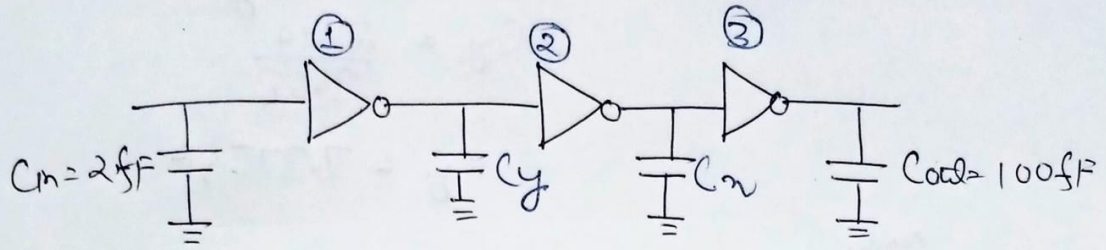
$d = NF^{1/N} + P$

$= 3(50)^{1/3} + 3$

$\boxed{d = 14.057}$

So, for optimum/least delay we select $\boxed{N = 3}$ for our design.

Calculation of parasitic capacitances & $(\frac{W}{L})$ ratio



$$\therefore \hat{f} = F^{1/4} = g_1h_1 = g_2h_2 = g_3h_3 \quad \text{—(i)}$$

(8) $$\therefore \hat{f} = g_3h_3 \Rightarrow (50)^{1/3} = g_3 \times \frac{100}{C_n}$$

$$C_n = \frac{100}{3.68}$$

$$\boxed{C_n = 27.14\,fF}$$

Now,

For Level 3, $\mu_n : \mu_p = 660 : 210$

$$= 3.14 : 1$$

$$\boxed{\mu_n : \mu_p \simeq 3 : 1}$$

$$\therefore (L \cdot C_{ox})(4W) = C_n$$

$$\Rightarrow (1\times10^{-6})(24.65\times10^{-4}\,F/m^2)(4W) = 27.14\times10^{-15}$$

$$\Rightarrow W = 2.755\times10^{-6}$$

$$\boxed{W = 2.755\,\mu m}$$

$$C_{ox} = \frac{\epsilon_0 \epsilon_{ox}}{t_{ox}} = \frac{3.9\times8.85\times10^{-12}}{1.4\times10^{-8}\,m}$$

$$\boxed{C_{ox} = 24.65\times10^{-4}\,F/m^2}$$

$$\boxed{\begin{aligned} &P\text{-}MOS_3 \Rightarrow 3W = 8.25\,\mu m \\ &NMOS_3 \Rightarrow \ \ W = 2.75\,\mu m \end{aligned}} \quad \text{—(ii)}$$

(ii) $f = g_2 h_2 \Rightarrow 3.68 = 1 \times \frac{C_m}{C_y}$

$C_y = \frac{27.14}{3.68}$

$C_y = 7.375 fF$

Now,

$(L \cdot C_{ox}) 4n = 7.375 fF$

$(1 \times 10^{-6}) \times (24.65 \times 10^{-4}) \cdot (4n) = 7.375 \times 10^{-15}$

$n = 0.748 \mu m$

pmos $\Rightarrow 3n = 2.22 \mu m$

nmos $\Rightarrow n = 0.748 \mu m$

(iii) $f = g_1 h_1 \Rightarrow 3.68 = 1 \times \frac{C_y}{C_a}$

$C_a = \frac{7.375}{3.68} = 2 fF$

$\therefore (L \cdot C_{ox}) 4n = 2 fF$

$(1 \times 10^{-6}) \times (24.65 \times 10^{-4}) (4n) = 2 \times 10^{-15}$

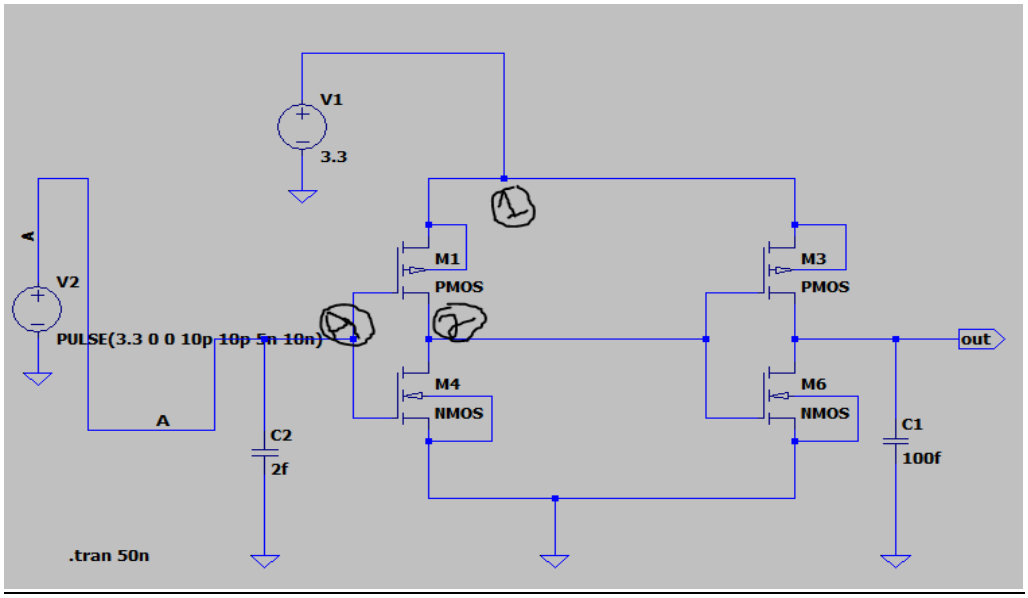
$n = 0.202 \mu m$

$\therefore$ pmos $\Rightarrow 3n = 0.608 \mu m$

nmos $\Rightarrow n = 0.202 \mu m$

(B)SPICE NETLIST

- Without optimisation

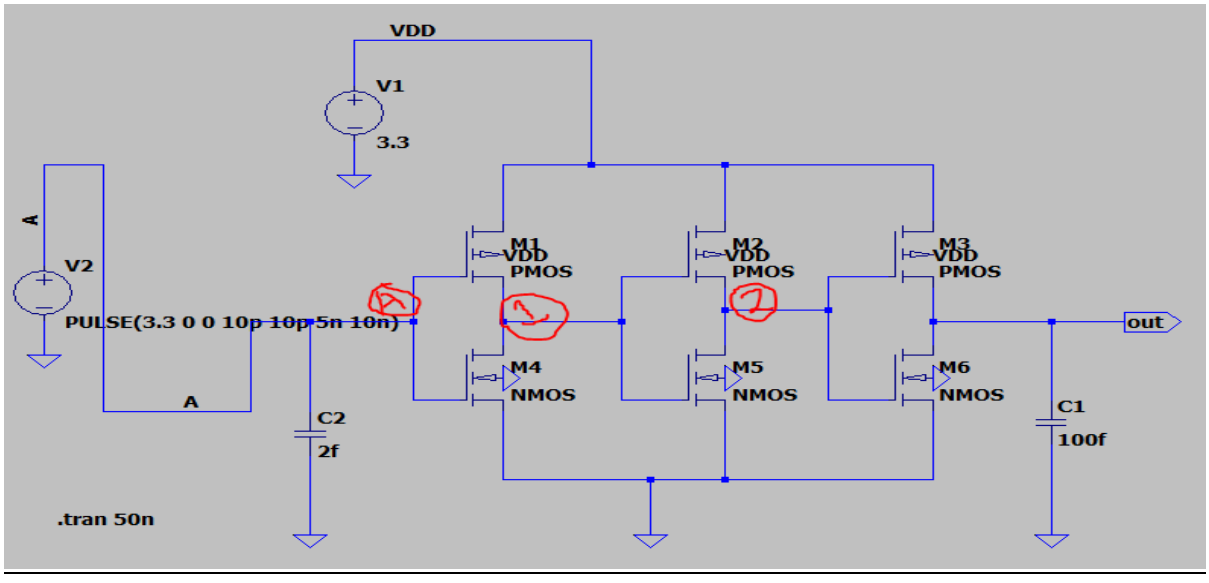



```
M1 1 A 2 1   PMOS l=1u w=3u
M3 1 2 out 1 PMOS l=1u w=3u
M6 out 2 0 0 NMOS l=1u w=1u
M4 2 A 0 0   NMOS l=1u w=1u
V1 N001 0 3.3

V2 A 0 PULSE(3.3 0 0 10p 10p 5n 10n)
C1 out 0 100f
C2 A 0 2f

.model NMOS NMOS
.model PMOS PMOS
.tran 50n
```

- Optimised



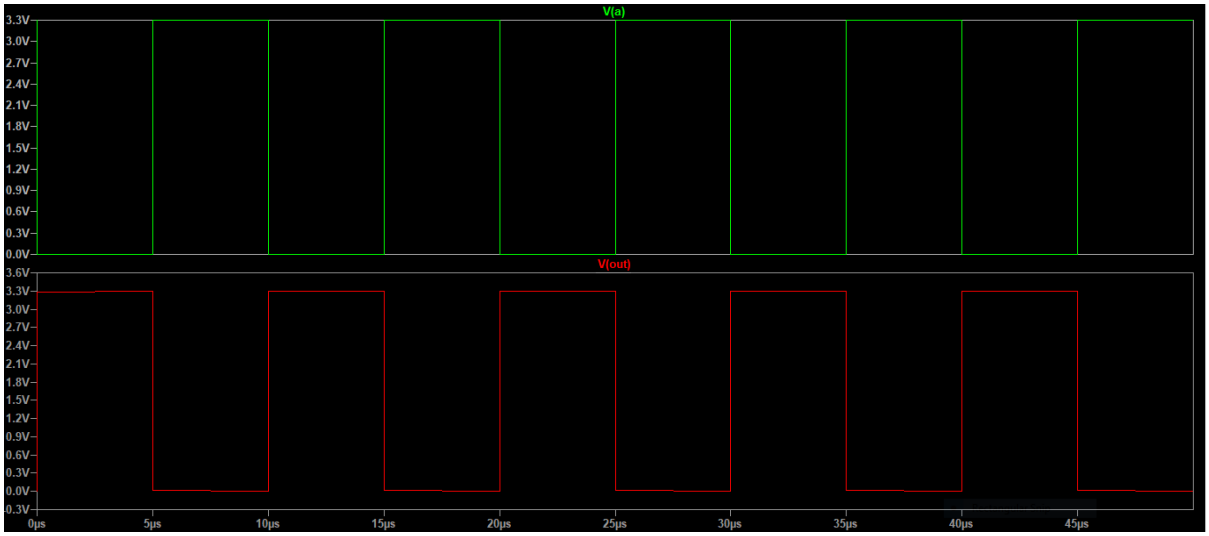
```
M1 VDD A 1 VDD    PMOS l=1u w=0.61u
M2 VDD 1 2 VDD    PMOS l=1u w=2.22u
M3 VDD 2 out VDD  PMOS l=1u w=8.25u
M5 2   1 0 0      NMOS l=1u w=0.75u
M6 out 2 0 0      NMOS l=1u w=2.75u
M4 1 A 0 0        NMOS l=1u w=0.20u

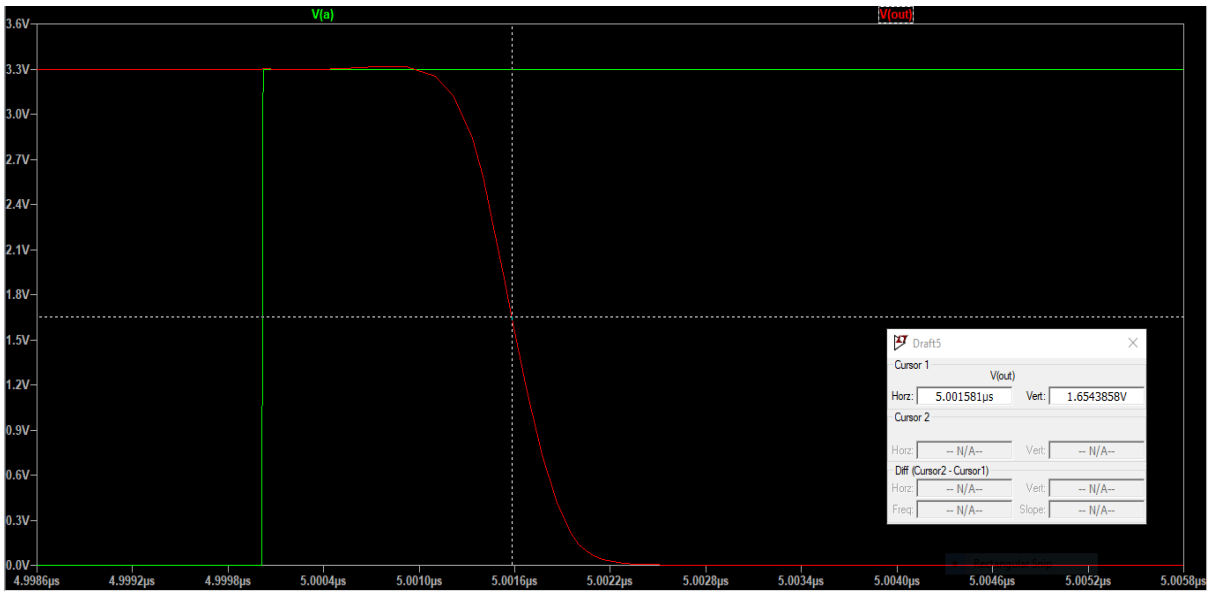
V1 VDD 0 3.3
V2 A 0 PULSE(3.3 0 0 10p 10p 5n 10n)

C1 out 0 100f
C2 A 0 2f

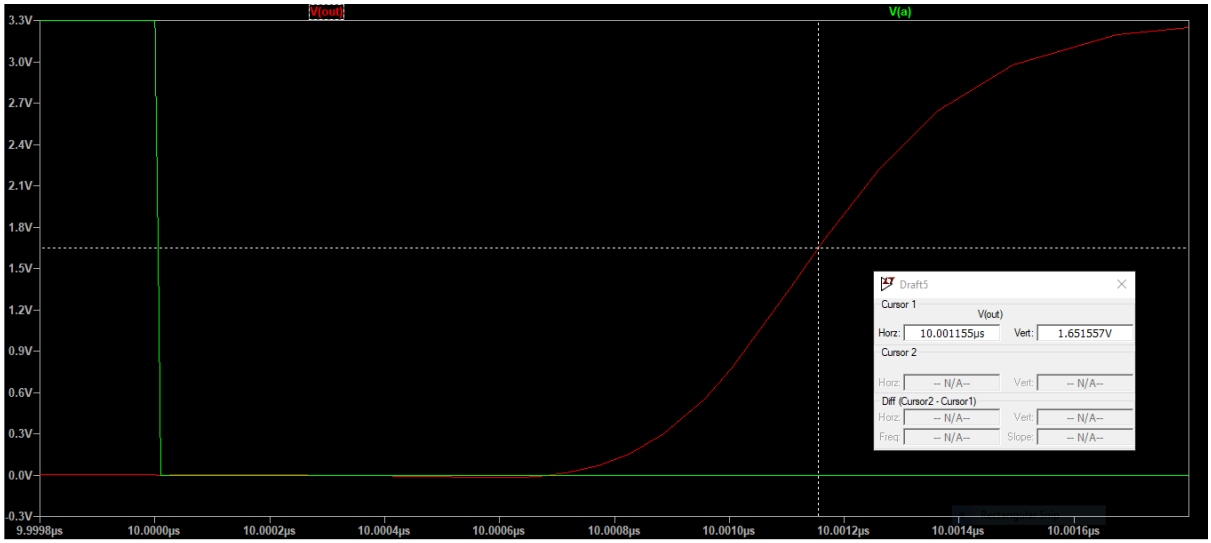
.model NMOS NMOS
.model PMOS PMOS
.tran 50n
```

(C) Simulation result and calculation of delay





FALL DELAY=1.581ns



RISE DELAY=1.155ns