CSN6114 - COMPUTER ARCHITECTURE & ORGANIZATION

TITLE :

ASSIGNMENT 1

LECTURE SECTION :

TC6L

TUTORIAL SECTION :

T21L

GROUP :

GROUP 3

No	Student ID	Name	Email
1	1211111809	MARYAM BINTI NORAZMAN	1211111809@soffice.mmu.edu.my
2	1211112284	NUR DANIA IMAN BINTI DESMAN DESA	1211112284@soffice.mmu.edu.my
3	1191100306	NURILL NABILLA BINTI HASLIN	1191100306@soffice.mmu.edu.my
4	1221103588	NURUL SYAHAFIZA BINTI NAZIRON	1221103588@soffice.mmu.edu.my

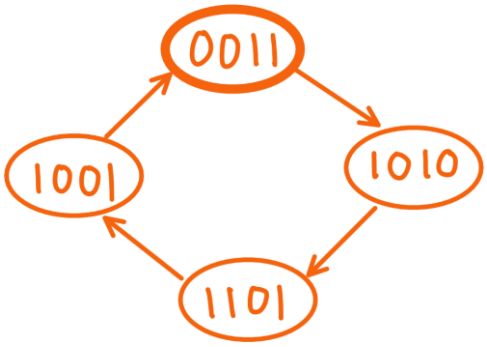
Problem Statement:

Design a 4-bit counter with one external input using D flip-flop. The circuit will receive a one-bit input. Different input will have different count sequences as shown in the table below.

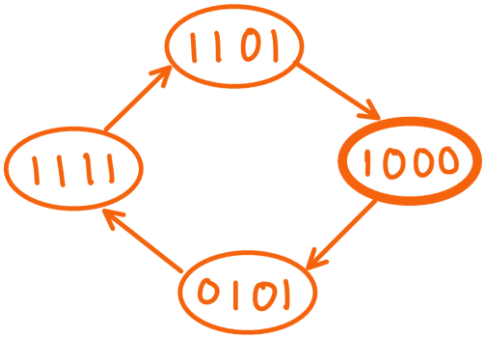
Input	Count Sequence	Push the undesired states to
0	9 -> 3 -> 10 -> 13	3
1	13 -> 8 -> 5 -> 15	8

i) State Transition Diagram

Input 0



Input 1



ii) State Transition Table

Input	Present				Next								
	A	B	C	D	A	B	C	D	DA	DB	DC	DD	Position in Decimal
0	0	0	0	0	0	0	1	1	0	0	1	1	0
0	0	0	0	1	0	0	1	1	0	0	1	1	1
0	0	0	1	0	0	0	1	1	0	0	1	1	2
0	0	0	1	1	1	0	1	0	1	0	1	0	3
0	0	1	0	0	0	0	1	1	0	0	1	1	4
0	0	1	0	1	0	0	1	1	0	0	1	1	5
0	0	1	1	0	0	0	1	1	0	0	1	1	6
0	0	1	1	1	0	0	1	1	0	0	1	1	7
0	1	0	0	0	0	0	1	1	0	0	1	1	8
0	1	0	0	1	0	0	1	1	0	0	1	1	9
0	1	0	1	0	1	1	0	1	1	1	0	1	10
0	1	0	1	1	0	0	1	1	0	0	1	1	11
0	1	1	0	0	0	0	1	1	0	0	1	1	12
0	1	1	0	1	1	0	0	1	1	0	0	1	13
0	1	1	1	0	0	0	1	1	0	0	1	1	14
0	1	1	1	1	0	0	1	1	0	0	1	1	15
1	0	0	0	0	1	0	0	0	1	0	0	0	16
1	0	0	0	1	1	0	0	0	1	0	0	0	17
1	0	0	1	0	1	0	0	0	1	0	0	0	18
1	0	0	1	1	1	0	0	0	1	0	0	0	19
1	0	1	0	0	1	0	0	0	1	0	0	0	20
1	0	1	0	1	1	1	1	1	1	1	1	1	21
1	0	1	1	0	1	0	0	0	1	0	0	0	22
1	0	1	1	1	1	0	0	0	1	0	0	0	23
1	1	0	0	0	0	1	0	1	0	1	0	1	24
1	1	0	0	1	1	0	0	0	1	0	0	0	25
1	1	0	1	0	1	0	0	0	1	0	0	0	26
1	1	0	1	1	1	0	0	0	1	0	0	0	27
1	1	1	0	0	1	0	0	0	1	0	0	0	28
1	1	1	0	1	1	0	0	0	1	0	0	0	29
1	1	1	1	0	1	0	0	0	1	0	0	0	30
1	1	1	1	1	1	1	0	1	1	1	0	1	31

iii) Simplification Using K Map

Input 0

DA

Input = 0						Input = 1				
AB\CD	00	01	11	10		AB\CD	00	01	11	10
00	0	0	1	0		00	1	1	1	1
01	0	0	0	0		01	1	1	1	1
11	0	1	0	0		11	1	1	1	1
10	0	0	0	1		10	0	1	1	1

DA = Input 0 (ABC'D + A'B'CD + AB'CD') + Input 1 (A' + B + C + D)

= Input (A' + B + C + D)

DB

Input = 0						Input = 1				
AB\CD	00	01	11	10		AB\CD	00	01	11	10
00	0	0	0	0		00	0	0	0	0
01	0	0	0	0		01	0	1	0	0
11	0	0	0	0		11	0	0	0	0
10	0	0	0	1		10	1	0	0	0

DB = Input 0 (AB'CD') + Input 1 (AB'C'D' + A'BC'D)

= Input (AB'C'D' + A'BC'D)

DC

Input = 0						Input = 1				
AB\CD	00	01	11	10		AB\CD	00	01	11	10
00	1	1	1	1		00	0	0	0	0
01	1	1	1	1		01	0	1	0	0
11	1	0	1	1		11	0	0	0	0
10	1	1	1	0		10	0	0	0	0

DC = Input 0(A' + CD + B'C' + BD') + Input 1(A'BC'D)

= Input (A'BC'D)

DD

AB\CD	00	01	11	10		AB\CD	00	01	11	10
00	1	1	0	1		00	0	0	0	0
01	1	1	1	1		01	0	1	0	0

11	1	1	1	1		11	0	0	0	0
10	1	1	1	1		10	1	0	0	0

DD = Input 0(A + B + C’ + D’) + Input 1(A’BC’D + AB’C’D’)

= Input (A’BC’D + AB’C’D’)

iv) Circuitverse Snapshot

4-bit D Flip Flop