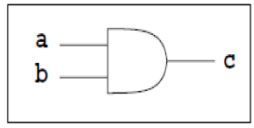
Verilog Test – SmartIOPS Inc

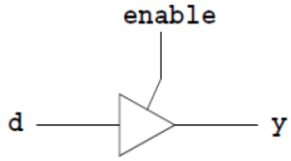
Note: Test bench must be written for all Verilog codes and simple Make file for questasim

Part -A

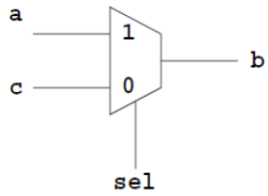
1 ▪ **For the following diagram**
- **Write verilog model using following modeling styles**
  - **gate level**
  - **continuous assignment**
  - **behavioral**



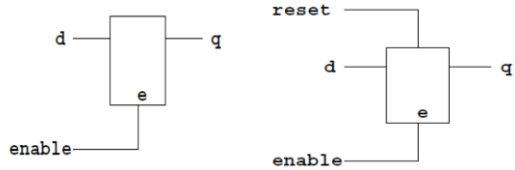
2 ▪ **For the following diagram**
- **Write verilog model using following modeling styles**
  - **gate level**
  - **continuous assignment**
  - **Behavioral**
- **Name the h/w**



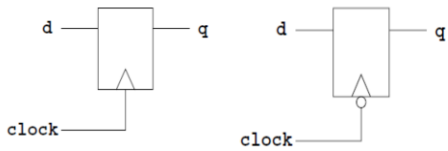
3 ▪ **For the following diagram**
- **Write verilog model using following modeling styles**
  - **continuous assignment**
  - **behavioral**
- **Name the h/w**



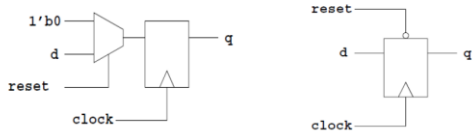
4 ▪ **For the following diagrams**
- **Write the behavioral verilog model**
- **Name the h/w**



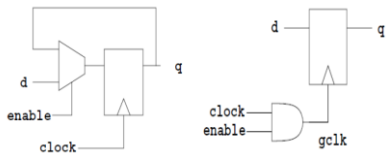
5 ▪ **For the following diagrams**
- **Write the behavioral verilog model**
- **Name the h/w**



6 ▪ **For the following diagrams**
- **Write the behavioral verilog model**
- **Name the h/w**



7 ▪ **For the following diagrams**
- **Write the behavioral verilog model**
- **Name the h/w**



8 **For the following code**

- **Draw the schematic and name the h/w**

```
output reg[3:0] Q;
input clk, reset;
reg [3:0] d = 3'b001;
always @ (posedge clk or posedge reset)
begin
 if (reset)
   Q <= d;
 else begin
   Q <= Q << 1;
   Q[0] <= Q[3];
 end
end
```

Part - B

9 Write a Verilog code for 1KB size of 32datawidth synchronous FIFO

10 Write RTL for an asynchronous FIFO with the following specifications. The FIFO must have optimal depth.
Writing frequency = fA = 100MHz.
Reading Frequency = fB = 40MHz.
Burst Length = No. of data items to be transferred = 100.
No. of idle cycles between two successive writes is = 1.
No. of idle cycles between two successive reads is = 3.

11. Write RTL for the following Sequence Detectors

Name of the candidate	Sequence	Overlap/Non-Overlap	Mealy -Moore
Aadithya	110011	nonoverlap	Moore
Jayasree	111000	nonoverlap	Mealy
Karthik	110110	nonoverlap	Moore
Lavanya	001001	nonoverlap	Mealy
Mathibala	101010	nonoverlap	Mealy
Nalina	101010	overlap	Mealy
Perumal	110110	overlap	Mealy
Suriyamanikandan	001001	overlap	Moore
Thanavignesh	111000	overlap	Mealy
Vinupriya	110011	overlap	Moore