Chapter 11
Read Noise

11.1 Introduction

The first data points collected by a PTC typically measure the read noise floor. This chapter reviews common CCD and CMOS read noise sources and their unique influence on PTCs. Table 11.1 lists the noise types in the order they will be presented. The general read noise equation is given by

$$\sigma_{\mathrm{READ}} = (\sigma_{\mathrm{SF}}^2 + \sigma_{\mathrm{RESET}}^2 + \sigma_{\mathrm{D\_SHOT}}^2 + \sigma_{\mathrm{D\_FPN}}^2 + \sigma_{\mathrm{ADC}}^2 + \sigma_{\mathrm{OFF\_FPN}}^2 + \sigma_{\mathrm{SY}}^2)^{1/2}. \tag{11.1}$$

It is important to point out that Eq. (11.1) is applied to all equations in the previous chapters that contain the term σ_{READ}.

11.2 Pixel Source Follower Noise

Ultimately, a pixel's source follower MOSFET, shown in Fig. 4.3, limits the read noise floor. Fortunately, other noise sources can usually be reduced to negligible levels relative to source follower noise. For example, dark current noise is removed by cooling the sensor to a low operating temperature. Remarkably, source follower noise for high-performance CMOS and CCD cameras have been driven down to approximately one noise electron rms.

To provide the reader some insight to the variables behind source follower read noise, we present a general formula that theoretically determines its amplitude. In

Table 11.1 Types of noise.

Noise Source	Symbol
Pixel source follower noise	σ_{SF}
Sense node reset noise	σ_{RESET}
Thermal dark current shot noise	$\sigma_{\mathrm{D\_SHOT}}$
Dark current FPN	$\sigma_{\mathrm{D\_FPN}}$
ADC quantizing noise	σ_{ADC}
Offset FPN	σ_{OFF}
System noise	σ_{SY}

electron units, the noise source is given by

$$\sigma_{\mathrm{SF}} = \frac{1}{\mathrm{A_{SN}A_{SF}}(1 - e^{-t_{\mathrm{s}}/\tau_{\mathrm{D}}})} \left[\int_0^{\infty} S_{\mathrm{DET}}(f) H_{\mathrm{CDS}}(f) df \right]^{1/2}, \tag{11.2}$$

where σ_{SF} is the source follower noise (e^- rms), f is electrical frequency (Hz), t_{s} is the correlated double sampling (CDS) sample-to-sample time (sec), and τ_{D} is the CDS dominant time constant.[1] $H_{\mathrm{CDS}}(f)$ is the CDS transfer function, expressed as

$$H_{\mathrm{CDS}}(f) = \left[\frac{1}{1 + (2\pi f \tau_{\mathrm{D}})^2} \right] [2 - 2\cos(2\pi f t_{\mathrm{s}})]. \tag{11.3}$$

The second term of Eq. (11.3) describes the frequency response of the CDS processor. The first term sets the CDS bandwidth for white noise rejection before sampling takes place through

$$B = \frac{1}{4\tau_{\mathrm{D}}}, \tag{11.4}$$

where B is defined as the equivalent noise bandwidth (Hz). The dominant time constant is nominally set to $\tau_{\mathrm{D}} = 0.5 t_{\mathrm{s}}$ for high-performance camera systems.

Pixel source follower MOSFET noise is composed of three components: white noise, flicker noise, and random telegraph signal (RTS) noise. In the frequency domain, the source follower's output noise power spectrum, $S_{\mathrm{DET}}(f)$, is given by

$$S_{\mathrm{DET}}(f) = W(f)^2 \left(1 + \frac{f_{\mathrm{c}}}{f} \right) + S_{\mathrm{RTS}}(f), \tag{11.5}$$

where $W(f)$ is the thermal white noise (V/Hz$^{1/2}$), f_{c} is the flicker noise corner frequency (i.e., the frequency where white and flicker noise are equal), and $S_{\mathrm{RTS}}(f)$ is the RTS noise power given by

$$S_{\mathrm{RTS}}(f) = \frac{2\Delta I^2 \tau_{\mathrm{RTS}}}{4 + (2\pi f \tau_{\mathrm{RTS}})^2}, \tag{11.6}$$

where τ_{RTS} is the RTS characteristic time constant (sec), and ΔI is the source follower current modulation induced by RTS (A). For CCD imagers, source follower noise is typically limited by flicker noise, whereas CMOS detectors are limited by RTS.[5]

Example 11.1

Plot the source follower read noise as a function of CDS sample-to-sample time, given the following parameters:

$W(f) = 15$ nV/Hz$^{1/2}$
$A_{\mathrm{SF}} = 0.9$ V/V

$$\tau_{\mathrm{D}} = 0.5t_{\mathrm{s}}$$
$$A_{\mathrm{SN}} = 6\ \mu\mathrm{V/e}^{-}$$
$$S_{\mathrm{RTS}}(f) = 0$$

Assume $f_{\mathrm{c}} = 10^3$, 10^4, 10^5, and 10^6 Hz.

Solution:
Applying Eq. (11.2), Fig. 11.1 shows the desired noise plots. Note that read noise decreases by the square root of t_{s} (or $2\tau_{\mathrm{D}}$) and levels out when the $1/f$ corner frequency is encountered (approximately at $t_{\mathrm{s}} = 1/f_{\mathrm{c}}$).

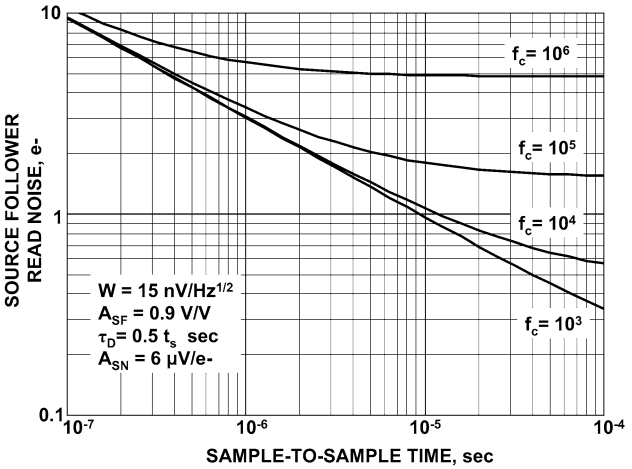

Figure 11.1 Source follower noise (rms e^{-}) with sample time for different $1/f$ corner frequencies.

11.3 Sense Node Reset Noise

Reset noise voltage is thermally generated by the channel resistance associated with the reset MOSFET induced on the sense node capacitor (refer to Fig. 4.3).[1] As a result, the sense node reference voltage is different each time a pixel is reset. Reset noise voltage is given by

$$\sigma_{\mathrm{RESET}}(V_{\mathrm{SN}}) = (4kTBR)^{1/2}, \tag{11.8}$$

where $\sigma_{\mathrm{RESET}}(V_{\mathrm{SN}})$ is the reset noise voltage (rms V), R is the MOSFET channel resistance (ohms), k is Boltzmann's constant (1.38×10^{-23} J/K), and T is the operating temperature (K).

Substituting $B = 1/4\tau$ into Eq. (11.8) yields

$$\sigma_{\mathrm{RESET}}(V_{\mathrm{SN}}) = \left(\frac{kTR}{\tau}\right)^{1/2}. \tag{11.9}$$

Noting that $\tau = RC_{\rm SN}$, Eq. (11.9) can be simplified to

$$\sigma_{\rm RESET}(V_{\rm SN}) = \left(\frac{kT}{C_{\rm SN}}\right)^{1/2}. \tag{11.10}$$

And since $C_{\rm SN} = q/V_{\rm SN}$, reset noise in terms of noise electrons is

$$\sigma_{\rm RESET} = \left(\frac{kTC_{\rm SN}}{q}\right)^{1/2}. \tag{11.11}$$

Note that Eqs. (11.10) and (11.11) appear to be in conflict. According to Eq. (11.10), reset noise voltage is lowered by increasing the sense node capacitance. On the other hand, Eq. (11.11) indicates that decreasing the capacitance is the best strategy. Obviously, for high S/N performance, it is desirable to have the number of noise electrons as low as possible because a photo-generated signal is composed of electrons. Therefore, Eq. (11.10) can be misleading. Together these equations serve as a good example for why noise (and other) measurements need to be made in the absolute units provided by photon transfer.

Assuming $C_{\rm SN} = q/A_{\rm SN}$, reset noise also can be expressed in terms of sense node gain as

$$\sigma_{\rm RESET} = \left(\frac{kT}{qA_{\rm SN}}\right)^{1/2}, \tag{11.12}$$

and

$$\sigma_{\rm RESET}(V_{\rm SN}) = \left(\frac{kTA_{\rm SN}}{q}\right)^{1/2}. \tag{11.13}$$

Note that low reset noise is achieved by making sense node gain as high as possible in terms of noise electrons.

Example 11.2

Determine the reset noise for a sense node gain of 1 μV/e$^-$. Express in electron and voltage units. Assume $T = 300$ K.

Solution:
From Eqs. (11.12) and (11.13), the reset noise on the sense node is

$$\sigma_{\rm RESET} = \left\{(1.38\times10^{-23})\times\frac{300}{[(1.6\times10^{-19})\times10^{-6}]}\right\}^{1/2} = 160\ {\rm e}^-\ {\rm rms},$$

and

$$\sigma_{\rm RESET}(V_{\rm SN}) = \left[(1.38\times10^{-23})\times\frac{300\times10^{-6}}{(1.6\times10^{-19})}\right]^{1/2} = 1.6\times10^{-4}\ {\rm V\ rms}.$$

For CCDs, reset noise is entirely removed by CDS signal processing, and therefore it is not an issue. However, it is difficult to remove reset noise for specific CMOS pixel architectures even if CDS processing is employed. For these pixels, reset noise increases by $2^{1/2}$ after CDS processing is applied because two samples are differenced. Two popular CMOS readout modes that exhibit this difficulty are referred to as "rolling shutter" and "snap."[6,7] Figure 11.2 presents a family of PTCs for these modes showing reset noise levels before and after CDS processing. The PTCs demonstrate that reset noise is significantly greater than the 5 e^- source follower noise that was assumed in the simulation. For example, a state-of-the-art sense node gain of 50 $\mu V/e^-$ generates 24 e^- of reset noise before CDS processing (as shown). A gain of 1000 $\mu V/e^-$ would be required to reduce reset noise to 5 e^-, which corresponds to a sense node capacitance of only 0.15 fF (this is not possible through design). Eliminating reset noise for CMOS imagers is briefly discussed in Sec. 11.6.

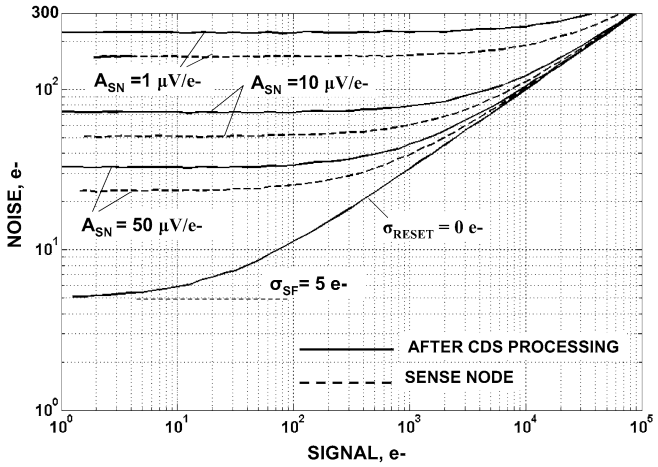

Figure 11.2 PTC responses for different sense node gains (V/e^-) compared to the ideal source follower noise without reset noise.

11.4 Dark Current Noise

All pixels naturally generate an unwanted source of charge, referred to as dark current. Although many kinds of dark current sources exist, thermally generated dark current is the most common source. The amount of dark charge produced varies from pixel to pixel, which contributes to the read noise floor. Two forms of thermal dark current noise exist: dark shot noise and dark FPN. The shot noise component is given by

$$\sigma_{\mathrm{D\_SHOT}} = (D)^{1/2}, \tag{11.14}$$

where D is the average dark current (e^-) given as

$$D = t_I D_R, \tag{11.15}$$

where t_I is the integration time allowed to collect dark charge (sec). D_R is the average dark current rate (e^-/sec/pixel) given by[1]

$$D_R = 2.55 \times 10^{15} P_A D_{FM} T^{1.5} e^{-E_g/(2kT)}, \tag{11.16}$$

where P_A is the pixel area (cm^{-2}); D_{FM} is the dark current figure-of-merit at 300 K (nA/cm^2), which varies significantly depending on the sensor manufacturer; k is Boltzmann's constant (8.62×10^{-5} eV/K); and E_g is the silicon bandgap energy given as

$$E_g = 1.1557 - \frac{7.021 \times 10^{-4} T^2}{1108 + T}. \tag{11.17}$$

Dark current FPN is expressed as

$$\sigma_{D\_FPN} = D D_N, \tag{11.18}$$

where D_N is the dark current FPN quality factor. This parameter typically varies between 10% and 40% for CCD and CMOS imagers. Note that "dark" FPN (D_N) is much greater than "light" FPN (P_N) by approximately 10–40 times.

Example 11.3

Find the average dark current rate, and related shot noise and FPN, given the following parameters:

$t_I = 0.08$ sec

$D_{FM} = 0.5$ nA/cm^2

$D_N = 0.3$

$T = 0$ C (273 K)

$P_A = (8 \times 10^{-4})^2$ cm^2

Solution:
From Eq. (11.17), the bandgap energy is

$$E_g = 1.1557 - \frac{(7.021 \times 10^{-4}) \times 273^2}{1108 + 273} = 1.120278 \text{ eV}.$$

From Eq. (11.16), the average dark current rate is

$$D_R = (2.55 \times 10^{15}) \times (8 \times 10^{-4})^2 \times 0.5 \times 273^{1.5} \times \exp\left[-\frac{1.120278}{2 \times (8.62 \times 10^{-5}) \times 273}\right];$$

$$D_{\mathrm{R}} = 178.3 \text{ e}^{-}/\text{sec}.$$

From Eq. (11.15), the dark current signal is

$$D = t_{\mathrm{I}} D_{\mathrm{R}} = 0.08 \times 178 = 14.2 \text{ e}^{-}.$$

From Eq. (11.14), the dark shot noise is

$$\sigma_{\mathrm{D\_SHOT}} = (14.2)^{1/2} = 3.77 \text{ e}^{-} \text{ rms}.$$

From Eq. (11.18), the dark FPN is

$$\sigma_{\mathrm{D\_FPN}} = 14.2 \times 0.3 = 4.26 \text{ e}^{-} \text{ rms}.$$

Example 11.4

Generate a PTC where the read noise is composed of dark and source follower noise. Assume the following:

$$K_{\mathrm{ADC}}(\text{e}^{-}/\text{DN}) = 1.5$$
$$\sigma_{\mathrm{SF}}(\text{DN}) = 3.33$$
$$D_{\mathrm{FM}} = 0.5 \text{ nA/cm}^2$$
$$D_{\mathrm{N}} = 0.3$$
$$P_{\mathrm{A}} = (8 \times 10^{-4})^2 \text{ cm}^2$$
$$t_{\mathrm{I}} = .08 \text{ sec}$$
$$T = 50,\ 40,\ 30,\ 20,\ 10,\ 0,\ -10,\ -20 \text{ C}$$

Make separate plots, with and without dark current FPN.

Solution:
The read noise and signal shot noise together are

$$\sigma_{\mathrm{READ+SHOT}} = [\sigma_{\mathrm{SF}}^2 + D + (DD_{\mathrm{N}})^2 + \sigma_{\mathrm{SHOT}}^2]^{1/2}. \tag{E11.1}$$

The read noise and signal shot noise without dark FPN is

$$\sigma_{\mathrm{READ+SHOT}} = (\sigma_{\mathrm{SF}}^2 + D + \sigma_{\mathrm{SHOT}}^2)^{1/2}. \tag{E11.2}$$

Equations (E11.1) and (E11.2) are plotted in Figs. 11.3 and 11.4, respectively. Note that the operating temperature must be less than -10 deg C for the dark current noise to be negligible compared to source follower noise. In comparing figures, it can be seen that dark FPN completely dominates dark shot noise.

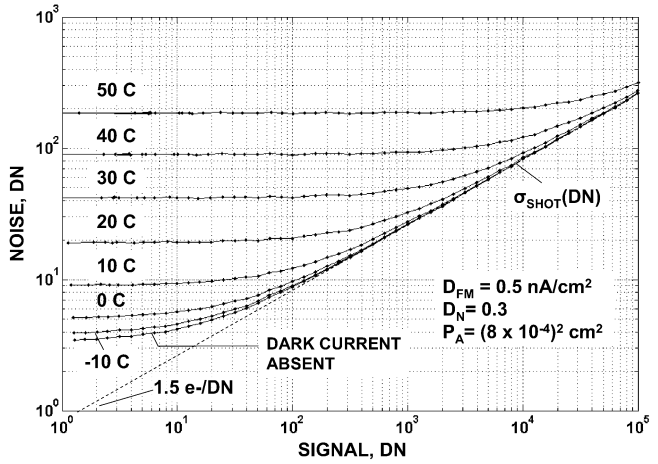

Figure 11.3 PTC responses with thermal dark current FPN at different operating temperatures.

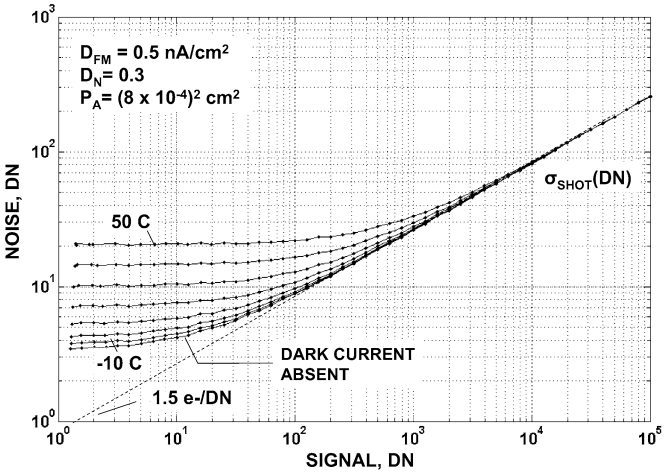

Figure 11.4 PTC responses with thermal dark current FPN removed.

Dark current parameters D_{N} and D_{FM} are found by plotting dark current shot noise and FPN as a function of dark current signal. A PTC generated like this, without a light source, is referred to as a "dark transfer curve" (DTC). Dark signal is varied by changing either the integration time or the operating temperature. The parameters $K_{\mathrm{ADC}}(\mathrm{e}^{-}/\mathrm{DN})$, D, D_{R}, D_{FM}, and D_{N} all can be determined from a DTC. Working equations to find these parameters are

$$K_{\mathrm{ADC}}(\mathrm{e}^{-}/\mathrm{DN}) = \frac{D(\mathrm{DN})}{\sigma_{\mathrm{D\_SHOT}}(\mathrm{DN})^2}, \tag{11.19}$$

where $D(\mathrm{DN})$ is the average dark current signal given by

$$D(\mathrm{DN}) = \frac{D}{K_{\mathrm{ADC}}(\mathrm{e}^{-}/\mathrm{DN})}. \tag{11.20}$$

The dark current figure of merit is found by substituting Eq. (11.16) into Eq. (11.15) and solving for D_{FM}, which yields

$$D_{\mathrm{FM}} = \frac{D_{\mathrm{R}}}{2.55 \times 10^{15} P_{\mathrm{A}} T^{1.5} e^{-E_{\mathrm{g}}/(2kT)}}. \tag{11.21}$$

The dark current FPN quality factor is defined by

$$D_{\mathrm{N}} = \frac{\sigma_{\mathrm{D\_FPN}}(\mathrm{DN})}{D(\mathrm{DN})}. \tag{11.22}$$

Note that the dark current signal level, where the dark shot noise and dark FPN are equal, is

$$D_{\mathrm{SHOT=FPN}} = \frac{1}{D_{\mathrm{N}}^2}. \tag{11.23}$$

Example 11.5

Figure 11.5 shows DTCs with and without dark current FPN based on these parameters:

$$K_{\mathrm{ADC}}(\mathrm{e}^{-}/\mathrm{DN}) = 1.5$$
$$\sigma_{\mathrm{SF}}(\mathrm{DN}) = 3.33$$

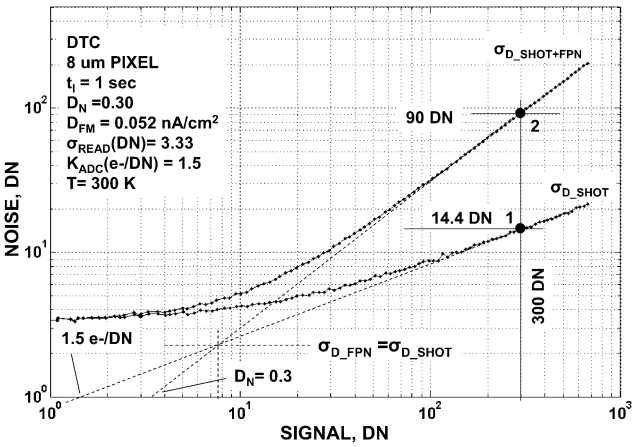

Figure 11.5 Dark transfer curve generated without light.

$$D_{\mathrm{FM}} = \text{nA/cm}^2$$
$$D_{\mathrm{N}} = 0.3$$
$$P_{\mathrm{A}} = (8 \times 10^{-4})^2 \text{ cm}^2$$
$$t_{\mathrm{I}} = 1 \text{ sec}$$
$$T = 300 \text{ K}$$

From the DTC curve presented, confirm $K_{\mathrm{ADC}}(\mathrm{e}^-/\mathrm{DN})$, D, D_{R}, D_{FM}, and D_{N}. Find the dark signal level where dark FPN begins to dominate dark shot noise.

Solution:
From Eq. (11.19) and data point 1 on the dark shot noise curve,

$$K_{\mathrm{ADC}}(\mathrm{e}^-/\mathrm{DN}) = \frac{300}{14.4^2} = 1.5.$$

From Eq. (11.20), the signal level at data point 1 is

$$D = 300 \times 1.5 = 450 \text{ e}^-.$$

From Eq. (11.15), the dark current rate is

$$D_{\mathrm{R}} = \frac{450}{1} = 450 \text{ e}^-/\text{sec}.$$

From Eq. (11.17), the silicon bandgap at 300 K is

$$E_{\mathrm{g}} = 1.1157 - \frac{7.021 \times 10^{-4} \times 300^2}{1108 + 300} = 1.071.$$

From Eq. (11.21), the dark current figure of merit is

$$\begin{aligned} D_{\mathrm{FM}} &= \frac{450}{\left\{(2.55 \times 10^{15}) \times (8 \times 10^{-4})^2 \times 300^{1.5} \exp\left[-\dfrac{1.071}{2 \times (8.62 \times 10^{-5}) \times 300}\right]\right\}} \\ &= 0.052 \text{ nA/cm}^2. \end{aligned}$$

From Eq. (11.22) and data point 2 on the FPN curve,

$$D_{\mathrm{N}} = \frac{90}{300} = 0.3.$$

From Eq. (11.23), the dark signal level where dark FPN starts to dominate dark shot noise is

$$D_{\mathrm{SHOT=FPN}} = \frac{1}{(0.3)^2} = 11 \text{ e}^-.$$

Figure 11.6 shows the buildup of dark current for 150 CMOS pixels as a function of time. The data are used to generate the DTCs presented in Fig. 11.7 with and without dark FPN. Note from Fig. 11.6 that dark current increases nonlinearly with time, indicating that D_{FM} is not a constant. Also note from Fig. 11.7 that the dark FPN slope 1 curve shifts toward the right, which signifies that D_{N} is decreasing with the signal level. Figure 11.8 plots dark current nonlinearity using the relation

$$\mathrm{NL_D} = 1 - \frac{D(\mathrm{DN})_{\mathrm{m}}/t_{\mathrm{m}}}{D(\mathrm{DN})/t_{\mathrm{I}}}, \tag{11.24}$$

where $\mathrm{NL_D}$ is the dark current nonlinearity, and $D(\mathrm{DN})_{\mathrm{m}}$ is the dark signal at some arbitrary time t_{m} (shown in Fig. 11.8 at 2.6 sec).

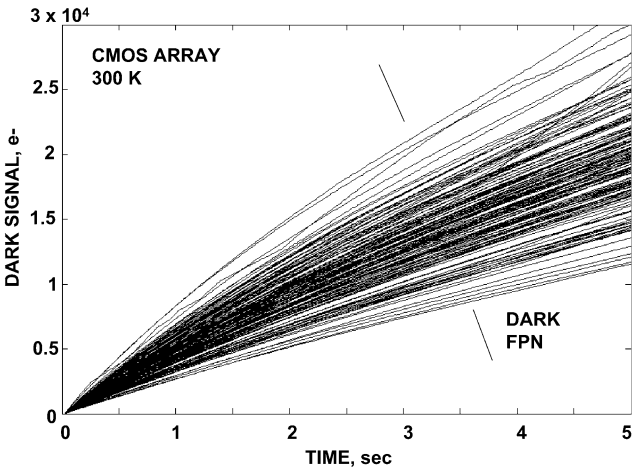

Figure 11.6 Nonlinear dark current build-up for 256 CMOS pixels showing dark FPN.

Example 11.6

For Fig. 11.7, determine the variation of dark FPN over the signal range measured.

Solution:
From Eq. (11.22) and the two data points [at $D(\mathrm{DN}) = 1000$)] shown in Fig. 11.7,

$$D_{\mathrm{N}} = \frac{300}{1000} = 0.3\ (30\%),$$

and

$$D_{\mathrm{N}} = \frac{200}{1000} = 0.2\ (20\%).$$

Nonlinearity characteristics shown in Figs. 11.6 to 11.8 are common to specific types of CMOS and CCD imagers, where dark current is influenced by electric

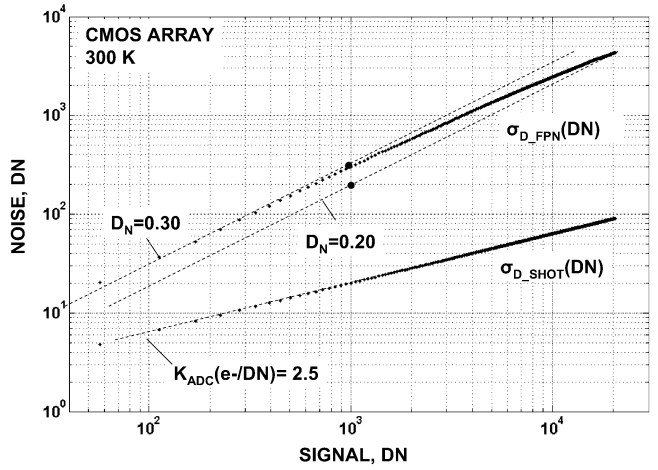

Figure 11.7 Dark transfer curves measuring dark current FPN nonlinearity with signal.

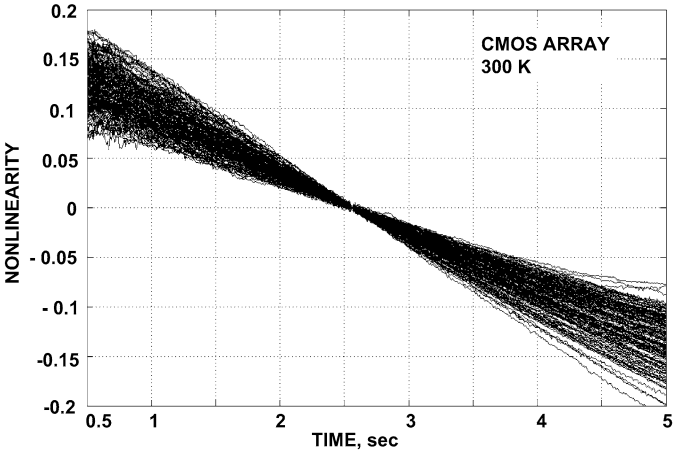

Figure 11.8 Dark current nonlinearity versus time for Fig. 11.6.

fields internal to a pixel. The fields decrease as signal charge collects, which in turn reduces the dark current rate. Dark current analysis is complex for these sensors, so DTC helps identify and quantify the problems like this. Fortunately, the majority of imagers (especially CCDs) behave according to the dark current relations given above.

PTC and DTC can be generated together on a single graph. For example, Fig. 11.9 shows a PTC/DTC combination plot. The DTC is generated by changing the integration time, yielding information for $K_{\mathrm{ADC}}(\mathrm{e}^{-}/\mathrm{DN})$, D_{N}, and D_{FM} para-

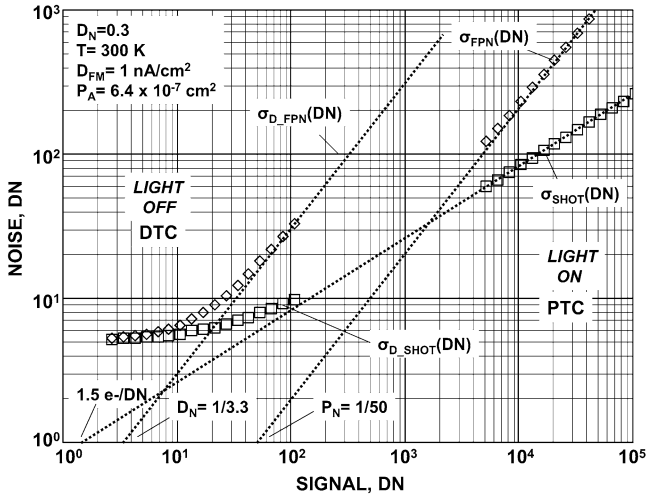

Figure 11.9 DTC and PTC responses generated on the same plot.

meters. For high signals, the integration time is fixed and the light level is varied to generate PTCs. The plot provides information for $K_{\mathrm{ADC}}(\mathrm{e}^{-}/\mathrm{DN})$ and P_{N}. Note that the dark and light shot noise curves merge on the slope $1/2$ line, whereas the two slope 1 curves are different and produce D_{N} and P_{N}.

11.5 ADC Quantizing Noise

11.5.1 Linear encoding

Figure 11.10 shows transfer characteristics for a linear ADC. As indicated, when a pixel signal is digitized it introduces an uncertainty, which can add to the read noise floor. The rms error about the perfect ramp response shown is called "ADC quantizing noise." For an ideal ADC, this noise amounts to

$$\sigma_{\mathrm{ADC}}(\mathrm{DN}) = \left(\frac{1}{12}\right)^{1/2} = 0.2887. \tag{11.25}$$

In terms of rms noise electrons,

$$\sigma_{\mathrm{ADC}} = 0.2887 K_{\mathrm{ADC}}(\mathrm{e}^{-}/\mathrm{DN}). \tag{11.26}$$

Equation (11.26) shows that quantizing noise is dependent on the ADC sensitivity, $K_{\mathrm{ADC}}(\mathrm{e}^{-}/\mathrm{DN})$. This connection is demonstrated in Fig. 11.11, which presents three 2 e^{-} read noise images at different sensitivities (2, 10, and 100 e^{-}/DN). As $K_{\mathrm{ADC}}(\mathrm{e}^{-}/\mathrm{DN})$ increases, the quantizing noise becomes apparent until it dominates the read noise floor. Figure 11.12 presents "stacked" column traces through each image shown in Fig. 11.11. The quantizing noise "steps" become more apparent as

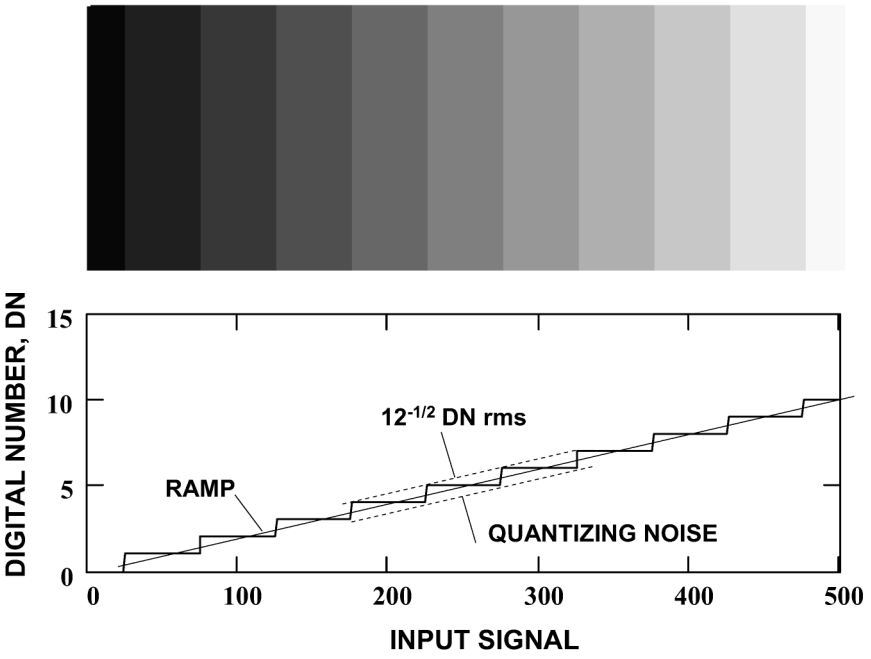

Figure 11.10 ADC quantizing noise image and transfer curve.

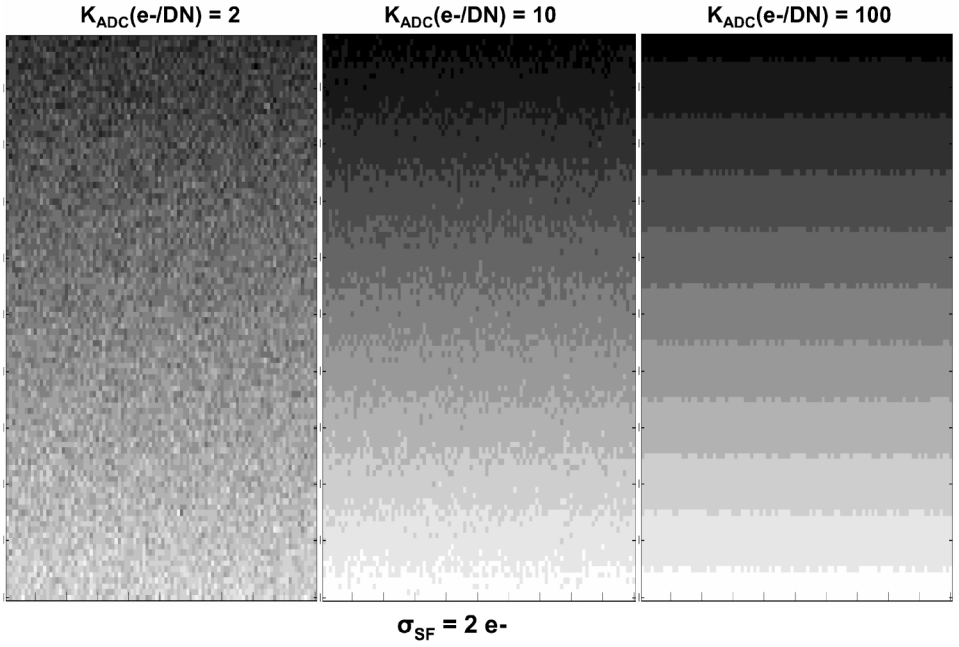

Figure 11.11 ADC quantizing noise images being hidden by random source follower noise by different K_{ADC}(e^{-}/DN).

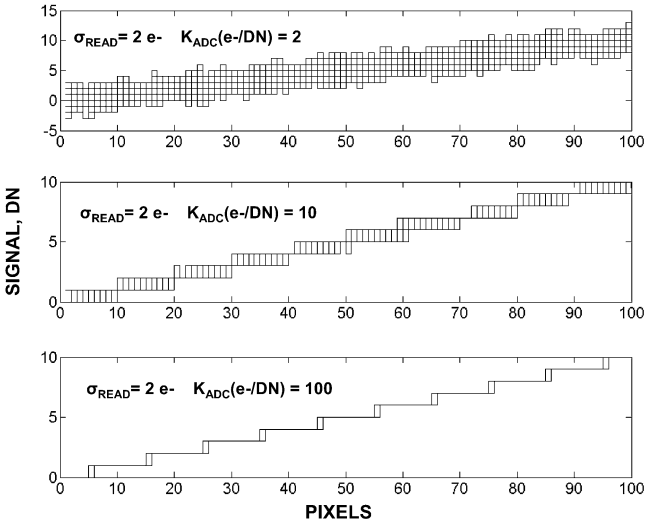

Figure 11.12 Video column traces of Fig. 11.10.

the ADC sensitivity increases. Note that quantizing noise becomes completely hidden when $K_{\mathrm{ADC}}(\mathrm{e}^-/\mathrm{DN})$ is approximately equal to the random noise level. Therefore, for proper noise encoding, we simply let

$$K_{\mathrm{ADC}}(\mathrm{e}^-/\mathrm{DN}) = \sigma_{\mathrm{READ}}. \tag{11.27}$$

This relation forces read noise to 1 DN rms, without quantizing noise issues.

Figure 11.13 shows similar images where signal shot noise is introduced along with the 2 e^- read noise floor. Comparing Figs. 11.11 and 11.13 shows that shot noise further hides the quantizing noise, which allows for a higher $K_{\mathrm{ADC}}(\mathrm{e}^-/\mathrm{DN})$. In fact, the ADC sensitivity required for a camera system depends on the lowest noise expected to be digitized, i.e.,

$$K_{\mathrm{ADC}}(\mathrm{e}^-/\mathrm{DN}) = \sigma_{\mathrm{LOW}}, \tag{11.28}$$

where σ_{LOW} is the lowest noise level encountered by a camera system (which includes FPN sources).

Example 11.7

Determine the read and shot noise for each DN step shown in Fig. 11.13 without ADC quantizing noise. Assume $\sigma_{\mathrm{SF}} = 2\,\mathrm{e}^-$.

Solution:
The random noise for each DN level is composed of source follower and shot noise, i.e.,

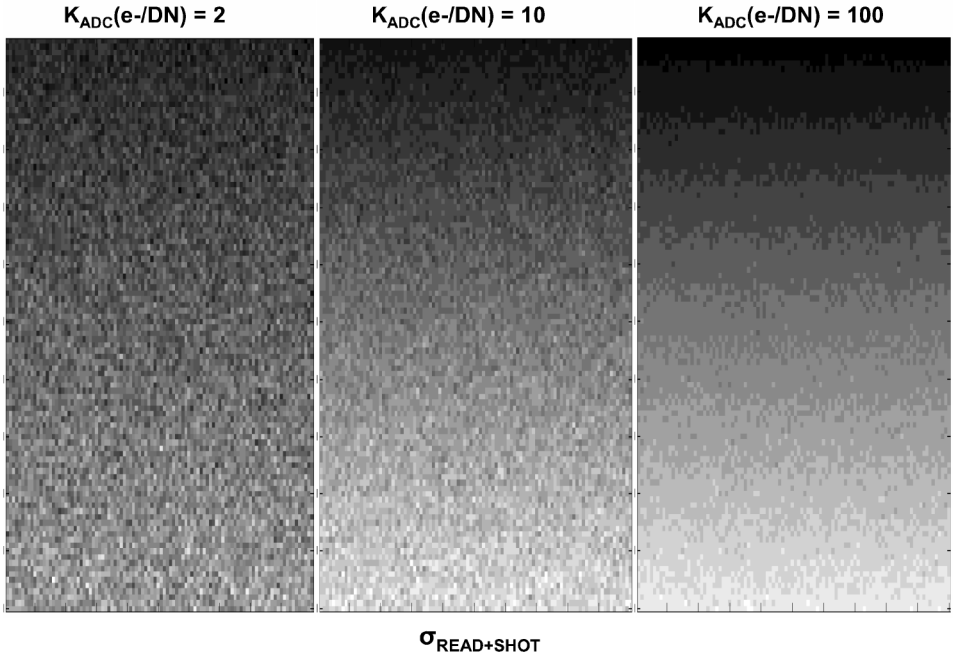

Figure 11.13 ADC quantizing noise images being hidden by random source follower and shot noise with different $K_{\mathrm{ADC}}(\mathrm{e}^{-}/\mathrm{DN})$.

$$\sigma_{\mathrm{READ+SHOT}}(\mathrm{DN}) = \left\{ [\sigma_{\mathrm{READ}}(\mathrm{DN})]^2 + \frac{S(\mathrm{DN})}{K_{\mathrm{ADC}}(\mathrm{e}^{-}/\mathrm{DN})} \right\}^{1/2}. \qquad \text{(E11.3)}$$

Table 11.2 tabulates the noise level as calculated by Eq. (E11.3).

Table 11.2 and Fig. 11.13 can be compared. The noise levels tabulated should be greater than $\sigma_{\mathrm{ADC}}(\mathrm{DN})$ if proper encoding is to take place [i.e., greater than 0.2887 DN, as defined by Eq. (11.25)]. This is not the condition for the third column. The second column is marginal, whereas the first column is satisfactory.

Besides encoding read noise properly, it is also important to encode the maximum signal level expected, which is typically the charge capacity of the sensor. The full-well encoding required is determined by

$$N_{\mathrm{ADC}} = \frac{S_{\mathrm{FW}}}{K_{\mathrm{ADC}}(\mathrm{e}^{-}/\mathrm{DN})}, \qquad (11.29)$$

where N_{ADC} is the number of DN levels required from the ADC. Substituting Eq. (11.27), which is the requirement to encode read noise properly into Eq. (11.29), yields

$$N_{\mathrm{ADC}} = \frac{S_{\mathrm{FW}}}{\sigma_{\mathrm{READ}}}, \qquad (11.30)$$

Table 11.2 Read and shot noise levels for Fig. 11.13.

DN Level	$\sigma_{\mathrm{READ+SHOT}}(\mathrm{DN})$ $K_{\mathrm{ADC}}(\mathrm{e^-/DN}) = 2\ \mathrm{e^-/DN}$ $\sigma_{\mathrm{READ}}(\mathrm{DN}) = 1\ \mathrm{DN}$	$\sigma_{\mathrm{READ+SHOT}}(\mathrm{DN})$ $K_{\mathrm{ADC}}(\mathrm{e^-/DN}) = 10\ \mathrm{e^-/DN}$ $\sigma_{\mathrm{READ}}(\mathrm{DN}) = 0.2\ \mathrm{DN}$	$\sigma_{\mathrm{READ+SHOT}}(\mathrm{DN})$ $K_{\mathrm{ADC}}(\mathrm{e^-/DN}) = 100\ \mathrm{e^-/DN}$ $\sigma_{\mathrm{READ}}(\mathrm{DN}) = 0.02\ \mathrm{DN}$
0	1	0.2000	0.0200
1	1.2247	0.3742	0.1020
2	1.4142	0.4899	0.1428
3	1.5811	0.5831	0.1744
4	1.7321	0.6633	0.2010
5	1.8708	0.7348	0.2245
6	2	0.8000	0.2458
7	2.1213	0.8602	0.2653
8	2.2361	0.9165	0.2835
9	2.3452	0.9695	0.3007
10	2.4495	1.0198	0.3169

which is simply the dynamic range for a camera system (a good rule of thumb to remember).

The number of bits required from an ADC is

$$N_{\mathrm{BITS}} = \frac{\log(N_{\mathrm{ADC}})}{\log(2)}. \tag{11.31}$$

Example 11.8

Plot the number of ADC bits required as a function of the lowest noise level to be encoded for different full-well levels (10^4, 5×10^4, 10^5, 5×10^5, and 10^6 e^-).

Solution:
From Eqs. (11.28) and (11.30), the number of DN levels required is

$$N_{\mathrm{ADC}} = \frac{S_{\mathrm{FW}}}{\sigma_{\mathrm{LOW}}}. \tag{E11.4}$$

Figure 11.14 plots Eq. (E11.4). For example, 16 bits is required to encode an 8 e^- noise level and a 5×10^5 full-well signal.

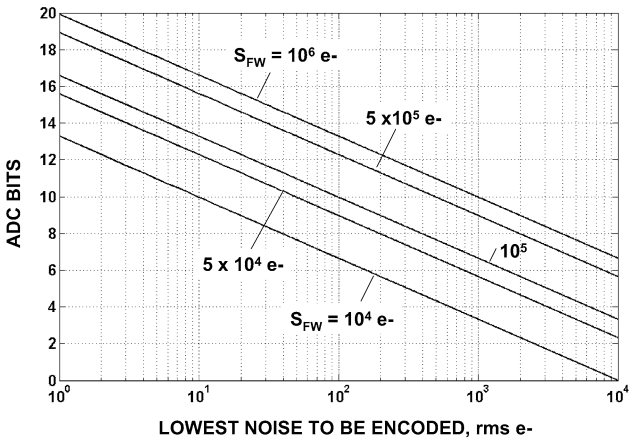

Figure 11.14 Number of ADC bits required to encode specific noise and full-well levels.

Example 11.9

Assume a camera system will be taking pictures that are always FPN limited. Determine the number of ADC bits required, given that the full well is 10^5 e^- and $P_{\mathrm{N}} = 0.01$.

Solution:
From Eqs. (11.28) and (11.30), the onset of FPN is

$$\frac{1}{P_{\mathrm{N}}^2} = \frac{1}{(0.01)^2} = 10{,}000\ \mathrm{e}^-.$$

Therefore, the lowest FPN to be encoded is

$$\sigma_{\mathrm{FPN}} = 0.01 \times 10{,}000 = 100\ \mathrm{e}^-.$$

From Fig. 11.14, the number of bits required is

$$N_{\mathrm{BITS}} = 10.$$

Figure 11.15 shows $\sigma_{\mathrm{READ+SHOT}}(\mathrm{DN})$ PTC responses, with and without ADC quantizing noise, at different read noise levels (100 e^-, 60 e^-, and 2 e^-). The plots assume a fixed ADC sensitivity of $K_{\mathrm{ADC}}(\mathrm{e}^-/\mathrm{DN}) = 100$ and an 8-bit ADC. When $\sigma_{\mathrm{READ}} < K_{\mathrm{ADC}}(\mathrm{e}^-/\mathrm{DN})$, quantizing error becomes appreciable. Note that quantizing noise is cyclic with a signal period of 1 DN for the 2 e^- noise case. The cyclic signature is quenched when the noise level is above 0.5 DN. The dotted line shown assumes a fixed quantizing noise of 0.2887 DN [i.e., Eq. (11.25)], which is only valid when the cyclic pattern is not present. Figure 11.16 presents noise variance PTCs using the same data set as Fig. 11.15, with and without quantizing noise. $K_{\mathrm{ADC}}(\mathrm{e}^-/\mathrm{DN})^{-1}$ is equal to the slope of all curves (i.e., $1/100$).

Figure 11.17 shows PTC data taken from a CMOS sensor that incorporates an on-chip 10-bit ADC. The ADC exhibits a bit weighting problem: the noise

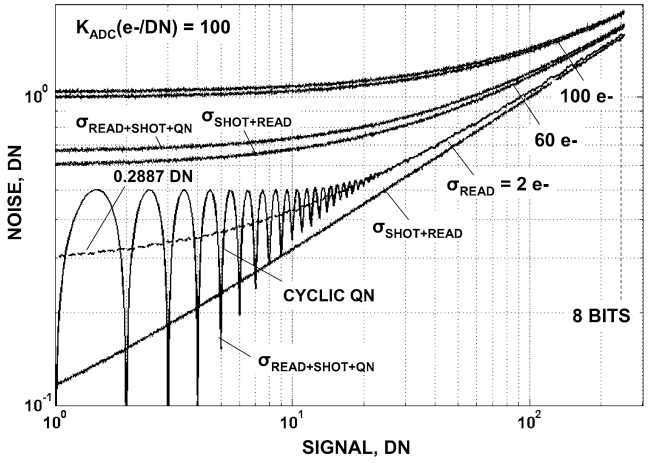

Figure 11.15 PTC responses showing how ADC quantizing noise becomes increasingly dominant as random read noise decreases.

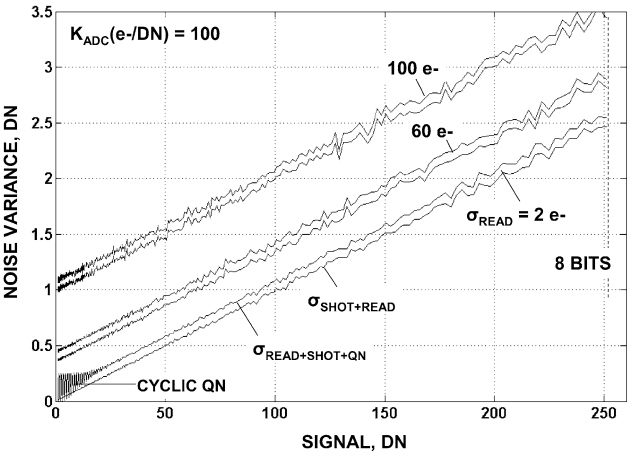

Figure 11.16 Corresponding variance PTCs for Fig. 11.15.

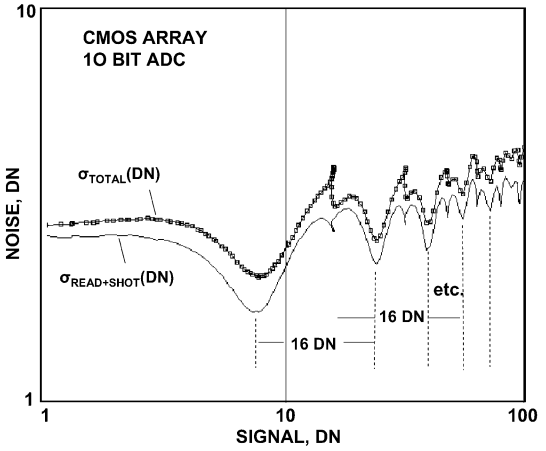

Figure 11.17 PTC responses demonstrating an ADC bit weighting problem.

varies cyclically every 16 bits in the signal. The source of the difficulty is seen in Fig. 11.18, where output DN is plotted against input signal. The staircase is interrupted every 16 bits, which reflects each "kink" in the PTC. Assuming additional ADC bits are available for full-well encoding, one can hide quantizing problems like this by increasing the voltage gain before the ADC, but this is not desirable.

11.5.2 Nonlinear encoding

All PTCs presented previously show that linear encoding excessively encodes shot noise and FPN. For example, a read noise of 10 e^- is equivalent to 1 DN, assuming $K_{\mathrm{ADC}}(\mathrm{e}^-/\mathrm{DN}) = \sigma_{\mathrm{READ}}$. However, a shot noise of 1000 e^- is encoded to

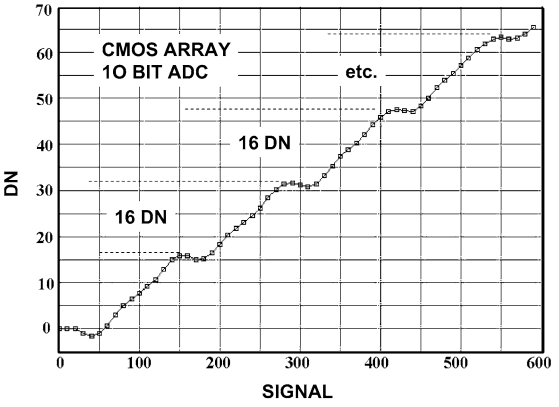

Figure 11.18 ADC transfer function showing the bit weighting problem characterized in Fig. 11.17.

100 DN, which is a hundred times greater encoding power than is necessary. For optimum shot noise digitization, $K_{\mathrm{ADC}}(\mathrm{e}^{-}/\mathrm{DN})$ should increase by the square root of the signal (i.e., $S^{1/2}$). Changing the ADC sensitivity in this manner will encode the shot noise to a fixed 1 DN level over the sensor's dynamic range. This encoding processor is called a "square-rooter"—a powerful compression technique applied to shot-noise-limited detectors.[1]

Figure 11.19 shows three PTCs that demonstrate the encoding compression technique. The first labeled curve, $K_{\mathrm{ADC}}(\mathrm{e}^{-}/\mathrm{DN}) = 2$, produces the standard, linearly encoded total noise PTC. FPN is encoded to 500 DN at full well [$S_{\mathrm{FW}}(\mathrm{DN}) = 50{,}000$]. The second plot assumes that $K_{\mathrm{ADC}}(\mathrm{e}^{-}/\mathrm{DN}) = S^{1/2}$, which optimally

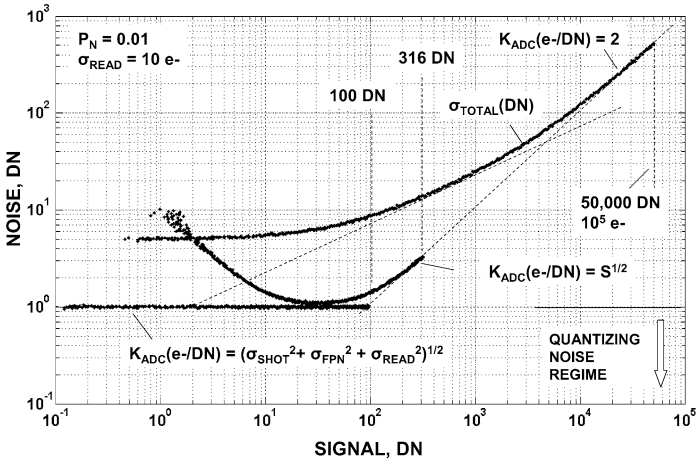

Figure 11.19 Square-rooter PTC responses showing optimum encoding for different $K_{\mathrm{ADC}}(\mathrm{e}^{-}/\mathrm{DN})$.

encodes shot noise to 1 DN. However, this sensitivity setting still over-encodes the read noise and FPN, which is seen in Fig. 11.19 when the curve deviates from the 1 DN noise level. In order to compress all three noise sources optimally to 1 DN, we let the ADC sensitivity vary as

$$K_{\mathrm{ADC}}(\mathrm{e^-/DN}) = \left[\sigma_{\mathrm{READ}}^2 + \eta_{\mathrm{i}} S + (P_{\mathrm{N}} S)^2\right]^{1/2}. \tag{11.32}$$

A PTC that assumes Eq. (11.32) is also shown in Fig. 11.19 as a flat-line response of 1 DN. Note that only 100 DN is required to cover the detector's dynamic range compared to 50,000 DN for linear encoding. This represents a compression ratio of 500 without information loss.

Substituting Eq. (11.32) into Eq. (11.29) determines the number of DN levels required for optimum nonlinear encoding:

$$N_{\mathrm{ADC}} = \frac{S_{\mathrm{FW}}}{[\sigma_{\mathrm{READ}}^2 + \eta_{\mathrm{i}} S + (P_{\mathrm{N}} S)^2]^{1/2}}. \tag{11.33}$$

If FPN dominates read and shot noise at full well, Eq. (11.33) simply reduces to

$$N_{\mathrm{ADC}} = \frac{1}{P_{\mathrm{N}}}. \tag{11.34}$$

Example 11.10

For Fig. 11.19, determine the number of DN levels and ADC bits required, given the following ADC sensitivities:

$$K_{\mathrm{ADC}}(\mathrm{e^-/DN}) = 2$$
$$K_{\mathrm{ADC}}(\mathrm{e^-/DN}) = \mathrm{S}^{1/2}$$
$$K_{\mathrm{ADC}}(\mathrm{e^-/DN}) = \left[\sigma_{\mathrm{READ}}^2 + S + (P_{\mathrm{N}} S)^2\right]^{1/2}$$

Assume a full well of $S_{\mathrm{FW}} = 10^5$ e$^-$, $\sigma_{\mathrm{READ}} = 10$ e$^-$, and $P_{\mathrm{N}} = 0.01$.

Solution:

1. $K_{\mathrm{ADC}}(\mathrm{e^-/DN}) = 2$
   From Eqs. (11.29) and (11.31):

$$N_{\mathrm{ADC}} = \frac{10^5}{2} = 50{,}000 \text{ DN}$$
$$N_{\mathrm{BITS}} = \frac{\log(50{,}000)}{\log 2} = 15.6 \text{ (or 16 bits)}$$

2. $K_{\mathrm{ADC}}(\mathrm{e}^{-}/\mathrm{DN}) = S^{1/2}$
   From Eqs. (11.29) and (11.31):

$$N_{\mathrm{ADC}} = \frac{10^5}{(10^5)^{1/2}} = 316 \text{ DN}$$

$$N_{\mathrm{BITS}} = \frac{\log(316)}{\log 2} = 8.3 \text{ (or 9 bits)}$$

3. $K_{\mathrm{ADC}}(\mathrm{e}^{-}/\mathrm{DN}) = [\sigma^2_{\mathrm{READ}} + S + (P_{\mathrm{N}}S)^2]^{1/2}$
   From Eqs. (11.34) and (11.31):

$$N_{\mathrm{ADC}} = \frac{1}{0.01} = 100 \text{ DN}$$

$$N_{\mathrm{BITS}} = \frac{\log(100)}{\log 2} = 6.6 \text{ (or 7 bits)}$$

These results are shown in Fig. 11.19.

Figure 11.20 shows two PTCs that assume $K_{\mathrm{ADC}}(\mathrm{e}^{-}/\mathrm{DN}) = S^{1/2}$ and $K_{\mathrm{ADC}}(\mathrm{e}^{-}/\mathrm{DN}) = 4 \times S^{1/2}$. The latter curve produces noise levels less than 1 DN, taking the sensor into the quantizing noise regime. Although further compression does take place (from 320 DN to 80 DN), the cyclic quantizing noise pattern also emerges. As long as the noise level is >1 DN, quantizing noise is controlled, which is the case when $K_{\mathrm{ADC}}(\mathrm{e}^{-}/\mathrm{DN}) = S^{1/2}$.

Figure 11.21 presents images showing full 10-bit encoding with the signal compressed to 6, 5, and 4 bits. Note that the 4-bit image has insufficient encoding and

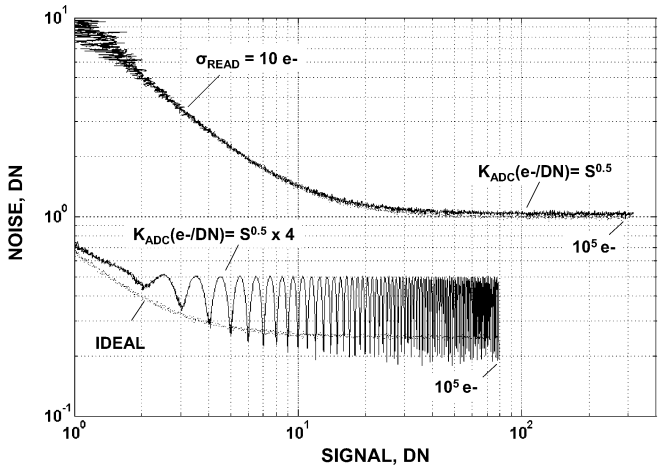

Figure 11.20 Square-rooter PTC responses showing ADC quantizing noise when the read noise level drops below 1 DN rms.

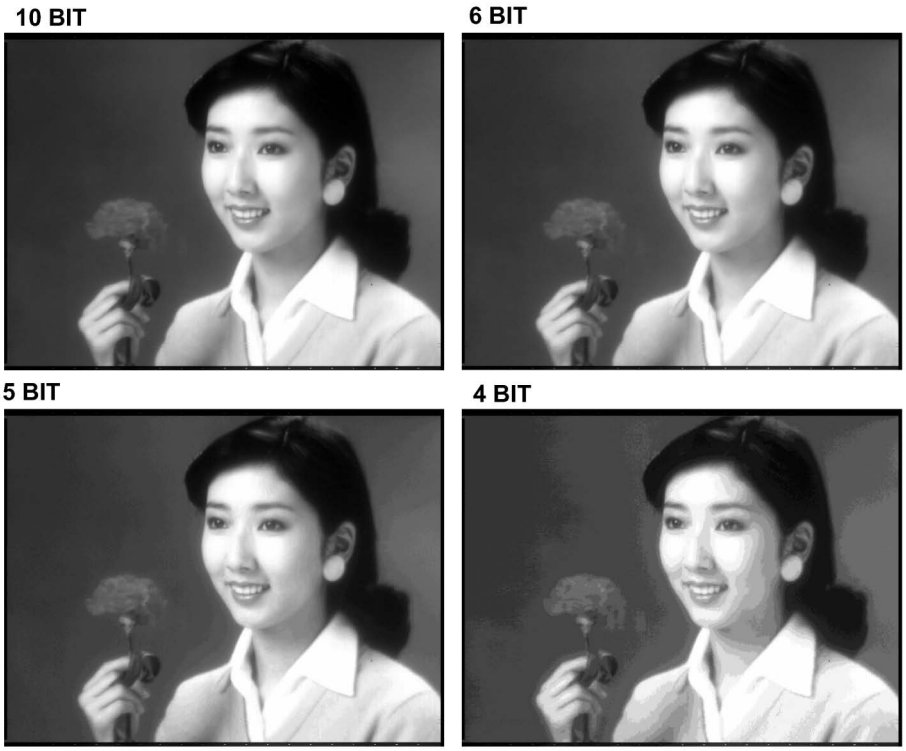

Figure 11.21 Square-rooter images showing 6-, 5- and 4-bit compressions from 10 bits.

shows ADC quantizing noise. Additional square-root discussions, including hardware implementation, are given in Ref. 1.

11.6 Offset Fixed Pattern Noise

Figures 5.9 and 5.10 demonstrated the importance of precisely knowing the offset level for accurate signal measurement. For CCD imagers, the offset level needs to be tracked for each amplifier port. For CMOS imagers, all pixels must be monitored because each pixel exhibits a different offset level. For example, Fig. 11.22 presents a single row of CMOS pixels showing 1000 e^- rms of offset FPN.

CMOS offset FPN noise is significantly greater than reset noise, which itself is greater than pixel source follower noise. For example, Fig. 11.23 compares offset, reset, and source follower noise for a CMOS imager (250 e^-, 28 e^-, and 2.5 e^- rms, respectively). Also shown for reference are three 5.9 keV, 1620 e^- x-ray events contained in the row of pixels. Figure 11.24 is a magnified view showing how much larger reset noise is to source follower noise.

For certain CMOS readout modes (rolling shutter and snap), "digital CDS" (DCDS) is employed to remove offset FPN and reset noise (e.g., Figs. 11.23 and 11.24 were processed in this manner).[8] DCDS processing first quickly reads

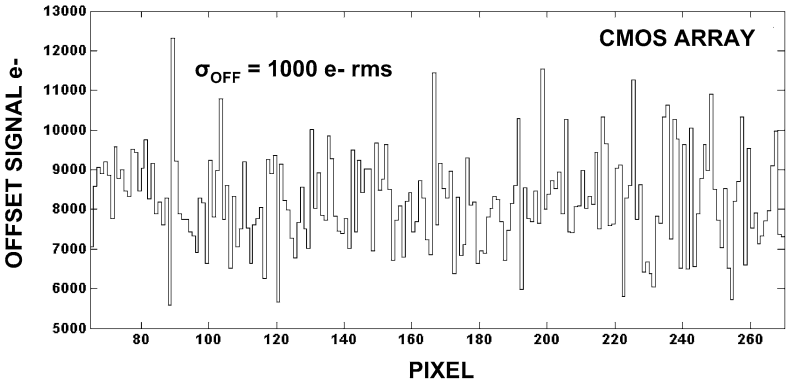

Figure 11.22 CMOS pixel offset FPN.

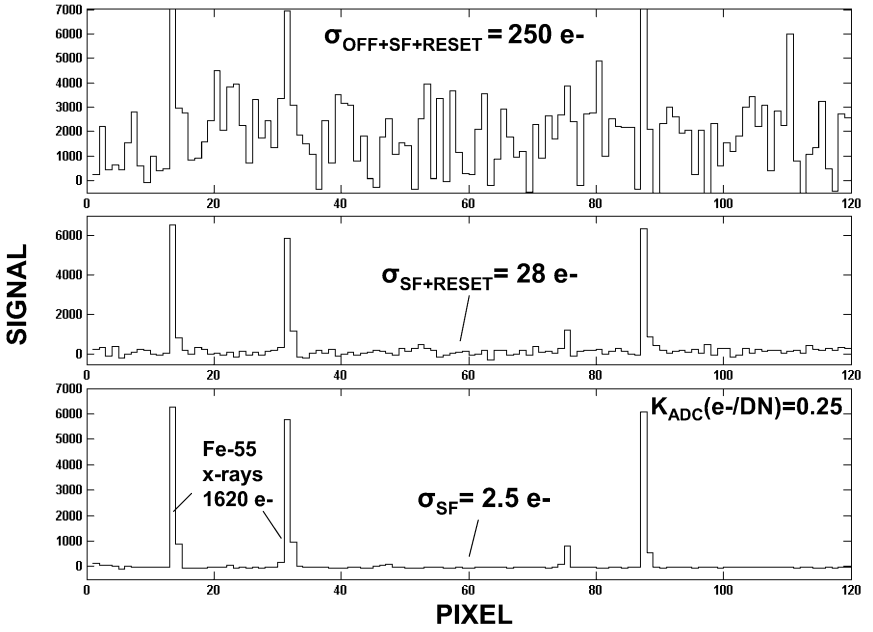

Figure 11.23 CMOS array video traces that compare offset FPN, reset and source follower noise levels.

all pixels after being globally reset. The offset/reset levels samples are stored in a computer. Then the signal charge is integrated for a specified period of time. The pixels are then read again, and their video levels are stored in the computer. Lastly, the video and offset/reset levels are differenced by the computer, thus performing DCDS. For example, Fig. 11.25 shows a video stream where four frames were taken by a 128×128 CMOS array. First, the sequence shows the offset/reset noise samples collected for the first frame. The noise level is approximately 250 e^-,

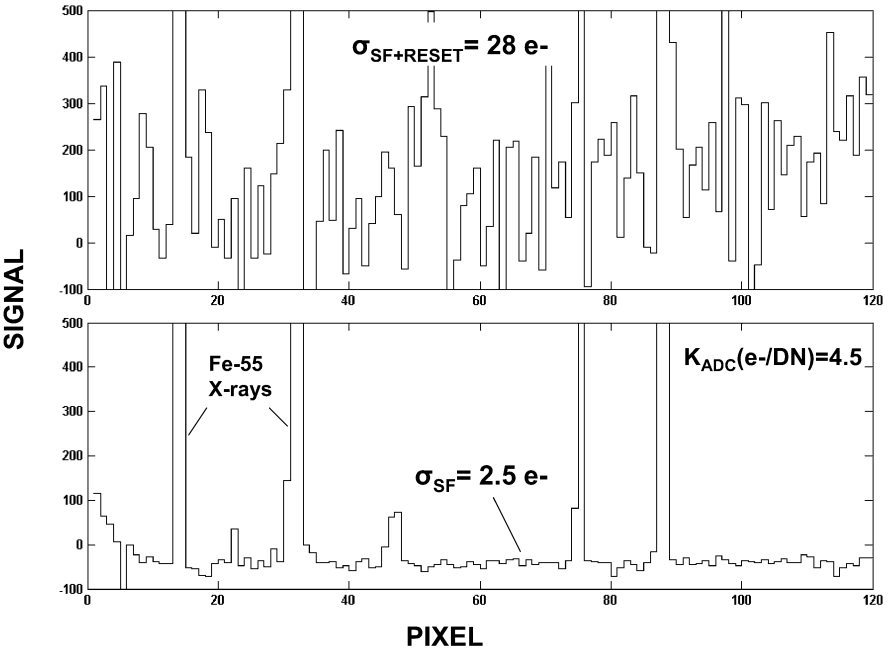

Figure 11.24 Magnified view of Fig. 11.23 showing 1620 e^- x-ray events imbedded in reset and source follower noise.

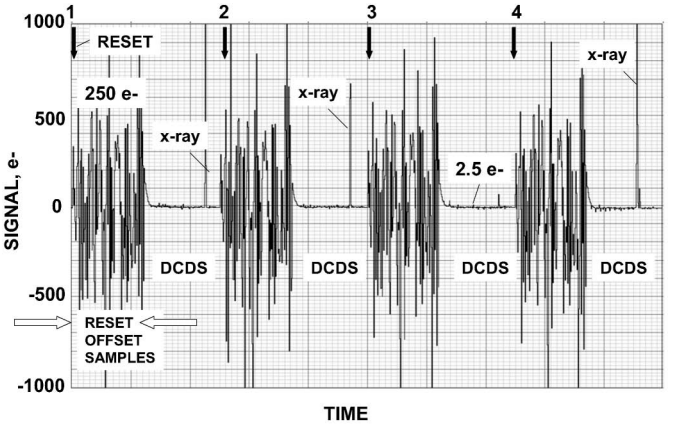

Figure 11.25 Video trace comparing noise level before and after digital CDS processing.

consisting primarily of offset FPN. After collecting offset/reset levels, the device integrates signal charge for 0.65 sec (not shown in the figure). The quiet region shown is the processed video after the two samples are subtracted by computer (i.e., DCDS). Offset and reset noise are removed entirely, reducing the read noise level to 2.5 e^-. The sequence is repeated three more times as shown. Note that

some 1620 e^- x-ray events are seen in the quiet processed regions. Figure 11.26 shows a full image of the x-ray events after DCDS is performed for the same imager and processing conditions. For comparison, Fig. 11.27 shows the raw video before DCDS processing, where offset/reset noise is present. Some x-ray events are circled but are difficult to see in the 250 e^- noise floor.

Offset FPN sources can enter downstream of the CDS processor. For example, Fig. 11.28 is a dark image taken from a single addressed CMOS pixel that shows an offset level that is systematically changing as it is read out. As the image shows, the offset variance is the same from row to row. The top of Fig. 11.29 presents a raw video trace taken before the offset pattern can be clearly seen. The second trace is derived from a 100 frame average. The offset FPN can now be seen because the averaging process reduces the random noise generated by source follower noise by a factor of 10 (the image in Fig. 11.28 is derived from this data). The first and second traces are then subtracted to remove the offset pattern. The bottom trace of Fig. 11.29 is the result after subtraction. Note that the video only contains random noise without offset FPN.

Figure 11.30 presents PTC data generated by a CMOS imager with CDS signal processing applied. As indicated, the total noise curve, $\sigma_{\mathrm{TOTAL}}(\mathrm{DN})$, exhibits some offset FPN created downstream of the CDS. This offset is removed by taking two back-to-back frames for each data point and subtracting them (pixel by pixel).

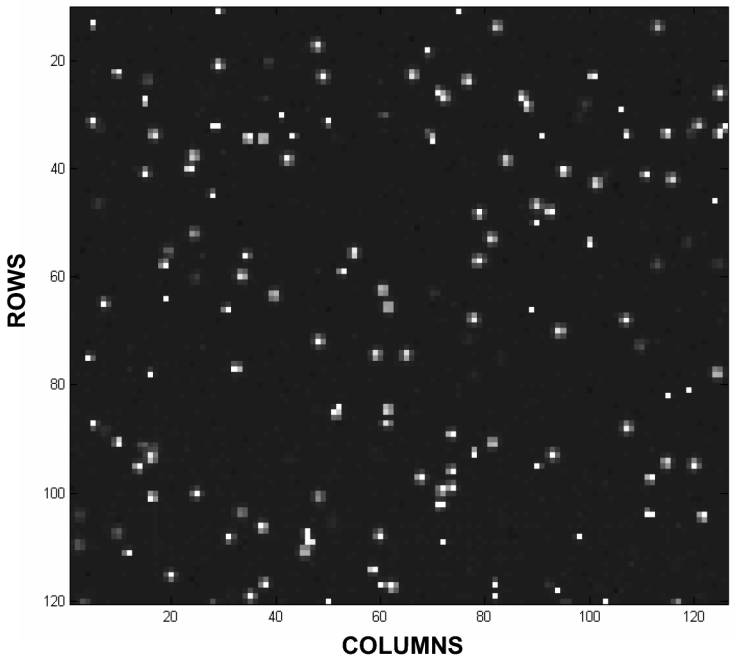

Figure 11.26 Fe-55 1620 e^- x-ray events after DCDS.

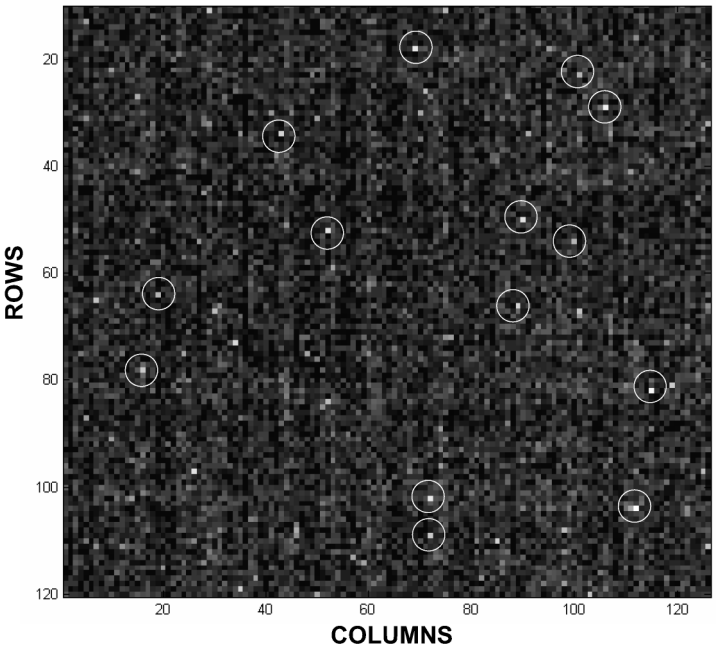

Figure 11.27 Fe-55 1620 e^- x-ray events before DCDS.

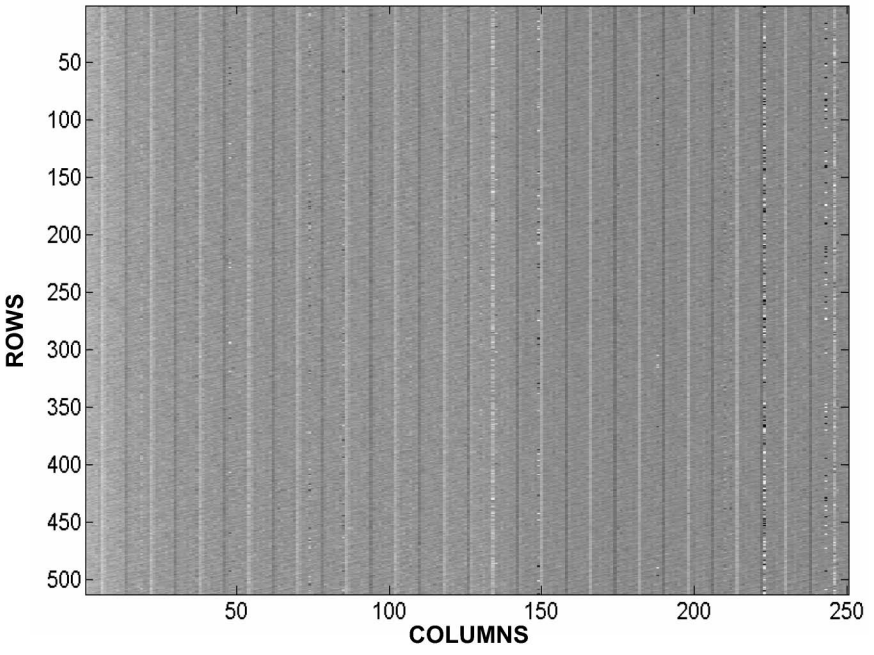

Figure 11.28 Systematic offset FPN.

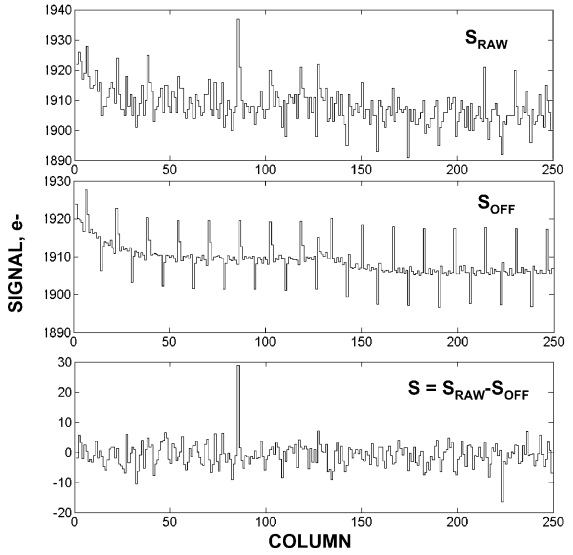

Figure 11.29 Raw signal, frame averaged offset FPN and differenced noise.

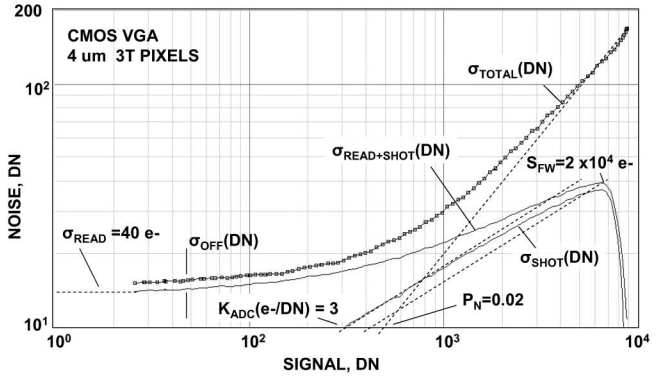

Figure 11.30 CMOS array PTC responses showing offset FPN after on-chip CDS processing and removal through frame differencing.

The process removes both offset and pixel FPN, leaving only read and shot noise. The result is plotted along with the shot noise curve.

11.7 System Noise

Dozens of system noise problems can potentially degrade the read noise floor, including preamp noise, transient noise, synchronous and nonsynchronous logic noise, settling and ringing noise, ground bounce noise, luminescence, clock phase jitter noise, ADC feedback noise, power supply noise, circuit crosstalk noise, oscillation noise, and electromagnetic noise, to name just a few. The majority of these

sources are dynamic as the noise level changes from frame to frame. For example, Fig. 11.31 shows two dark CMOS images taken at two different rates (2.25 and 5.0 Mpixels/sec). Although the system noise appears to be well behaved for the slower rate, it increases significantly when the readout frequency is doubled. The noise source is also nonsynchronous (i.e., not fixed from frame to frame), making it difficult to remove by computer. For purposes of analysis, all system noise sources are lumped together into one term called σ_{SY}. Ideally, the noise sources should not be present.

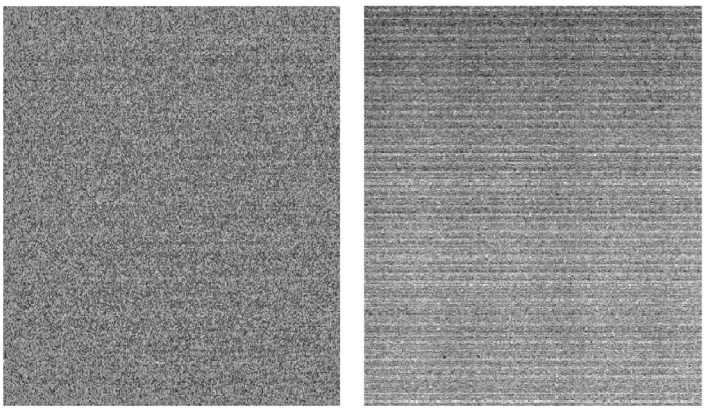

Figure 11.31 System noise compared at two pixel rates.

Important Points

1. The pixel source follower amplifier ultimately limits the read noise floor for CCD and CMOS imagers. PTC determines if the ideal noise floor has been achieved.
2. Reset and offset FPN noise are removed by CDS/DCDS signal processing.
3. A dark transfer curve (DTC) is generated without a light source to determine various dark current performance parameters, including the PT conversion constant $K_{\mathrm{ADC}}(\mathrm{e}^-/\mathrm{DN})$.
4. Thermal dark current FPN dominates dark shot noise at all signal levels.
5. ADC quantizing noise is made negligible by hiding the noise in random noise, such as pixel source follower noise. For proper noise encoding, $K_{\mathrm{ADC}}(\mathrm{e}^-/\mathrm{DN})$ is made equal to the read noise level in electron units.
6. The number of DN levels required to encode both read noise and full well optimally is equal to the sensor's dynamic range.
7. Linear ADC encoding excessively digitizes the noise source, such as shot noise and FPN. Optimal encoding is achieved when $K_{\mathrm{ADC}}(\mathrm{e}^-/\mathrm{DN})$ is made equal to the noise level in electron units.