61 STM32L412xx/422xx devices bootloader

61.1 Bootloader configuration

The STM32L412xx/422xx bootloader is activated by applying Pattern 6 (described in *Table 2: Bootloader activation patterns*). The following table shows the hardware resources used by this bootloader.

Table 131. STM32L412xx/422xx configuration in system memory boot mode

Bootloader	Feature/Peripheral	State	Comment
Common to all bootloaders	RCC	HSI enabled	The HSI is used at startup as clock source for system clock configured to 72 MHz and for USART, I2C, SPI and USB bootloader operation.
		-	The clock recovery system (CRS) is enabled for the DFU bootloader to allow USB to be clocked by HSI48 48 MHz.
	RAM	-	12 Kbyte starting from address 0x20000000 are used by the bootloader firmware
	System memory	-	28 Kbyte starting from address 0x1FFF0000, contain the bootloader firmware
	IWDG	-	The independent watchdog (IWDG) prescaler is configured to its maximum value. It is periodically refreshed to prevent watchdog reset (in case the hardware IWDG option was previously enabled by the user).
	Power	-	The DFU cannot be used to communicate with bootloader if the voltage scaling range 2 is selected. Bootloader firmware does not configure voltage scaling range value in PWR_CR1 register.
USART1 bootloader	USART1	Enabled	Once initialized the USART1 configuration is: 8-bit, even parity and 1 Stop bit
	USART1_RX pin	Input	PA10 pin: USART1 in reception mode. Used in input no pull mode.
	USART1_TX pin	Output	PA9 pin: USART1 in transmission mode. Used in input no pull mode.
USART2 bootloader	USART2	Enabled	Once initialized the USART2 configuration is: 8-bit, even parity and 1 Stop bit
	USART2_RX pin	Input	PA3 pin: USART2 in reception mode. Used in input pull-up mode.
	USART2_TX pin	Output	PA2 pin: USART2 in transmission mode. Used in input pull-up mode
USART3 bootloader	USART3	Enabled	Once initialized the USART3 configuration is: 8-bit, even parity and 1 Stop bit
	USART3_RX pin	Input	PC11 pin: USART3 in reception mode. Used in input pull-up mode.
	USART3_TX pin	Output	PC10 pin: USART3 in transmission mode. Used in input pull-up mode.

Table 131. STM32L412xx/422xx configuration in system memory boot mode (continued)

Bootloader	Feature/Peripheral	State	Comment
USARTx bootloaders	SysTick timer	Enabled	Used to automatically detect the serial baud rate from the host for USARTx bootloaders.
I2C1 bootloader	I2C1	Enabled	The I2C1 configuration is: I2C speed: up to 1 MHz, 7-bit address, slave mode, analog filter ON. Slave 7-bit address: 0b1010010x (where x = 0 for write and x = 1 for read)
	I2C1_SCL pin	Input/Output	PB6 pin: clock line is used in open-drain no pull mode.
	I2C1_SDA pin	Input/Output	PB7 pin: data line is used in open-drain no pull mode.
I2C2 bootloader	I2C2	Enabled	The I2C2 configuration is: I2C speed: up to 1 MHz, 7-bit address, slave mode, analog filter ON. Slave 7-bit address: 0b1010010x (where x = 0 for write and x = 1 for read)
	I2C2_SCL pin	Input/Output	PB10 pin: clock line is used in open-drain no pull mode.
	I2C2_SDA pin	Input/Output	PB11 pin: data line is used in open-drain no pull mode.
I2C3 bootloader	I2C3	Enabled	The I2C3 configuration is: I2C speed: up to 1 MHz, 7-bit address, slave mode, analog filter ON. Slave 7-bit address: 0b1010010x (where x = 0 for write and x = 1 for read)
	I2C3_SCL pin	Input/Output	PC0 pin: clock line is used in open-drain no pull mode.
	I2C3_SDA pin	Input/Output	PC1 pin: data line is used in open-drain no pull mode.
SPI1 bootloader	SPI1	Enabled	The SPI1 configuration is: – Slave mode – Full Duplex – 8-bit MSB – Speed up to 8 MHz – Polarity: CPOL Low, CPHA Low, NSS hardware.
	SPI1_MOSI pin	Input	PA7 pin: Slave data Input line, used in push-pull, pull-down mode
	SPI1_MISO pin	Output	PA6 pin: Slave data output line, used in push-pull, pull-down mode.(1)
	SPI1_SCK pin	Input	PA5 pin: Slave clock line, used in push-pull, pull-down mode
	SPI1_NSS pin	Input	PA4 pin: slave chip select pin used in push-pull, pull-down mode. **Note:** This IO can be tied to GND if the SPI Master does not use it.

Table 131. STM32L412xx/422xx configuration in system memory boot mode (continued)

Bootloader	Feature/Peripheral	State	Comment
SPI2 bootloader	SPI2	Enabled	The SPI2 configuration is: – Slave mode – Full Duplex – 8-bit MSB – Speed up to 8 MHz Polarity: CPOL Low, CPHA Low, NSS hardware
	SPI2_MOSI pin	Input	PB15 pin: Slave data Input line, used in push-pull, pull-down mode
	SPI2_MISO pin	Output	PB14 pin: Slave data output line, used in push-pull, pull-down mode.(1)
	SPI2_SCK pin	Input	PB13 pin: Slave clock line, used in push-pull, pull-down mode
	SPI2_NSS pin	Input	PB12 pin: slave chip select pin used in push-pull, pull-down mode. **Note:** This IO can be tied to GND if the SPI Master does not use it.
DFU bootloader	USB	Enabled	USB FS configured in forced device mode. USB FS interrupt vector is enabled and used for USB DFU communications. **Note**: VDDUSB IO must be connected to 3.3 V as USB peripheral is used by the bootloader.
	USB_DM pin	Input/Output	PA11: USB DM line. Used in alternate push-pull, no pull mode.
	USB_DP pin		PA12: USB DP line. Used in alternate push-pull, no pull mode. No external pull-up resistor is required

1. SPI Tx (MISO) is handled by DMA. On the bootloader statup after SPI initialisation as soon as the bit DMATx enable on SPI CR2 register is set to 0x1, the MISO line will be set to 3.3 V.

Note: If VDDUSB pin is not connected to VDD, then SPI Flash memory write operations may be corrupted due to voltage issue. For more details, please refer to product's datasheet and errata sheet.

61.2 Bootloader selection

The figures below show the bootloader selection mechanism.

Figure 76. Dual bank boot Implementation for STM32L412xx/422xx bootloader V9.x

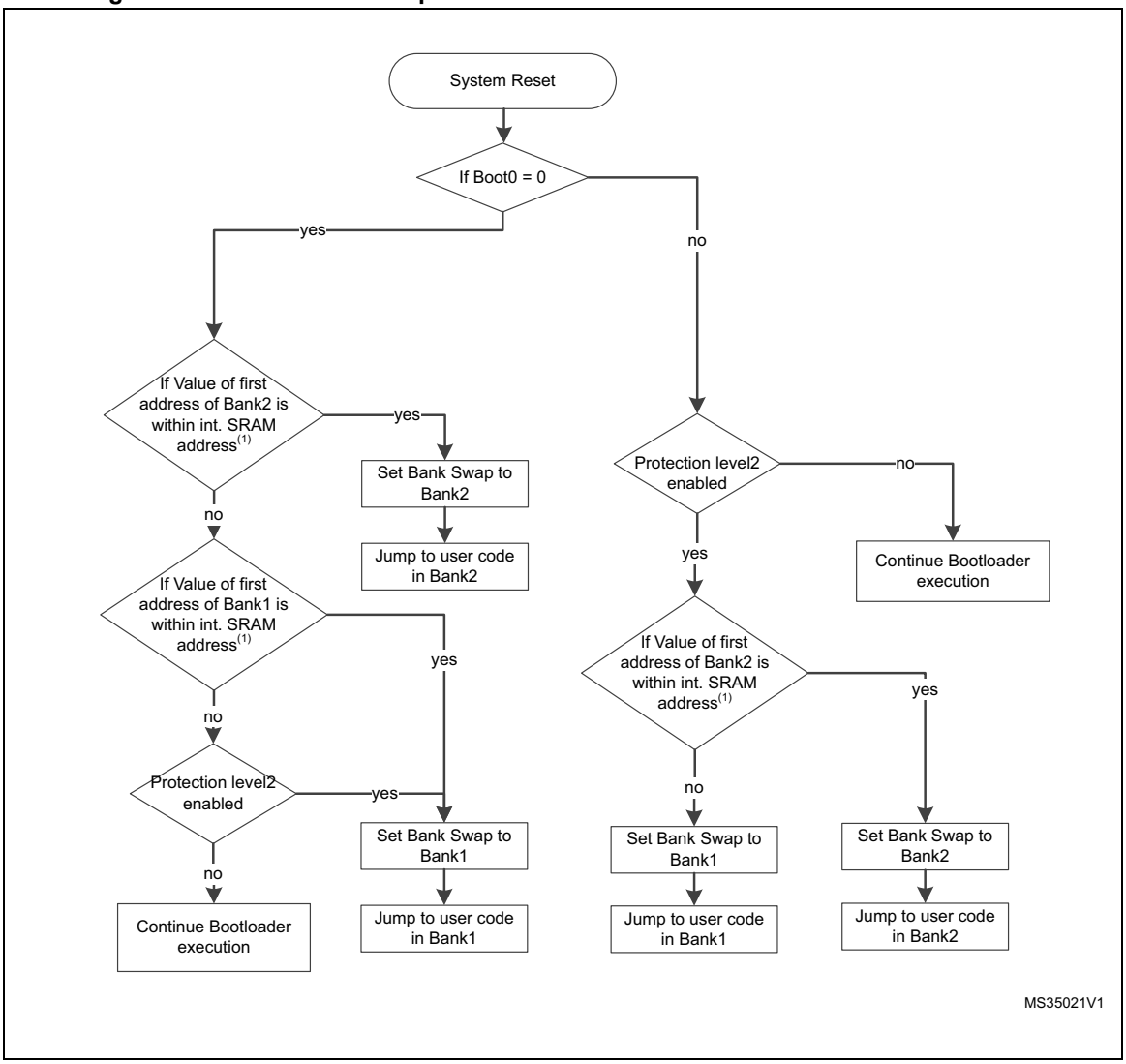
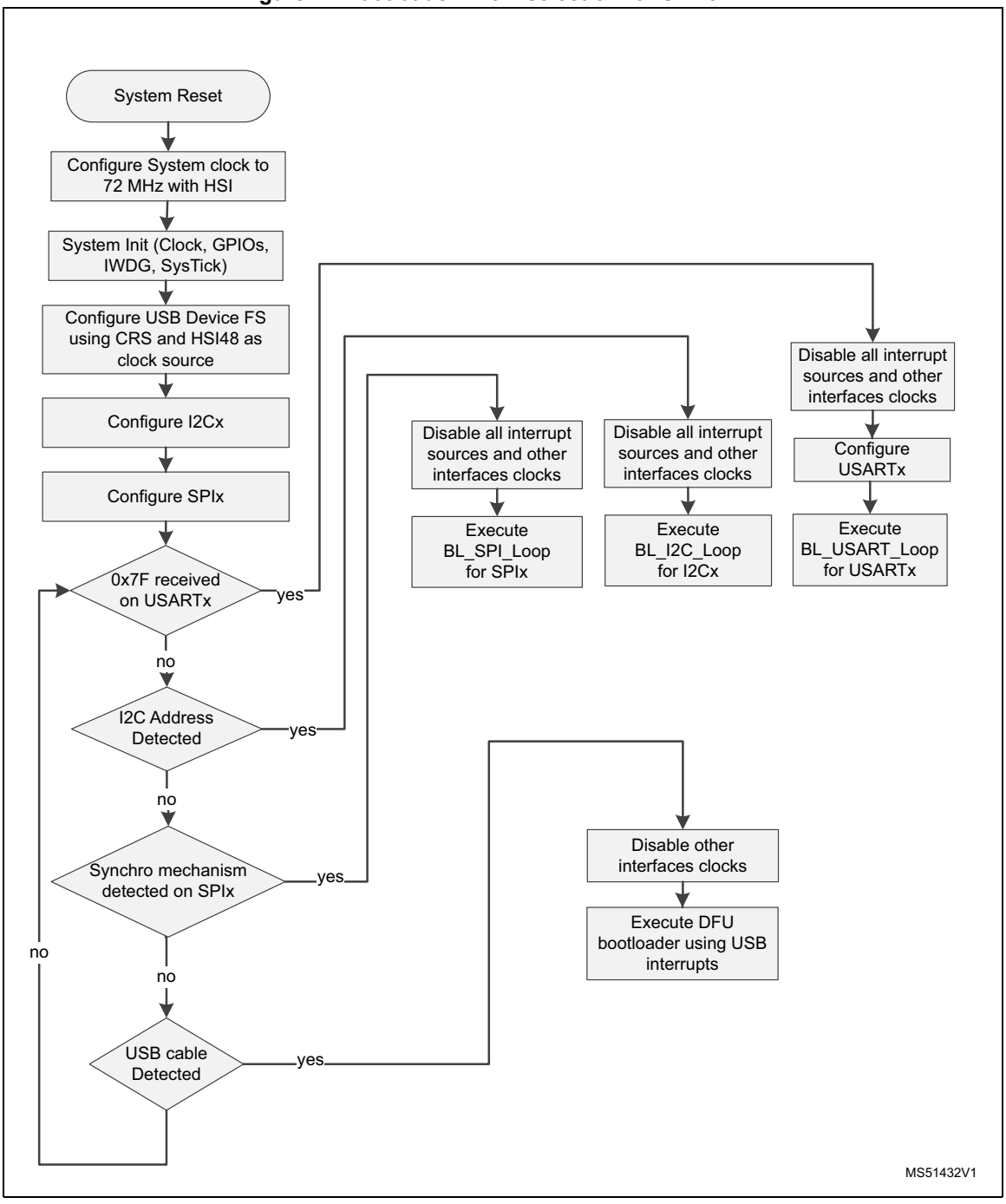


Figure 77.Bootloader V13.x selection for STM32L412xx/422xx



61.3 Bootloader version

Table 132 lists the STM32L412xx/422xx devices bootloader version.

Table 132. STM32L412xx/422xx bootloader versions

Bootloader version number	Description	Known limitations
V13.1	Initial bootloader version	– On connection phase, USART responds with two ACK bytes (0x79) instead of only one. – PcROP option bytes cannot be written as Bootloader uses Byte access while PcROP must be accessed using Half-Word access. **Workaround**: load a code snippest in SRAM using Bootloader interface then jump to it, and that code would write PcROP value.