



Escuela de Ingeniería en Computadores

CE-1109 Arquitectura de Computadores I

Tarea 2

Estudiante

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Profesor

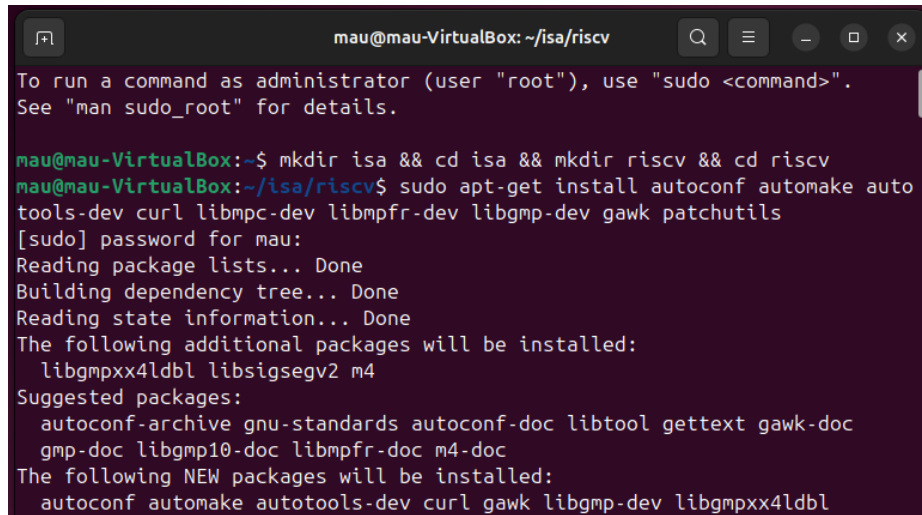
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RISCV

A continuación, se documentan las evidencias de la ejecución del debugging en RISCV así como las capturas de los pasos más importantes durante la instalación de las herramientas.

1. Primeramente, se crea la carpeta central ISA y se procede a crear un directorio solo para el debug de RISCV.

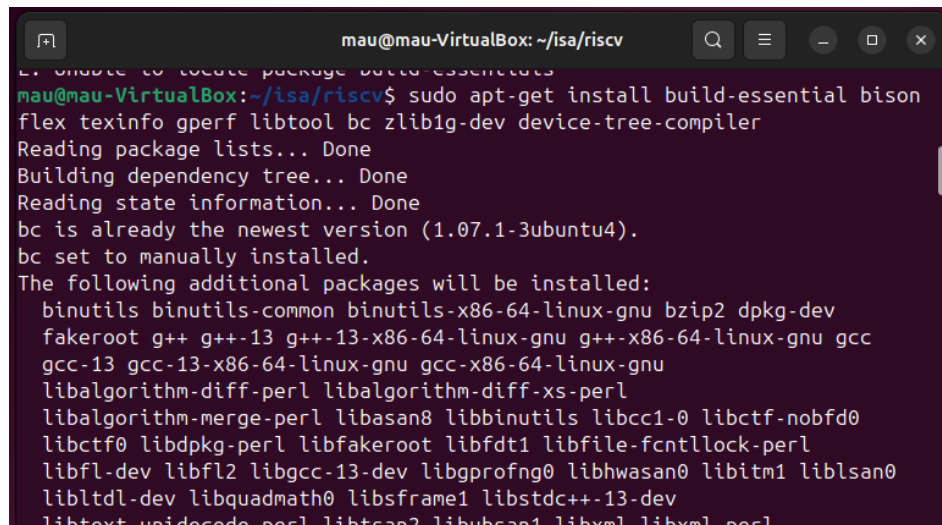
A terminal window titled 'mau@mau-VirtualBox: ~/isa/riscv'. It shows the execution of 'mkdir isa' and 'cd isa', followed by 'mkdir riscv' and 'cd riscv'. Then, 'sudo apt-get install autoconf automake autotools-dev curl libmpc-dev libmpfr-dev libgmp-dev gawk patchutils' is run. The terminal output shows the password prompt, package lists, dependency tree, and a list of additional packages to be installed: libgmpxx4ldbl, libsigsegv2, and m4. Suggested packages include autoconf-archive, gnu-standards, autoconf-doc, libtool, gettext, gawk-doc, gmp-doc, libgmp10-doc, libmpfr-doc, and m4-doc. The final list of NEW packages to be installed is autoconf, automake, autotools-dev, curl, gawk, libgmp-dev, libgmpxx4ldbl, and libsigsegv2.

```
mau@mau-VirtualBox: ~/isa/riscv
To run a command as administrator (user "root"), use "sudo <command>".
See "man sudo_root" for details.

mau@mau-VirtualBox:~$ mkdir isa && cd isa && mkdir riscv && cd riscv
mau@mau-VirtualBox:~/isa/riscv$ sudo apt-get install autoconf automake auto
tools-dev curl libmpc-dev libmpfr-dev libgmp-dev gawk patchutils
[sudo] password for mau:
Reading package lists... Done
Building dependency tree... Done
Reading state information... Done
The following additional packages will be installed:
  libgmpxx4ldbl libsigsegv2 m4
Suggested packages:
  autoconf-archive gnu-standards autoconf-doc libtool gettext gawk-doc
  gmp-doc libgmp10-doc libmpfr-doc m4-doc
The following NEW packages will be installed:
  autoconf automake autotools-dev curl gawk libgmp-dev libgmpxx4ldbl
```

Figura 1. Creación de directorios

2. Seguidamente se ejecutan los comandos para instalar las herramientas necesarias para realizar el debug de RISCV, al ser varios comandos, se observan a continuación en las Figuras 2 y 3.

A terminal window titled 'mau@mau-VirtualBox: ~/isa/riscv'. It shows the execution of 'sudo apt-get install build-essential bison flex texinfo gperf libtool bc zlib1g-dev device-tree-compiler'. The terminal output shows the password prompt, package lists, dependency tree, and a list of additional packages to be installed: binutils, binutils-common, binutils-x86-64-linux-gnu, bzip2, dpkg-dev, fakeroot, g++, g++-13, g++-13-x86-64-linux-gnu, g++-x86-64-linux-gnu, gcc, gcc-13, gcc-13-x86-64-linux-gnu, gcc-x86-64-linux-gnu, libalgorithm-diff-perl, libalgorithm-diff-xs-perl, libalgorithm-merge-perl, libasan8, libbinutils, libbctf1, libbctf-nobfd0, libbctf0, libdpkg-perl, libfakeroot, libfdt1, libfile-fcntllock-perl, libfl-dev, libfl2, libgcc-13-dev, libgprofng0, libhwasan0, libitm1, liblsan0, libltdl-dev, libquadmath0, libstdc++13-dev, libstdc++13-dev, libtext-unidecode-perl, libtsan2, libubsan1, libxml2, and libxml2-perl. The final list of NEW packages to be installed is build-essential, bison, flex, texinfo, gperf, libtool, bc, zlib1g-dev, device-tree-compiler, binutils, binutils-common, binutils-x86-64-linux-gnu, bzip2, dpkg-dev, fakeroot, g++, g++-13, g++-13-x86-64-linux-gnu, g++-x86-64-linux-gnu, gcc, gcc-13, gcc-13-x86-64-linux-gnu, gcc-x86-64-linux-gnu, libalgorithm-diff-perl, libalgorithm-diff-xs-perl, libalgorithm-merge-perl, libasan8, libbinutils, libbctf1, libbctf-nobfd0, libbctf0, libdpkg-perl, libfakeroot, libfdt1, libfile-fcntllock-perl, libfl-dev, libfl2, libgcc-13-dev, libgprofng0, libhwasan0, libitm1, liblsan0, libltdl-dev, libquadmath0, libstdc++13-dev, libstdc++13-dev, libtext-unidecode-perl, libtsan2, libubsan1, libxml2, and libxml2-perl.

```
mau@mau-VirtualBox:~/isa/riscv$ sudo apt-get install build-essential bison
flex texinfo gperf libtool bc zlib1g-dev device-tree-compiler
Reading package lists... Done
Building dependency tree... Done
Reading state information... Done
bc is already the newest version (1.07.1-3ubuntu4).
bc set to manually installed.
The following additional packages will be installed:
  binutils binutils-common binutils-x86-64-linux-gnu bzip2 dpkg-dev
  fakeroot g++ g++-13 g++-13-x86-64-linux-gnu g++-x86-64-linux-gnu gcc
  gcc-13 gcc-13-x86-64-linux-gnu gcc-x86-64-linux-gnu
  libalgorithm-diff-perl libalgorithm-diff-xs-perl
  libalgorithm-merge-perl libasan8 libbinutils libbctf1 libbctf-nobfd0
  libbctf0 libdpkg-perl libfakeroot libfdt1 libfile-fcntllock-perl
  libfl-dev libfl2 libgcc-13-dev libgprofng0 libhwasan0 libitm1 liblsan0
  libltdl-dev libquadmath0 libstdc++13-dev libstdc++13-dev
  libtext-unidecode-perl libtsan2 libubsan1 libxml2 libxml2-perl
```

Figura 2. Instalación de los paquetes

```
mau@mau-VirtualBox: ~/isa/riscv
Processing triggers for man-db (2.12.0-4ubuntu2) ...
Processing triggers for install-info (7.1-3build2) ...
mau@mau-VirtualBox:~/isa/riscv$ sudo apt-get install libexpat1-dev
Reading package lists... Done
Building dependency tree... Done
Reading state information... Done
The following NEW packages will be installed:
  libexpat1-dev
0 upgraded, 1 newly installed, 0 to remove and 87 not upgraded.
Need to get 139 kB of archives.
After this operation, 847 kB of additional disk space will be used.
Get:1 http://archive.ubuntu.com/ubuntu noble/main amd64 libexpat1-dev amd64
  2.6.1-2build1 [139 kB]
Fetched 139 kB in 6s (24.9 kB/s)
Selecting previously unselected package libexpat1-dev:amd64.
(Reading database ... 152595 files and directories currently installed.)
Preparing to unpack ../libexpat1-dev_2.6.1-2build1_amd64.deb ...
Unpacking libexpat1-dev:amd64 (2.6.1-2build1)
```

Figura 3. Instalación de los paquetes

3. Se clona el repositorio del toolchain de RISC-V.

```
mau@mau-VirtualBox: ~/isa/riscv
Processing triggers for man-db (2.12.0-4ubuntu2) ...
mau@mau-VirtualBox:~/isa/riscv$ git clone --recursive https://github.com/riscv/riscv-gnu-toolchain
Cloning into 'riscv-gnu-toolchain'...
remote: Enumerating objects: 9240, done.
remote: Counting objects: 100% (6/6), done.
remote: Compressing objects: 100% (6/6), done.
remote: Total 9240 (delta 2), reused 0 (delta 0), pack-reused 9234 (from 1)
Receiving objects: 100% (9240/9240), 6.34 MiB | 5.84 MiB/s, done.
Resolving deltas: 100% (4573/4573), done.
Submodule 'binutils' (https://sourceware.org/git/binutils-gdb.git) registered for path 'binutils'
Submodule 'dejagnu' (https://git.savannah.gnu.org/git/dejagnu.git) registered for path 'dejagnu'
Submodule 'gcc' (https://gcc.gnu.org/git/gcc.git) registered for path 'gcc'
Submodule 'gdb' (https://sourceware.org/git/binutils-gdb.git) registered for path 'gdb'
Submodule 'glibc' (https://sourceware.org/git/glibc.git) registered for path 'glibc'
```

Figura 4. Clonación del toolchain RISC-V

4. Ya con la toolchain construida y el RV8 instalado, se procede a realizar el debug del código del triángulo de pascal haciendo uso de las herramientas instaladas. Para este punto ya se creó el archivo .s y el mismo ya posee el código a ejecutar, por lo que se realiza la compilación y enlace, esto se muestra en la Figura 5.

```

mau@mau-VirtualBox: ~/isa/riscv/test
mau@mau-VirtualBox:~/isa/riscv/test$ riscv32-unknown-elf-as -march=rv32imafdc -o
test.o test.s
mau@mau-VirtualBox:~/isa/riscv/test$ riscv32-unknown-elf-ld -o test test.o
riscv32-unknown-elf-ld: warning: cannot find entry symbol _start; defaulting to
00010094

```

Figura 5. Compilación y enlazamiento.

5. Luego se procede a utilizar el debugger para comprobar el funcionamiento del código. Para esto se puede utilizar el “rv-jit -d test” el cual permite establecer breakpoints, sin embargo para que se vea un mejor flujo tambien podemos ejecutar simplemente “rv-jit test” y con la herramientas nos mostrará el cambio en los registros respectivos. En nuestro caso el que muestra el valor de como se va calculando el triangulo de pascal es t6, el cual es las siguientes imágenes se puede ver como este va conteniendo los valores del triangulo de pascal de un N = 5.

```

riscv32-unknown-elf-ld: warning: cannot find entry symbol _start; defaulting to 00010094
mau@mau-VirtualBox:~/isa/riscv/test$ rv-jit test
mau@mau-VirtualBox:~/isa/riscv/test$ rv-jit -d test
(rv-sim) run
mau@mau-VirtualBox:~/isa/riscv/test$ rv-jit -d test
(rv-sim) run 3000
0000000000000000 core-0 :00010094 (868a ) mv      a3, sp          a3=0x7fffff64, sp=0x7fffff64
0000000000000001 core-0 :00010096 (00001397) auipc   t2, pc + 4096    t2=0x11096
0000000000000002 core-0 :0001009a (08c3a383) lw      t2, 140(t2)    t2=0x5
0000000000000003 core-0 :0001009e (0076a023) sw      t2, 0(a3)    a3=0x7fffff64, t2=0x5
0000000000000004 core-0 :000100a2 (00468e13) addi    t3, a3, 4    a3=0x7fffff64, t3=0x7fffff68
0000000000000005 core-0 :000100a6 (4505 ) addi    a0, zero, 1  a0=0x1, zero=0x0
0000000000000006 core-0 :000100a8 (00ae2023) sw      a0, 0(t3)    a0=0x1, t3=0x7fffff68
0000000000000007 core-0 :000100ac (8ef2 ) mv      t4, t3      t3=0x7fffff68, t4=0x7fffff68
0000000000000008 core-0 :000100ae (8f72 ) mv      t5, t3      t3=0x7fffff68, t5=0x7fffff68
0000000000000009 core-0 :000100b0 (8972 ) mv      s2, t3      s2=0x7fffff68, t3=0x7fffff68
0000000000000010 core-0 :000100b2 (89f2 ) mv      s3, t3      s3=0x7fffff68, t3=0x7fffff68
0000000000000011 core-0 :000100b4 (4501 ) mv      a0, zero    a0=0x0, zero=0x0
0000000000000012 core-0 :000100b6 (0e11 ) addi    t3, t3, 4    t3=0x7fffff6c
0000000000000013 core-0 :000100b8 (4381 ) mv      t2, zero     t2=0x0, zero=0x0
0000000000000014 core-0 :000100ba (a009 ) j       pc + 2      pc = 2
0000000000000015 core-0 :000100bc (0006a303) lw      t1, 0(a3)    a3=0x7fffff64, t1=0x5
0000000000000016 core-0 :000100c0 (00651363) bne     a0, t1, pc + 6 a0=0x0, t1=0x5
0000000000000017 core-0 :000100c6 (0505 ) addi    a0, a0, 1    a0=0x1
0000000000000018 core-0 :000100c8 (00150393) addi    t2, a0, 1    a0=0x1, t2=0x2
0000000000000019 core-0 :000100cc (8eca ) mv      t4, s2      s2=0x7fffff68, t4=0x7fffff68
0000000000000020 core-0 :000100ce (8f4e ) mv      t5, s3      s3=0x7fffff68, t5=0x7fffff68
0000000000000021 core-0 :000100d0 (a009 ) j       pc + 2      pc = 2
0000000000000022 core-0 :000100d2 (00150f93) addi    t6, a0, 1    a0=0x1, t6=0x2
0000000000000023 core-0 :000100d6 (01f38663) beq     t2, t6, pc + 12 t2=0x2, t6=0x2
0000000000000024 core-0 :000100e2 (4f85 ) addi    t6, zero, 1  t6=0x1, zero=0x0
0000000000000025 core-0 :000100e4 (01fe2023) sw      t6, 0(t3)    t3=0x7fffff6c, t6=0x1
0000000000000026 core-0 :000100e8 (8972 ) mv      s2, t3      s2=0x7fffff6c, t3=0x7fffff6c
0000000000000027 core-0 :000100ea (0e11 ) addi    t3, t3, 4    t3=0x7fffff70
0000000000000028 core-0 :000100ec (13fd ) addi    t2, t2, -1    t2=0x1
0000000000000029 core-0 :000100ee (b7d5 ) j       pc - 28     pc = 28
0000000000000030 core-0 :000100d2 (00150f93) addi    t6, a0, 1    a0=0x1, t6=0x2
0000000000000031 core-0 :000100d6 (01f38663) beq     t2, t6, pc + 12 t2=0x1, t6=0x2
0000000000000032 core-0 :000100da (4f85 ) addi    t6, zero, 1  t6=0x1, zero=0x0
0000000000000033 core-0 :000100dc (01f38a63) beq     t2, t6, pc + 20 t2=0x1, t6=0x1
0000000000000034 core-0 :000100f0 (4f85 ) addi    t6, zero, 1  t6=0x1, zero=0x0
0000000000000035 core-0 :000100f2 (01fe2023) sw      t6, 0(t3)    t3=0x7fffff70, t6=0x1
0000000000000036 core-0 :000100f6 (89f2 ) mv      s3, t3      s3=0x7fffff70, t3=0x7fffff70
0000000000000037 core-0 :000100f8 (0e11 ) addi    t3, t3, 4    t3=0x7fffff74
0000000000000038 core-0 :000100fa (13fd ) addi    t2, t2, -1    t2=0x0

```

Figura 6. Debug del código en RISC V 1.


```

000000000000000039 core-0 :000100fc (b7c1) j pc - 64
000000000000000040 core-0 :000100bc (0006a303) lw t1, 0(a3) a3=0x7ffffff64, t1=0x5
000000000000000041 core-0 :000100c0 (00651363) bne a0, t1, pc + 6 a0=0x1, t1=0x5
000000000000000042 core-0 :000100c6 (0505) addi a0, a0, 1 a0=0x2
000000000000000043 core-0 :000100c8 (00150393) addi t2, a0, 1 a0=0x2, t2=0x3
000000000000000044 core-0 :000100cc (8eca) mv t4, s2 s2=0x7ffffff6c, t4=0x7ffffff6c
000000000000000045 core-0 :000100ce (8f4e) mv t5, s3 s3=0x7ffffff70, t5=0x7ffffff70
000000000000000046 core-0 :000100d0 (a009) j pc + 2
000000000000000047 core-0 :000100d2 (00150f93) addi t6, a0, 1 a0=0x2, t6=0x3
000000000000000048 core-0 :000100d6 (01f38663) beq t2, t6, pc + 12 t2=0x3, t6=0x3
000000000000000049 core-0 :000100e2 (4f85) addi t6, zero, 1 t6=0x1, zero=0x0
000000000000000050 core-0 :000100e4 (01fe2023) sw t6, 0(t3) t3=0x7ffffff74, t6=0x1
000000000000000051 core-0 :000100e8 (8972) mv s2, t3 s2=0x7ffffff74, t3=0x7ffffff74
000000000000000052 core-0 :000100ea (0e11) addi t3, t3, 4 t3=0x7ffffff78
000000000000000053 core-0 :000100ec (13fd) addi t2, t2, -1 t2=0x2
000000000000000054 core-0 :000100ee (b7d5) j pc - 28
000000000000000055 core-0 :000100d2 (00150f93) addi t6, a0, 1 a0=0x2, t6=0x3
000000000000000056 core-0 :000100d6 (01f38663) beq t2, t6, pc + 12 t2=0x2, t6=0x3
000000000000000057 core-0 :000100da (4f85) addi t6, zero, 1 t6=0x1, zero=0x0
000000000000000058 core-0 :000100dc (01f38a63) beq t2, t6, pc + 20 t2=0x2, t6=0x1
000000000000000059 core-0 :000100e0 (a839) j pc + 30
000000000000000060 core-0 :000100fe (000eaf83) lw t6, 0(t4) t4=0x7ffffff6c, t6=0x1
000000000000000061 core-0 :00010102 (004e8593) addi a1, t4, 4 a1=0x7ffffff70, t4=0x7ffffff6c
000000000000000062 core-0 :00010106 (0005a303) lw t1, 0(a1) a1=0x7ffffff70, t1=0x1
000000000000000063 core-0 :0001010a (9f9a) add t6, t6, t1 t1=0x1, t6=0x2
000000000000000064 core-0 :0001010c (01fe2023) sw t6, 0(t3) t3=0x7ffffff78, t6=0x2
000000000000000065 core-0 :00010110 (0e11) addi t3, t3, 4 t3=0x7ffffff7c
000000000000000066 core-0 :00010112 (0e91) addi t4, t4, 4 t4=0x7ffffff70
000000000000000067 core-0 :00010114 (13fd) addi t2, t2, -1 t2=0x1
000000000000000068 core-0 :00010116 (bf75) j pc - 68
000000000000000069 core-0 :000100d2 (00150f93) addi t6, a0, 1 a0=0x2, t6=0x3
000000000000000070 core-0 :000100d6 (01f38663) beq t2, t6, pc + 12 t2=0x1, t6=0x3
000000000000000071 core-0 :000100da (4f85) addi t6, zero, 1 t6=0x1, zero=0x0
000000000000000072 core-0 :000100dc (01f38a63) beq t2, t6, pc + 20 t2=0x1, t6=0x1
000000000000000073 core-0 :000100f0 (4f85) addi t6, zero, 1 t6=0x1, zero=0x0
000000000000000074 core-0 :000100f2 (01fe2023) sw t6, 0(t3) t3=0x7ffffff7c, t6=0x1
000000000000000075 core-0 :000100f6 (89f2) mv s3, t3 s3=0x7ffffff7c, t3=0x7ffffff7c
000000000000000076 core-0 :000100f8 (0e11) addi s3, t3, 4 s3=0x7ffffff80
000000000000000077 core-0 :000100fa (13fd) addi t2, t2, -1 t2=0x0
000000000000000078 core-0 :000100fc (b7c1) j pc - 64
000000000000000079 core-0 :000100bc (0006a303) lw t1, 0(a3) a3=0x7ffffff64, t1=0x5
000000000000000080 core-0 :000100c0 (00651363) bne a0, t1, pc + 6 a0=0x2, t1=0x5
000000000000000081 core-0 :000100c6 (0505) addi a0, a0, 1 a0=0x3
000000000000000082 core-0 :000100c8 (00150393) addi t2, a0, 1 a0=0x3, t2=0x4
000000000000000083 core-0 :000100cc (8eca) mv t4, s2 s2=0x7ffffff74, t4=0x7ffffff74

```

Figura 7. Debug del código en RISC-V 2.

```

000000000000000084 core-0 :000100ce (8f4e) mv t5, s3 s3=0x7ffffff7c, t5=0x7ffffff7c
000000000000000085 core-0 :000100d0 (a009) j pc + 2
000000000000000086 core-0 :000100d2 (00150f93) addi t6, a0, 1 a0=0x3, t6=0x4
000000000000000087 core-0 :000100d6 (01f38663) beq t2, t6, pc + 12 t2=0x4, t6=0x4
000000000000000088 core-0 :000100e2 (4f85) addi t6, zero, 1 t6=0x1, zero=0x0
000000000000000089 core-0 :000100e4 (01fe2023) sw t6, 0(t3) t3=0x7ffffff80, t6=0x1
000000000000000090 core-0 :000100e8 (8972) mv s2, t3 s2=0x7ffffff80, t3=0x7ffffff80
000000000000000091 core-0 :000100ea (0e11) addi t3, t3, 4 t3=0x7ffffff84
000000000000000092 core-0 :000100ec (13fd) addi t2, t2, -1 t2=0x3
000000000000000093 core-0 :000100ee (b7d5) j pc - 28
000000000000000094 core-0 :000100d2 (00150f93) addi t6, a0, 1 a0=0x3, t6=0x4
000000000000000095 core-0 :000100d6 (01f38663) beq t2, t6, pc + 12 t2=0x3, t6=0x4
000000000000000096 core-0 :000100da (4f85) addi t6, zero, 1 t6=0x1, zero=0x0
000000000000000097 core-0 :000100dc (01f38a63) beq t2, t6, pc + 20 t2=0x3, t6=0x1
000000000000000098 core-0 :000100e0 (a839) j pc + 30
000000000000000099 core-0 :000100fe (000eaf83) lw t6, 0(t4) t4=0x7ffffff74, t6=0x1
000000000000000100 core-0 :00010102 (004e8593) addi a1, t4, 4 a1=0x7ffffff78, t4=0x7ffffff74
000000000000000101 core-0 :00010106 (0005a303) lw t1, 0(a1) a1=0x7ffffff78, t1=0x2
000000000000000102 core-0 :0001010a (9f9a) add t6, t6, t1 t1=0x2, t6=0x3
000000000000000103 core-0 :0001010c (01fe2023) sw t6, 0(t3) t3=0x7ffffff84, t6=0x3
000000000000000104 core-0 :00010110 (0e11) addi t3, t3, 4 t3=0x7ffffff88
000000000000000105 core-0 :00010112 (0e91) addi t4, t4, 4 t4=0x7ffffff78
000000000000000106 core-0 :00010114 (13fd) addi t2, t2, -1 t2=0x2
000000000000000107 core-0 :00010116 (bf75) j pc - 68
000000000000000108 core-0 :000100d2 (00150f93) addi t6, a0, 1 a0=0x3, t6=0x4
000000000000000109 core-0 :000100d6 (01f38663) beq t2, t6, pc + 12 t2=0x2, t6=0x4
000000000000000110 core-0 :000100da (4f85) addi t6, zero, 1 t6=0x1, zero=0x0
000000000000000111 core-0 :000100dc (01f38a63) beq t2, t6, pc + 20 t2=0x2, t6=0x1
000000000000000112 core-0 :000100e0 (a839) j pc + 30
000000000000000113 core-0 :000100fe (000eaf83) lw t6, 0(t4) t4=0x7ffffff78, t6=0x2
000000000000000114 core-0 :00010102 (004e8593) addi a1, t4, 4 a1=0x7ffffff7c, t4=0x7ffffff78
000000000000000115 core-0 :00010106 (0005a303) lw t1, 0(a1) a1=0x7ffffff7c, t1=0x1
000000000000000116 core-0 :0001010a (9f9a) add t6, t6, t1 t1=0x1, t6=0x3
000000000000000117 core-0 :0001010c (01fe2023) sw t6, 0(t3) t3=0x7ffffff8, t6=0x3
000000000000000118 core-0 :00010110 (0e11) addi t3, t3, 4 t3=0x7ffffff8c
000000000000000119 core-0 :00010112 (0e91) addi t4, t4, 4 t4=0x7ffffff7c
000000000000000120 core-0 :00010114 (13fd) addi t2, t2, -1 t2=0x1
000000000000000121 core-0 :00010116 (bf75) j pc - 68
000000000000000122 core-0 :000100d2 (00150f93) addi t6, a0, 1 a0=0x3, t6=0x4
000000000000000123 core-0 :000100d6 (01f38663) beq t2, t6, pc + 12 t2=0x1, t6=0x4
000000000000000124 core-0 :000100da (4f85) addi t6, zero, 1 t6=0x1, zero=0x0
000000000000000125 core-0 :000100dc (01f38a63) beq t2, t6, pc + 20 t2=0x1, t6=0x1
000000000000000126 core-0 :000100f0 (4f85) addi t6, zero, 1 t6=0x1, zero=0x0
000000000000000127 core-0 :000100f2 (01fe2023) sw t6, 0(t3) t3=0x7ffffff8c, t6=0x1
000000000000000128 core-0 :000100f6 (89f2) mv s3, t3 s3=0x7ffffff8c, t3=0x7ffffff8c

```

Figura 8. Debug del código en RISC-V 3.


```

0000000000000000129 core-0 :000100f8 (0e11 ) addi t3, t3, 4 t3=0x7fffff90
0000000000000000130 core-0 :000100fa (13fd ) addi t2, t2, -1 t2=0x0
0000000000000000131 core-0 :000100fc (b7c1 ) j pc - 64
0000000000000000132 core-0 :000100bc (0006a303) lw t1, 0(a3) a3=0x7fffff64, t1=0x5
0000000000000000133 core-0 :000100c0 (00651363) bne a0, t1, pc + 6 a0=0x3, t1=0x5
0000000000000000134 core-0 :000100c6 (0505 ) addi a0, a0, 1 a0=0x4
0000000000000000135 core-0 :000100c8 (00150393) addi t2, a0, 1 a0=0x4, t2=0x5
0000000000000000136 core-0 :000100cc (8eca ) mv s2=0x7fffff80, t4=0x7fffff80
0000000000000000137 core-0 :000100ce (8f4e ) mv t5, s3 s3=0x7fffff8c, t5=0x7fffff8c
0000000000000000138 core-0 :000100d0 (a009 ) j pc + 2
0000000000000000139 core-0 :000100d2 (00150f93) addi t6, a0, 1 a0=0x4, t6=0x5
0000000000000000140 core-0 :000100d6 (01f38663) beq t2, t6, pc + 12 t2=0x5, t6=0x5
0000000000000000141 core-0 :000100e2 (4f85 ) addi t6, zero, 1 t6=0x1, zero=0x0
0000000000000000142 core-0 :000100e4 (01fe2023) sw t6, 0(t3) t3=0x7fffff90, t6=0x1
0000000000000000143 core-0 :000100e8 (8972 ) mv s2, t3 s2=0x7fffff90, t3=0x7fffff90
0000000000000000144 core-0 :000100ea (0e11 ) addi t3, t3, 4 t3=0x7fffff94
0000000000000000145 core-0 :000100ec (13fd ) addi t2, t2, -1 t2=0x4
0000000000000000146 core-0 :000100ee (b7d5 ) j pc - 28
0000000000000000147 core-0 :000100d2 (00150f93) addi t6, a0, 1 a0=0x4, t6=0x5
0000000000000000148 core-0 :000100d6 (01f38663) beq t2, t6, pc + 12 t2=0x4, t6=0x5
0000000000000000149 core-0 :000100da (4f85 ) addi t6, zero, 1 t6=0x1, zero=0x0
0000000000000000150 core-0 :000100dc (01f38a63) beq t2, t6, pc + 20 t2=0x4, t6=0x1
0000000000000000151 core-0 :000100e0 (a839 ) j pc + 30
0000000000000000152 core-0 :000100fe (000eaf83) lw t6, 0(t4) t4=0x7fffff80, t6=0x1
0000000000000000153 core-0 :00010102 (004e8593) addi a1, t4, 4 a1=0x7fffff84, t4=0x7fffff80
0000000000000000154 core-0 :00010106 (0005a303) lw t1, 0(a1) a1=0x7fffff84, t1=0x3
0000000000000000155 core-0 :0001010a (9f9a ) add t6, t6, t1 t1=0x3, t6=0x4
0000000000000000156 core-0 :0001010c (01fe2023) sw t6, 0(t3) t3=0x7fffff94, t6=0x4
0000000000000000157 core-0 :00010110 (0e11 ) addi t3, t3, 4 t3=0x7fffff98
0000000000000000158 core-0 :00010112 (0e91 ) addi t4, t4, 4 t4=0x7fffff84
0000000000000000159 core-0 :00010114 (13fd ) addi t2, t2, -1 t2=0x3
0000000000000000160 core-0 :00010116 (bf75 ) j pc - 68
0000000000000000161 core-0 :000100d2 (00150f93) addi t6, a0, 1 a0=0x4, t6=0x5
0000000000000000162 core-0 :000100d6 (01f38663) beq t2, t6, pc + 12 t2=0x3, t6=0x5
0000000000000000163 core-0 :000100da (4f85 ) addi t6, zero, 1 t6=0x1, zero=0x0
0000000000000000164 core-0 :000100dc (01f38a63) beq t2, t6, pc + 20 t2=0x3, t6=0x1
0000000000000000165 core-0 :000100e0 (a839 ) j pc + 30
0000000000000000166 core-0 :000100fe (000eaf83) lw t6, 0(t4) t4=0x7fffff84, t6=0x3
0000000000000000167 core-0 :00010102 (004e8593) addi a1, t4, 4 a1=0x7fffff88, t4=0x7fffff84
0000000000000000168 core-0 :00010106 (0005a303) lw t1, 0(a1) a1=0x7fffff88, t1=0x3
0000000000000000169 core-0 :0001010a (9f9a ) add t6, t6, t1 t1=0x3, t6=0x6
0000000000000000170 core-0 :0001010c (01fe2023) sw t6, 0(t3) t3=0x7fffff98, t6=0x6
0000000000000000171 core-0 :00010110 (0e11 ) addi t3, t3, 4 t3=0x7fffff9c
0000000000000000172 core-0 :00010112 (0e91 ) addi t4, t4, 4 t4=0x7fffff88
0000000000000000173 core-0 :00010114 (13fd ) addi t2, t2, -1 t2=0x2

```

Figura 9. Debug del código en RISC-V 4.

```

0000000000000000174 core-0 :00010116 (bf75 ) j pc - 68
0000000000000000175 core-0 :000100d2 (00150f93) addi t6, a0, 1 a0=0x4, t6=0x5
0000000000000000176 core-0 :000100d6 (01f38663) beq t2, t6, pc + 12 t2=0x2, t6=0x5
0000000000000000177 core-0 :000100da (4f85 ) addi t6, zero, 1 t6=0x1, zero=0x0
0000000000000000178 core-0 :000100dc (01f38a63) beq t2, t6, pc + 20 t2=0x2, t6=0x1
0000000000000000179 core-0 :000100e0 (a839 ) j pc + 30
0000000000000000180 core-0 :000100fe (000eaf83) lw t6, 0(t4) t4=0x7fffff88, t6=0x3
0000000000000000181 core-0 :00010102 (004e8593) addi a1, t4, 4 a1=0x7fffff8c, t4=0x7fffff88
0000000000000000182 core-0 :00010106 (0005a303) lw t1, 0(a1) a1=0x7fffff8c, t1=0x1
0000000000000000183 core-0 :0001010a (9f9a ) add t6, t6, t1 t1=0x1, t6=0x4
0000000000000000184 core-0 :0001010c (01fe2023) sw t6, 0(t3) t3=0x7fffff9c, t6=0x4
0000000000000000185 core-0 :00010110 (0e11 ) addi t3, t3, 4 t3=0x7fffffa0
0000000000000000186 core-0 :00010112 (0e91 ) addi t4, t4, 4 t4=0x7fffff8c
0000000000000000187 core-0 :00010114 (13fd ) addi t2, t2, -1 t2=0x1
0000000000000000188 core-0 :00010116 (bf75 ) j pc - 68
0000000000000000189 core-0 :000100d2 (00150f93) addi t6, a0, 1 a0=0x4, t6=0x5
0000000000000000190 core-0 :000100d6 (01f38663) beq t2, t6, pc + 12 t2=0x1, t6=0x5
0000000000000000191 core-0 :000100da (4f85 ) addi t6, zero, 1 t6=0x1, zero=0x0
0000000000000000192 core-0 :000100dc (01f38a63) beq t2, t6, pc + 20 t2=0x1, t6=0x1
0000000000000000193 core-0 :000100f0 (4f85 ) addi t6, zero, 1 t6=0x1, zero=0x0
0000000000000000194 core-0 :000100f2 (01fe2023) sw t6, 0(t3) t3=0x7fffffa0, t6=0x1
0000000000000000195 core-0 :000100f6 (89f2 ) mv s3, t3 s3=0x7fffffa0, t3=0x7fffffa0
0000000000000000196 core-0 :000100f8 (0e11 ) addi t3, t3, 4 t3=0x7fffffa4
0000000000000000197 core-0 :000100fa (13fd ) addi t2, t2, -1 t2=0x0
0000000000000000198 core-0 :000100fc (b7c1 ) j pc - 64
0000000000000000199 core-0 :000100bc (0006a303) lw t1, 0(a3) a3=0x7fffff64, t1=0x5
0000000000000000200 core-0 :000100c0 (00651363) bne a0, t1, pc + 6 a0=0x4, t1=0x5
0000000000000000201 core-0 :000100c6 (0505 ) addi a0, a0, 1 a0=0x5
0000000000000000202 core-0 :000100c8 (00150393) addi t2, a0, 1 a0=0x5, t2=0x6
0000000000000000203 core-0 :000100cc (8eca ) mv s2=0x7fffff90, t4=0x7fffff90
0000000000000000204 core-0 :000100ce (8f4e ) mv t5, s3 s3=0x7fffffa0, t5=0x7fffffa0
0000000000000000205 core-0 :000100d0 (a009 ) j pc + 2
0000000000000000206 core-0 :000100d2 (00150f93) addi t6, a0, 1 a0=0x5, t6=0x6
0000000000000000207 core-0 :000100d6 (01f38663) beq t2, t6, pc + 12 t2=0x6, t6=0x6
0000000000000000208 core-0 :000100e2 (4f85 ) addi t6, zero, 1 t6=0x1, zero=0x0
0000000000000000209 core-0 :000100e4 (01fe2023) sw t6, 0(t3) t3=0x7fffffa4, t6=0x1
0000000000000000210 core-0 :000100e8 (8972 ) mv s2, t3 s2=0x7fffffa4, t3=0x7fffffa4
0000000000000000211 core-0 :000100ea (0e11 ) addi t3, t3, 4 t3=0x7fffffa8
0000000000000000212 core-0 :000100ec (13fd ) addi t2, t2, -1 t2=0x5
0000000000000000213 core-0 :000100ee (b7d5 ) j pc - 28
0000000000000000214 core-0 :000100d2 (00150f93) addi t6, a0, 1 a0=0x5, t6=0x6
0000000000000000215 core-0 :000100d6 (01f38663) beq t2, t6, pc + 12 t2=0x5, t6=0x6
0000000000000000216 core-0 :000100da (4f85 ) addi t6, zero, 1 t6=0x1, zero=0x0
0000000000000000217 core-0 :000100dc (01f38a63) beq t2, t6, pc + 20 t2=0x5, t6=0x1
0000000000000000218 core-0 :000100e0 (a839 ) j pc + 30

```

Figura 10. Debug del código en RISC-V 5.

```

0000000000000000219 core-0 :000100fe (000eaf83) lw t6, 0(t4) t4=0x7fffff90, t6=0x1
0000000000000000220 core-0 :00010102 (004e8593) addi a1, t4, 4 a1=0x7fffff94, t4=0x7fffff90
0000000000000000221 core-0 :00010106 (0005a303) lw t1, 0(a1) a1=0x7fffff94, t1=0x4
0000000000000000222 core-0 :0001010a (9f9a) add t6, t6, t1 t1=0x4, t6=0x5
0000000000000000223 core-0 :0001010c (01fe2023) sw t6, 0(t3) t3=0x7fffffa8, t6=0x5
0000000000000000224 core-0 :00010110 (0e11) addi t3, t3, 4 t3=0x7fffffac
0000000000000000225 core-0 :00010112 (0e91) addi t4, t4, 4 t4=0x7fffff94
0000000000000000226 core-0 :00010114 (13fd) addi t2, t2, -1 t2=0x4
0000000000000000227 core-0 :00010116 (bf75) j pc - 68
0000000000000000228 core-0 :000100d2 (00150f93) addi t6, a0, 1 a0=0x5, t6=0x6
0000000000000000229 core-0 :000100d6 (01f38663) beq t2, t6, pc + 12 t2=0x4, t6=0x6
0000000000000000230 core-0 :000100da (4f85) addi t6, zero, 1 t6=0x1, zero=0x0
0000000000000000231 core-0 :000100dc (01f38a63) beq t2, t6, pc + 20 t2=0x4, t6=0x1
0000000000000000232 core-0 :000100e0 (a839) j pc + 30
0000000000000000233 core-0 :000100fe (000eaf83) lw t6, 0(t4) t4=0x7fffff94, t6=0x4
0000000000000000234 core-0 :00010102 (004e8593) addi a1, t4, 4 a1=0x7fffff98, t4=0x7fffff94
0000000000000000235 core-0 :00010106 (0005a303) lw t1, 0(a1) a1=0x7fffff98, t1=0x6
0000000000000000236 core-0 :0001010a (9f9a) add t6, t6, t1 t1=0x6, t6=0xa
0000000000000000237 core-0 :0001010c (01fe2023) sw t6, 0(t3) t3=0x7fffffac, t6=0xa
0000000000000000238 core-0 :00010110 (0e11) addi t3, t3, 4 t3=0x7fffffb0
0000000000000000239 core-0 :00010112 (0e91) addi t4, t4, 4 t4=0x7fffff98
0000000000000000240 core-0 :00010114 (13fd) addi t2, t2, -1 t2=0x3
0000000000000000241 core-0 :00010116 (bf75) j pc - 68
0000000000000000242 core-0 :000100d2 (00150f93) addi t6, a0, 1 a0=0x5, t6=0x6
0000000000000000243 core-0 :000100d6 (01f38663) beq t2, t6, pc + 12 t2=0x3, t6=0x6
0000000000000000244 core-0 :000100da (4f85) addi t6, zero, 1 t6=0x1, zero=0x0
0000000000000000245 core-0 :000100dc (01f38a63) beq t2, t6, pc + 20 t2=0x3, t6=0x1
0000000000000000246 core-0 :000100e0 (a839) j pc + 30
0000000000000000247 core-0 :000100fe (000eaf83) lw t6, 0(t4) t4=0x7fffff98, t6=0x6
0000000000000000248 core-0 :00010102 (004e8593) addi a1, t4, 4 a1=0x7fffff9c, t4=0x7fffff98
0000000000000000249 core-0 :00010106 (0005a303) lw t1, 0(a1) a1=0x7fffff9c, t1=0x4
0000000000000000250 core-0 :0001010a (9f9a) add t6, t6, t1 t1=0x4, t6=0xa
0000000000000000251 core-0 :0001010c (01fe2023) sw t6, 0(t3) t3=0x7fffffb0, t6=0xa
0000000000000000252 core-0 :00010110 (0e11) addi t3, t3, 4 t3=0x7fffffb4
0000000000000000253 core-0 :00010112 (0e91) addi t4, t4, 4 t4=0x7fffff9c
0000000000000000254 core-0 :00010114 (13fd) addi t2, t2, -1 t2=0x2
0000000000000000255 core-0 :00010116 (bf75) j pc - 68
0000000000000000256 core-0 :000100d2 (00150f93) addi t6, a0, 1 a0=0x5, t6=0x6
0000000000000000257 core-0 :000100d6 (01f38663) beq t2, t6, pc + 12 t2=0x2, t6=0x6
0000000000000000258 core-0 :000100da (4f85) addi t6, zero, 1 t6=0x1, zero=0x0
0000000000000000259 core-0 :000100dc (01f38a63) beq t2, t6, pc + 20 t2=0x2, t6=0x1
0000000000000000260 core-0 :000100e0 (a839) j pc + 30
0000000000000000261 core-0 :000100fe (000eaf83) lw t6, 0(t4) t4=0x7fffff9c, t6=0x4
0000000000000000262 core-0 :00010102 (004e8593) addi a1, t4, 4 a1=0x7fffffa0, t4=0x7fffff9c
0000000000000000263 core-0 :00010106 (0005a303) lw t1, 0(a1) a1=0x7fffffa0, t1=0x1

```

Figura 11. Debug del código en RISCv 6.

```

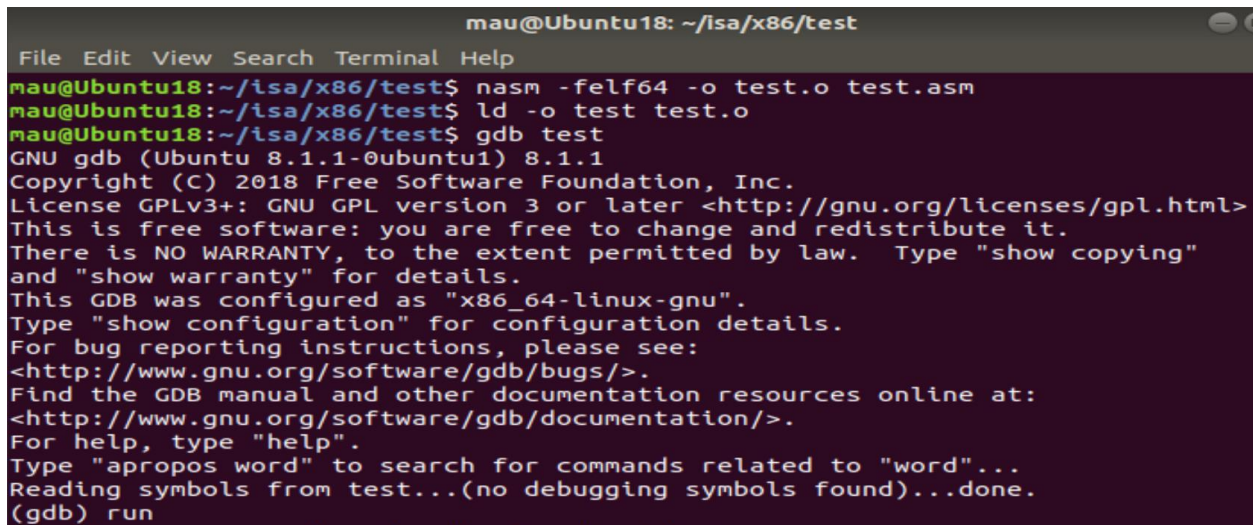
0000000000000000259 core-0 :000100dc (01f38a63) beq t2, t6, pc + 20 t2=0x2, t6=0x1
0000000000000000260 core-0 :000100e0 (a839) j pc + 30
0000000000000000261 core-0 :000100fe (000eaf83) lw t6, 0(t4) t4=0x7fffff9c, t6=0x4
0000000000000000262 core-0 :00010102 (004e8593) addi a1, t4, 4 a1=0x7fffffa0, t4=0x7fffff9c
0000000000000000263 core-0 :00010106 (0005a303) lw t1, 0(a1) a1=0x7fffffa0, t1=0x1
0000000000000000264 core-0 :0001010a (9f9a) add t6, t6, t1 t1=0x1, t6=0x5
0000000000000000265 core-0 :0001010c (01fe2023) sw t6, 0(t3) t3=0x7fffffb4, t6=0x5
0000000000000000266 core-0 :00010110 (0e11) addi t3, t3, 4 t3=0x7fffffb8
0000000000000000267 core-0 :00010112 (0e91) addi t4, t4, 4 t4=0x7fffffa0
0000000000000000268 core-0 :00010114 (13fd) addi t2, t2, -1 t2=0x1
0000000000000000269 core-0 :00010116 (bf75) j pc - 68
0000000000000000270 core-0 :000100d2 (00150f93) addi t6, a0, 1 a0=0x5, t6=0x6
0000000000000000271 core-0 :000100d6 (01f38663) beq t2, t6, pc + 12 t2=0x1, t6=0x6
0000000000000000272 core-0 :000100da (4f85) addi t6, zero, 1 t6=0x1, zero=0x0
0000000000000000273 core-0 :000100dc (01f38a63) beq t2, t6, pc + 20 t2=0x1, t6=0x1
0000000000000000274 core-0 :000100f0 (4f85) addi t6, zero, 1 t6=0x1, zero=0x0
0000000000000000275 core-0 :000100f2 (01fe2023) sw t6, 0(t3) t3=0x7fffffb8, t6=0x1
0000000000000000276 core-0 :000100f6 (89f2) mv s3, t3 s3=0x7fffffb8, t3=0x7fffffb8
0000000000000000277 core-0 :000100f8 (0e11) addi t3, t3, 4 t3=0x7fffffbc
0000000000000000278 core-0 :000100fa (13fd) addi t2, t2, -1 t2=0x0
0000000000000000279 core-0 :000100fc (b7c1) j pc - 64
0000000000000000280 core-0 :000100bc (0006a303) lw t1, 0(a3) a3=0x7fffff64, t1=0x5
0000000000000000281 core-0 :000100c0 (00651363) bne a0, t1, pc + 6 a0=0x5, t1=0x5
0000000000000000282 core-0 :000100c4 (a891) j pc + 84
0000000000000000283 core-0 :00010118 (05d00893) addi a7, zero, 93 a7=0x5d, zero=0x0
0000000000000000284 core-0 :0001011c (4501) mv a0, zero a0=0x0, zero=0x0

```

Figura 12. Debug del código en RISCv 7.

X86

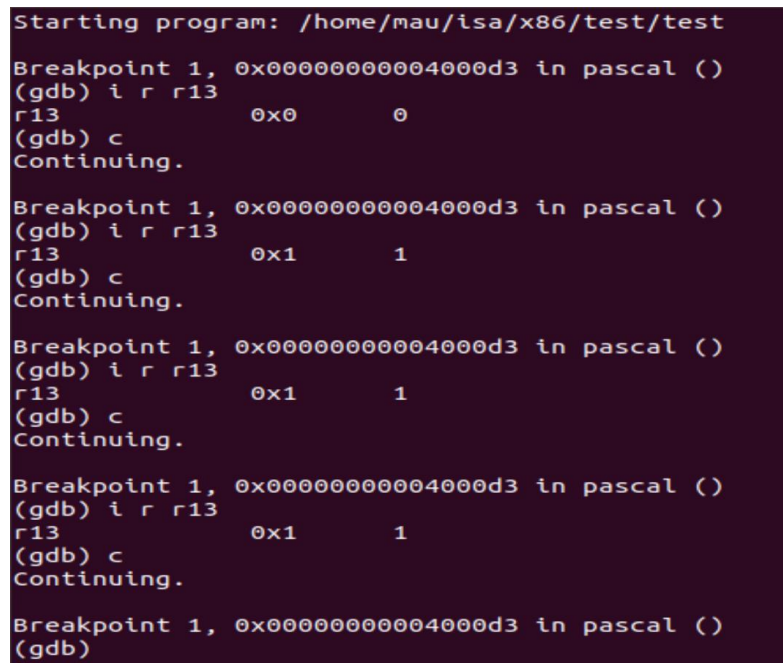
En el caso de x86 se instaló GDB para poder realizar el debug respectivo del código, este no presentó ningún problema durante la instalación, luego de esto se crearon las carpetas y el archivo .asm respectivo, el cual también se adjunta con este documento. Seguidamente se realizó la compilación y enlazamiento del código y se procedió a utilizar GDB para comenzar el debug, esto se muestra en la Figura 13.



```
mau@Ubuntu18: ~/isa/x86/test
File Edit View Search Terminal Help
mau@Ubuntu18:~/isa/x86/test$ nasm -felf64 -o test.o test.asm
mau@Ubuntu18:~/isa/x86/test$ ld -o test test.o
mau@Ubuntu18:~/isa/x86/test$ gdb test
GNU gdb (Ubuntu 8.1.1-0ubuntu1) 8.1.1
Copyright (C) 2018 Free Software Foundation, Inc.
License GPLv3+: GNU GPL version 3 or later <http://gnu.org/licenses/gpl.html>
This is free software: you are free to change and redistribute it.
There is NO WARRANTY, to the extent permitted by law. Type "show copying"
and "show warranty" for details.
This GDB was configured as "x86_64-linux-gnu".
Type "show configuration" for configuration details.
For bug reporting instructions, please see:
<http://www.gnu.org/software/gdb/bugs/>.
Find the GDB manual and other documentation resources online at:
<http://www.gnu.org/software/gdb/documentation/>.
For help, type "help".
Type "apropos word" to search for commands related to "word"...
Reading symbols from test...(no debugging symbols found)...done.
(gdb) run
```

Figura 13. Compilación y enlazamiento del código en x86.

Seguidamente se muestran las capturas del programa en debugging usando GDB



```
Starting program: /home/mau/isa/x86/test/test
Breakpoint 1, 0x00000000004000d3 in pascal ()
(gdb) i r r13
r13          0x0          0
(gdb) c
Continuing.

Breakpoint 1, 0x00000000004000d3 in pascal ()
(gdb) i r r13
r13          0x1          1
(gdb) c
Continuing.

Breakpoint 1, 0x00000000004000d3 in pascal ()
(gdb) i r r13
r13          0x1          1
(gdb) c
Continuing.

Breakpoint 1, 0x00000000004000d3 in pascal ()
(gdb) i r r13
r13          0x1          1
(gdb) c
Continuing.

Breakpoint 1, 0x00000000004000d3 in pascal ()
(gdb)
```

Figura 14. Debug x86 iteración 1


```

Breakpoint 1, 0x00000000004000d3 in pascal ()
(gdb) i r r13
r13          0x15      2
(gdb) c
Continuing.

Breakpoint 1, 0x00000000004000d3 in pascal ()
(gdb) i r r13
r13          0x1       1
(gdb) c
Continuing.

Breakpoint 1, 0x00000000004000d3 in pascal ()
(gdb) i r r13
r13          0x1       1
(gdb) c
Continuing.

Breakpoint 1, 0x00000000004000d3 in pascal ()
(gdb) i r r13
r13          0x5       5
(gdb) c
Continuing.

Breakpoint 1, 0x00000000004000d3 in pascal ()
(gdb) i r r13
r13          0xd      13
(gdb)

```

Figura 15. Debug x86 iteración 2

```

Continuing.

Breakpoint 1, 0x00000000004000d3 in pascal ()
(gdb) i r r13
r13          0x5       5
(gdb) c
Continuing.

Breakpoint 1, 0x00000000004000d3 in pascal ()
(gdb) i r r13
r13          0x1       1
(gdb) c
Continuing.

Breakpoint 1, 0x00000000004000d3 in pascal ()
(gdb) i r r13
r13          0x1       1
(gdb) c
Continuing.

Breakpoint 1, 0x00000000004000d3 in pascal ()
(gdb) i r r13
r13          0x5       5
(gdb) c
Continuing.

Breakpoint 1, 0x00000000004000d3 in pascal ()
(gdb)

```

Figura 16. Debug x86 iteración 3

```

Breakpoint 1, 0x00000000004000d3 in pascal ()
(gdb) i r r13
r13          0xd      13
(gdb) c
Continuing.

Breakpoint 1, 0x00000000004000d3 in pascal ()
(gdb) i r r13
r13          0x1       1
(gdb) c
Continuing.

Breakpoint 1, 0x00000000004000d3 in pascal ()
(gdb) i r r13
r13          0x1       1
(gdb) c
Continuing.

Breakpoint 1, 0x00000000004000d3 in pascal ()
(gdb) i r r13
r13          0x5       5
(gdb) c
Continuing.

Breakpoint 1, 0x00000000004000d3 in pascal ()
(gdb) i r r13
r13          0xd      13
(gdb)

```

Figura 17. Debug x86 iteración 4

ARM

Por último para ARM se tuvo que realizar utilizando qemu y realizando el debug por sockets, para esto se hizo uso del puerto 1233 y con la ayuda de dos terminales se pudo realizar el debug del código en ARM que fue el original entregado en la tarea 1. A continuación se muestran las imágenes del debug paso a paso del código en ARM señalando el estado del registro R7 que es el que almacenaba los valores calculados del triángulo de pascal.

Debido a que el breakpoint establecido en la sección pascal, no es posible observar el primer valor de 1 por lo que en la iteración 1 el valor sale como 0, pero en realidad en memoria si se quiere el nivel 0 que es 1.

```

r0          0x1       1
r1          0xffffef0c8 -69432
r2          0xffffef0c4 -69436
r3          0xffffef0c4 -69436
r4          0x2        2
r5          0x0        0
r6          0xffffef0c0 -69440
r7          0x0        0

```

Figura 18 Debug ARM iteración 1

```

r0          0x1       1
r1          0xffffef0cc -69428
r2          0xffffef0c4 -69436
r3          0xffffef0c4 -69436
r4          0x1        1
r5          0x2        2
r6          0xffffef0c0 -69440
r7          0x1        1

```

Figura 19 Debug ARM iteración 2

r0	0x1	1	
r1	0xffffef0cc		-69428
r2	0xffffef0c4		-69436
r3	0xffffef0c4		-69436
r4	0x1	1	
r5	0x2	2	
r6	0xffffef0c0		-69440
r7	0x1	1	

Figura 20 Debug ARM iteración 3

r0	0x1	1	
r1	0xffffef0cc		-69428
r2	0xffffef0c4		-69436
r3	0xffffef0c4		-69436
r4	0x1	1	
r5	0x2	2	
r6	0xffffef0c0		-69440
r7	0x1	1	

Figura 21 Debug ARM iteración 4

r0	0x2	2	
r1	0xffffef0d8		-69416
r2	0xffffef0cc		-69428
r3	0xffffef0cc		-69428
r4	0x1	1	
r5	0x1	1	
r6	0xffffef0c0		-69440
r7	0x2	2	

Figura 22 Debug ARM iteración 5

r0	0x3	3	
r1	0xffffef0dc		-69412
r2	0xffffef0d0		-69424
r3	0xffffef0d8		-69416
r4	0x4	4	
r5	0x3	3	
r6	0xffffef0c0		-69440
r7	0x1	1	

Figura 23 Debug ARM iteración 6

r0	0x3	3	
r1	0xffffef0e0		-69408
r2	0xffffef0d0		-69424
r3	0xffffef0d8		-69416
r4	0x3	3	
r5	0x4	4	
r6	0xffffef0c0		-69440
r7	0x1	1	

Figura 24 Debug ARM iteración 7

r0	0x3	3	
r1	0xffffef0e4		-69404
r2	0xffffef0d4		-69420
r3	0xffffef0d8		-69416
r4	0x2	2	
r5	0x1	1	
r6	0xffffef0c0		-69440
r7	0x3	3	

Figura 25 Debug ARM iteración 8

r0	0x3	3	
r1	0xffffef0e8		-69400
r2	0xffffef0d8		-69416
r3	0xffffef0d8		-69416
r4	0x1	1	
r5	0x2	2	
r6	0xffffef0c0		-69440
r7	0x3	3	

Figura 26 Debug ARM iteración 9

r0	0x4	4	
r1	0xffffef0ec		-69396
r2	0xffffef0dc		-69412
r3	0xffffef0e8		-69400
r4	0x5	5	
r5	0x4	4	
r6	0xffffef0c0		-69440
r7	0x1	1	

Figura 27 Debug ARM iteración 10

r0	0x4	4	
r1	0xffffef0f0		-69392
r2	0xffffef0dc		-69412
r3	0xffffef0e8		-69400
r4	0x4	4	
r5	0x5	5	
r6	0xffffef0c0		-69440
r7	0x1	1	

Figura 28 Debug ARM iteración 11

r0	0x4	4	
r1	0xffffef0f4		-69388
r2	0xffffef0e0		-69408
r3	0xffffef0e8		-69400
r4	0x3	3	
r5	0x1	1	
r6	0xffffef0c0		-69440
r7	0x4	4	

Figura 29 Debug ARM iteración 12

r0	0x4	4	
r1	0xffffef0f8		-69384
r2	0xffffef0e4		-69404
r3	0xffffef0e8		-69400
r4	0x2	2	
r5	0x3	3	
r6	0xffffef0c0		-69440
r7	0x6	6	

Figura 30 Debug ARM iteración 13

r0	0x4	4	
r1	0xffffef0fc		-69380
r2	0xffffef0e8		-69400
r3	0xffffef0e8		-69400
r4	0x1	1	
r5	0x3	3	
r6	0xffffef0c0		-69440
r7	0x4	4	

Figura 31 Debug ARM iteración 14

r0	0x5	5	
r1	0xffffef100		-69376
r2	0xffffef0ec		-69396
r3	0xffffef0fc		-69380
r4	0x6	6	
r5	0x5	5	
r6	0xffffef0c0		-69440
r7	0x1	1	

Figura 32 Debug ARM iteración 15

r0	0x5	5	
r1	0xffffef104		-69372
r2	0xffffef0ec		-69396
r3	0xffffef0fc		-69380
r4	0x5	5	
r5	0x6	6	
r6	0xffffef0c0		-69440
r7	0x1	1	

Figura 33 Debug ARM iteración 16

r0	0x5	5	
r1	0xffffef108		-69368
r2	0xffffef0f0		-69392
r3	0xffffef0fc		-69380
r4	0x4	4	
r5	0x1	1	
r6	0xffffef0c0		-69440
r7	0x5	5	

Figura 34 Debug ARM iteración 17

r0	0x5	5	
r1	0xffffef10c		-69364
r2	0xffffef0f4		-69388
r3	0xffffef0fc		-69380
r4	0x3	3	
r5	0x4	4	
r6	0xffffef0c0		-69440
r7	0xa	10	

Figura 35 Debug ARM iteración 18

r0	0x5	5	
r1	0xffffef110		-69360
r2	0xffffef0f8		-69384
r3	0xffffef0fc		-69380
r4	0x2	2	
r5	0x6	6	
r6	0xffffef0c0		-69440
r7	0xa	10	

Figura 36 Debug ARM iteración 19

r0	0x5	5	
r1	0xffffef114		-69356
r2	0xffffef0fc		-69380
r3	0xffffef0fc		-69380
r4	0x1	1	
r5	0x4	4	
r6	0xffffef0c0		-69440
r7	0x5	5	

Figura 37 Debug ARM iteración 20

El ultimo 1 no es posible mostrarlo ya que pasa algo parecido al primer 1 el cual no se puede mostrar sin embargo acá tampoco se muestra el registro porque no llega a pasar por la etiqueta “pascal” que es la que muestra los registros sino que sale directamente del programa y muestra este mensaje, confirmando que el código finalizo.

```
Continuing.
[Inferior 1 (Remote target) exited normally]
(gdb) i r
The program has no registers now.
(gdb) █
```

Figura 38 Debug ARM última iteración