Lab 3

Agenda

- Review Verilog
- Understand Timing
- Memory
- Debugging

Review: Don’t

- Don’t use “assign” statement inside always block.
- Don’t add code inside generate-for only component instantiations.
- Don’t mix sensitivity list parameters with different edges, only use one clk (one edge at an always block)
- Don’t mix blocking and non-blocking assignment unless you know what you are doing.
- Don’t set a value in two different blocks
  - Inside & outside always block
  - Inside two different always blocks

Review: Do

- Do use always block for each edge
- Do use non-blocking(<=) assignment, if element is synchronized.
- Do use blocking (=) assignment, if making intermediate calculation.
- Do add assertions and displays to summarize the testing results

Review: Remember

- Reg: doesn’t always mean register, your code decides what it means.
- Assign: is hard wiring.
- Missing conditions generate memory elements (posedge/negedge) leads to missing conditions.
- Only registers, latches, memories require clock. Please don’t add clock to combinational elements.

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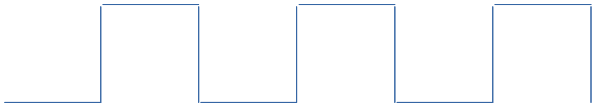
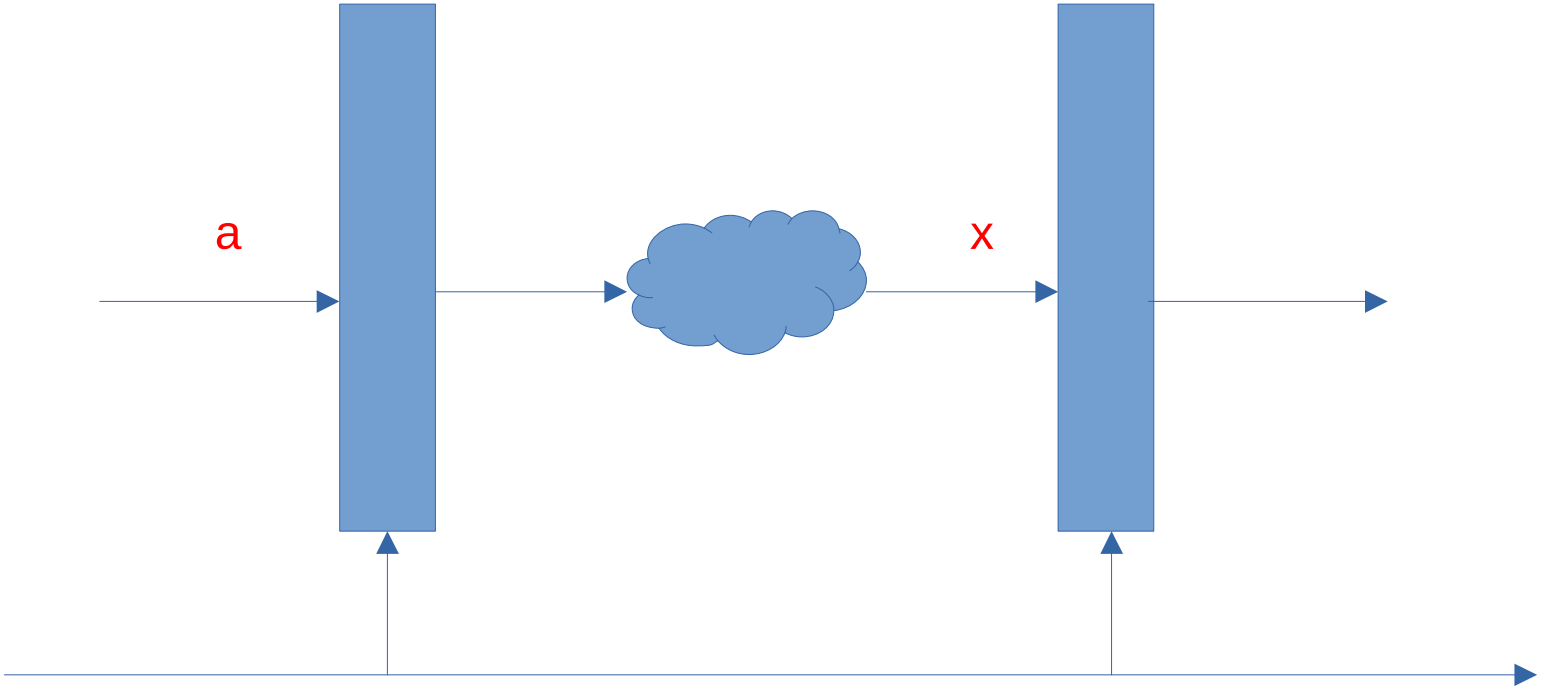
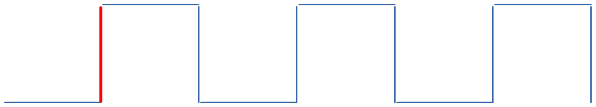
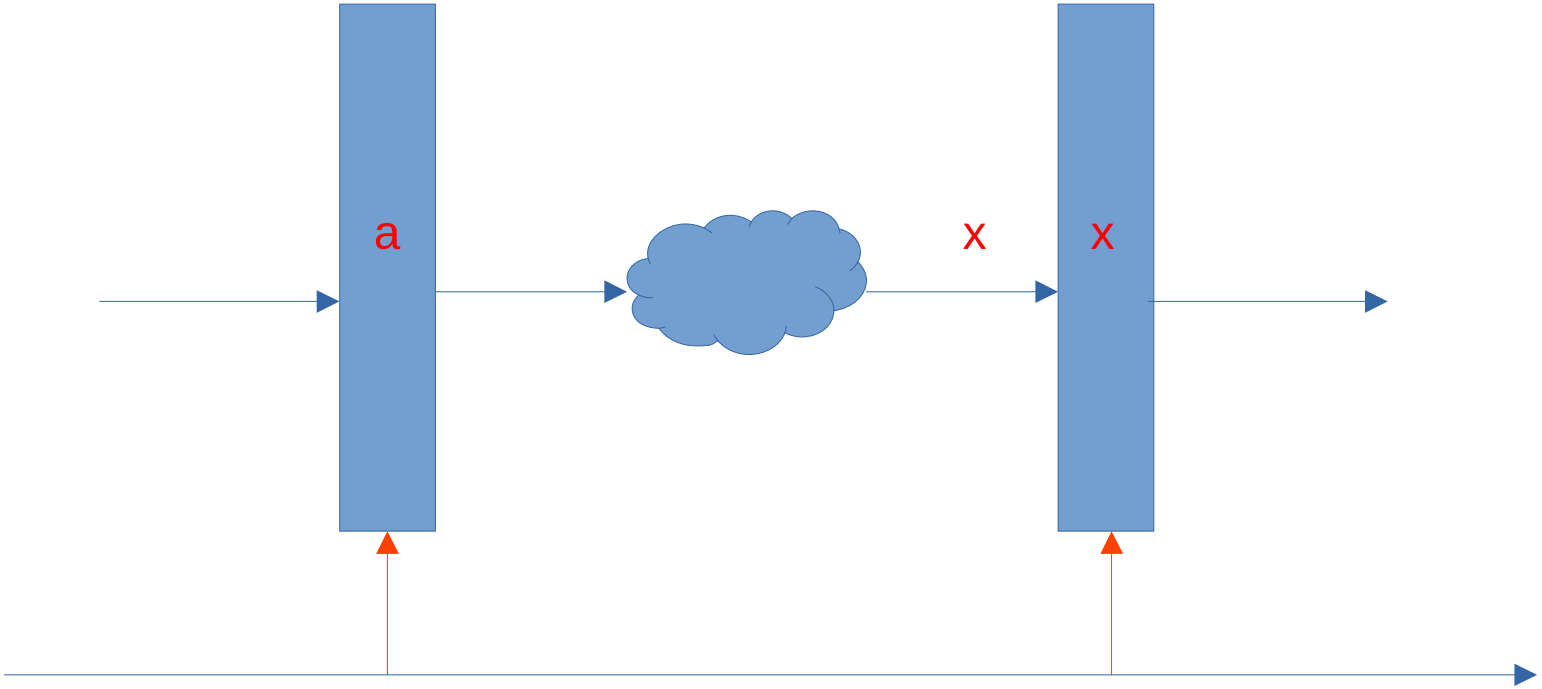
Timing



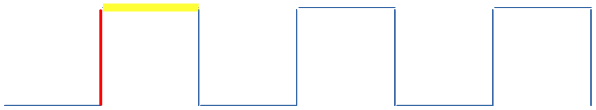


Timing

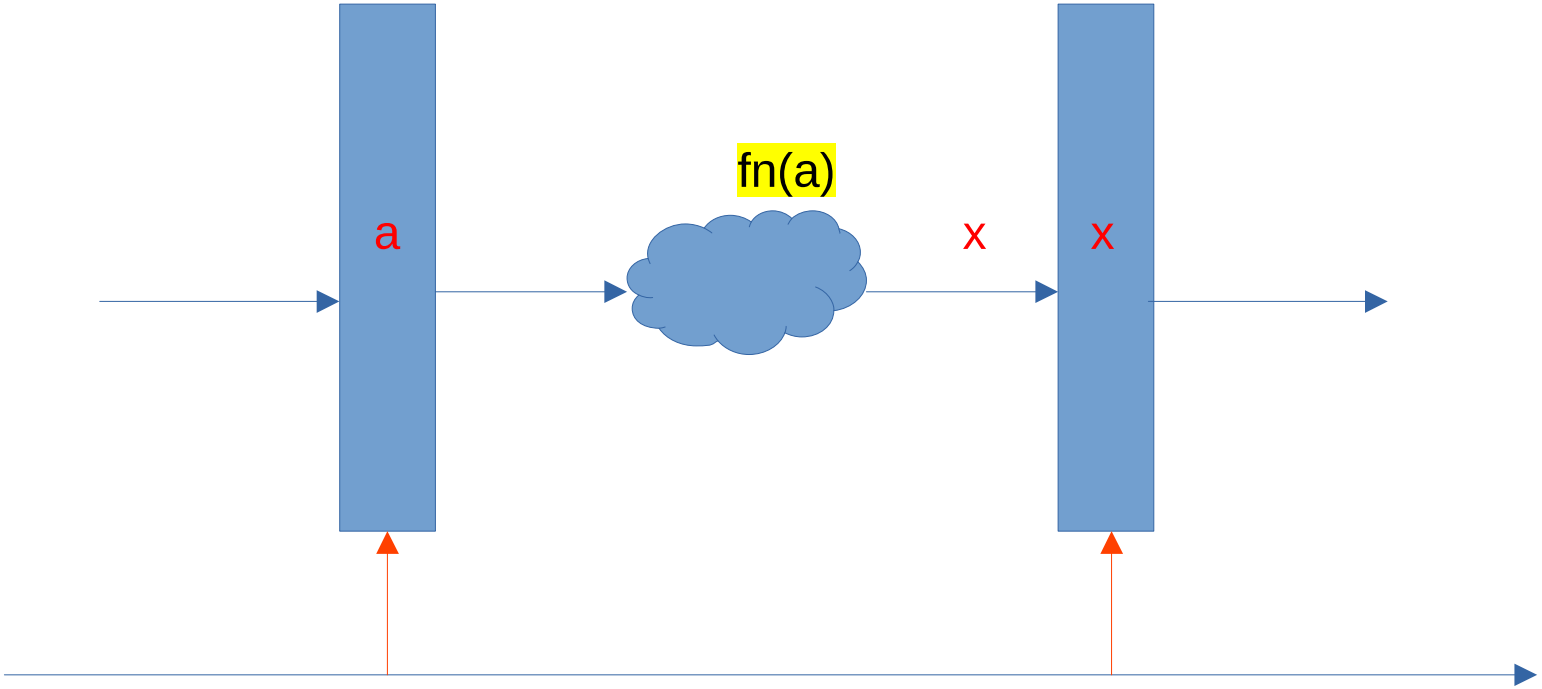




Timing

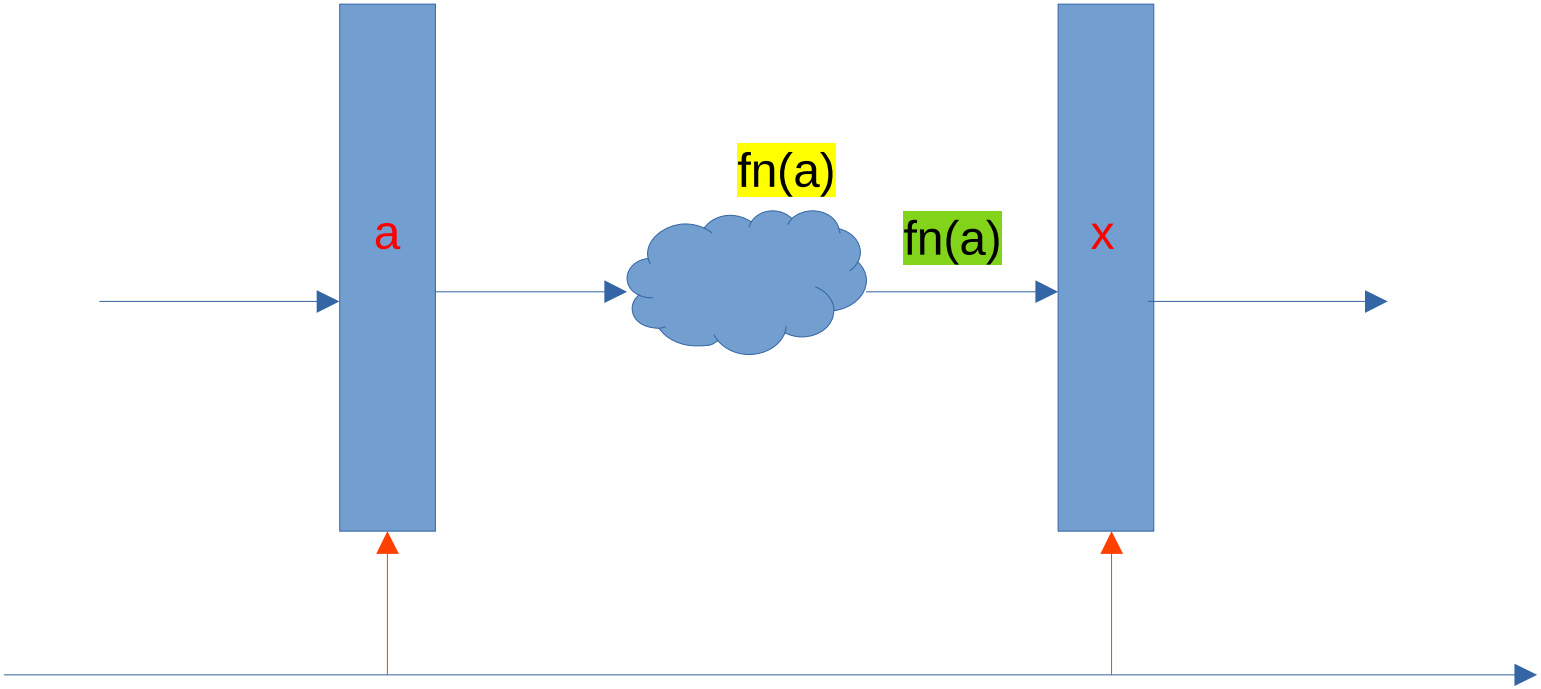


Asynchronous read



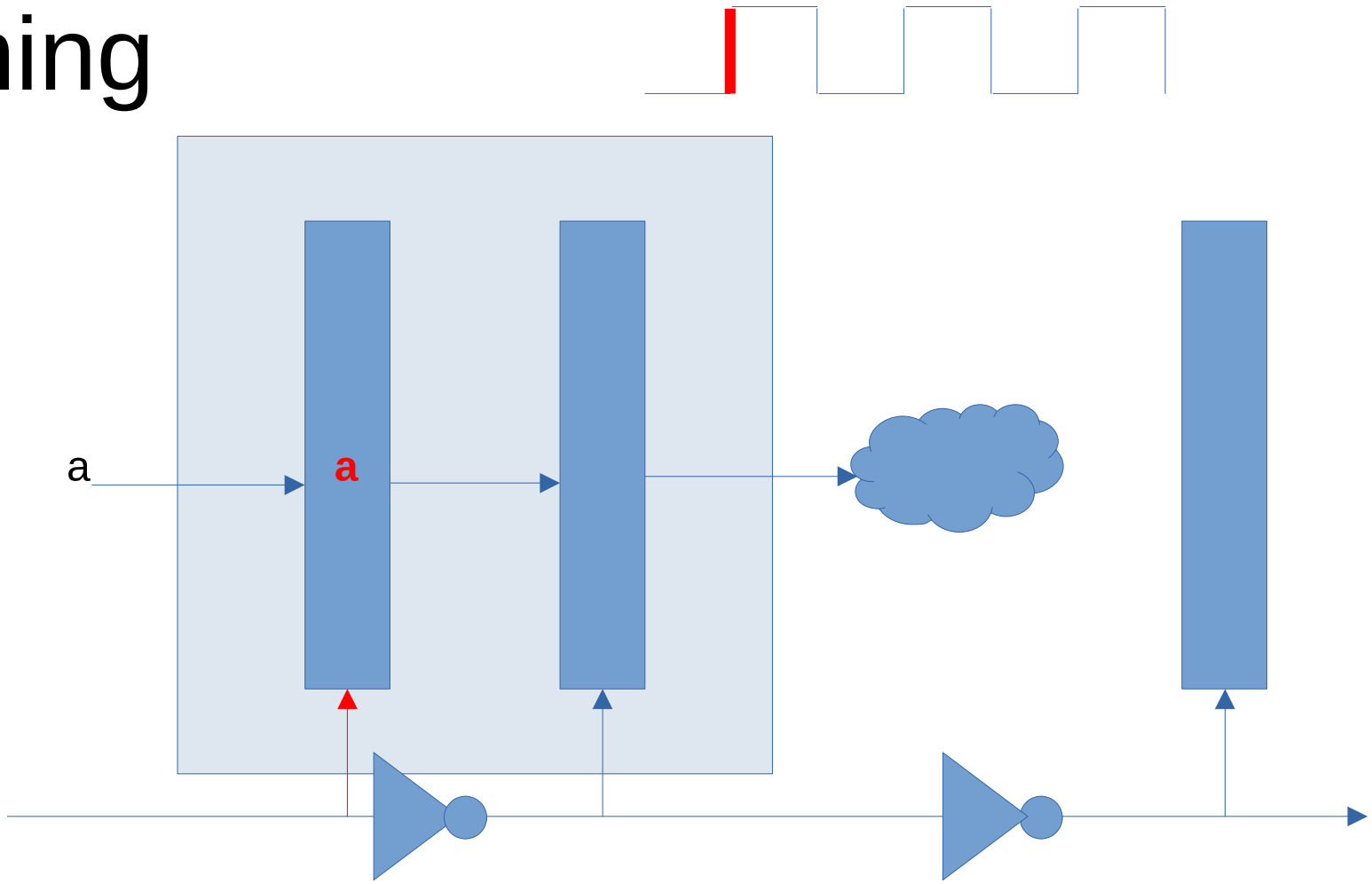
Timing

Asynchronous read

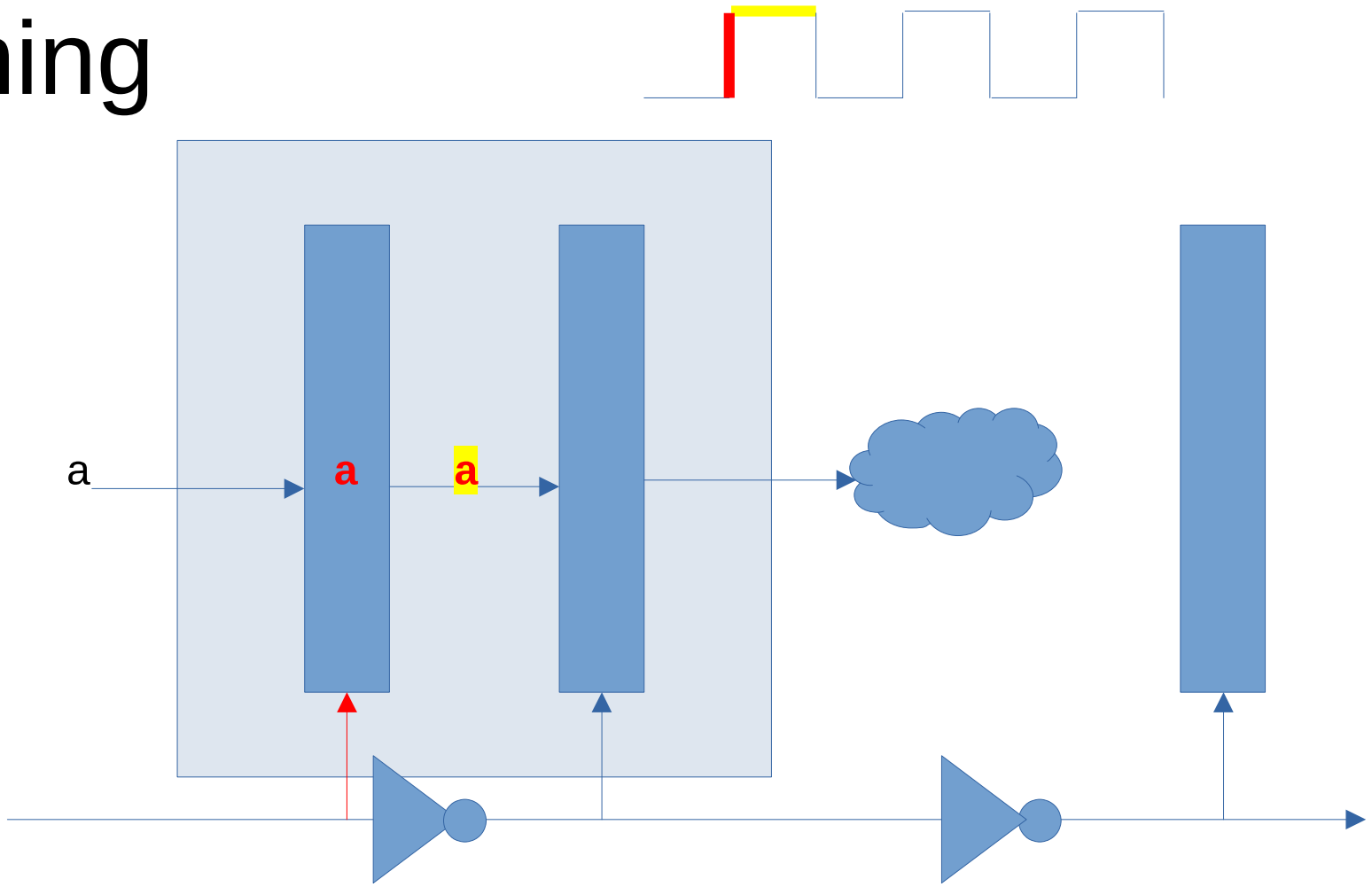


Synchronous Read

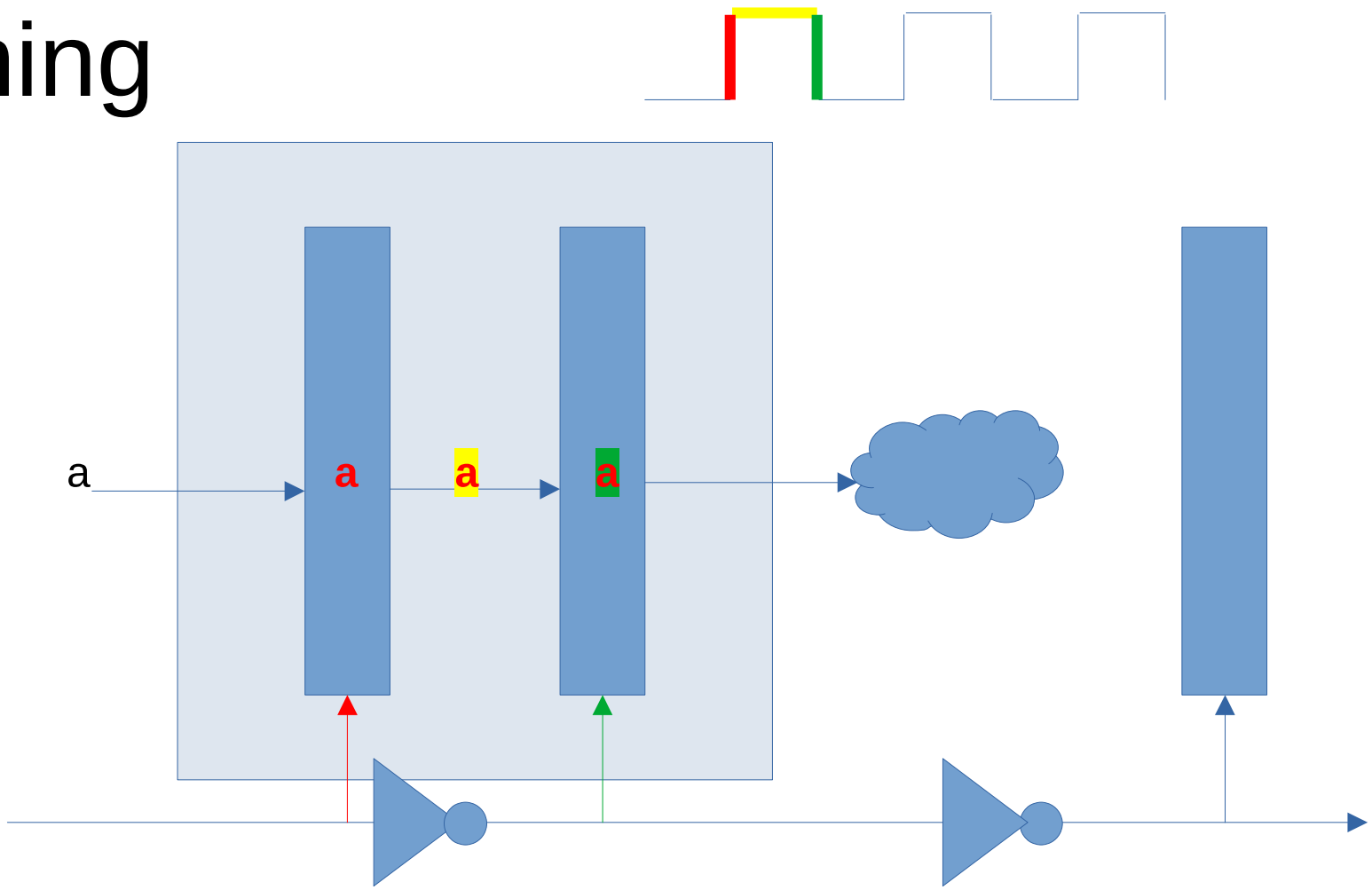
Timing



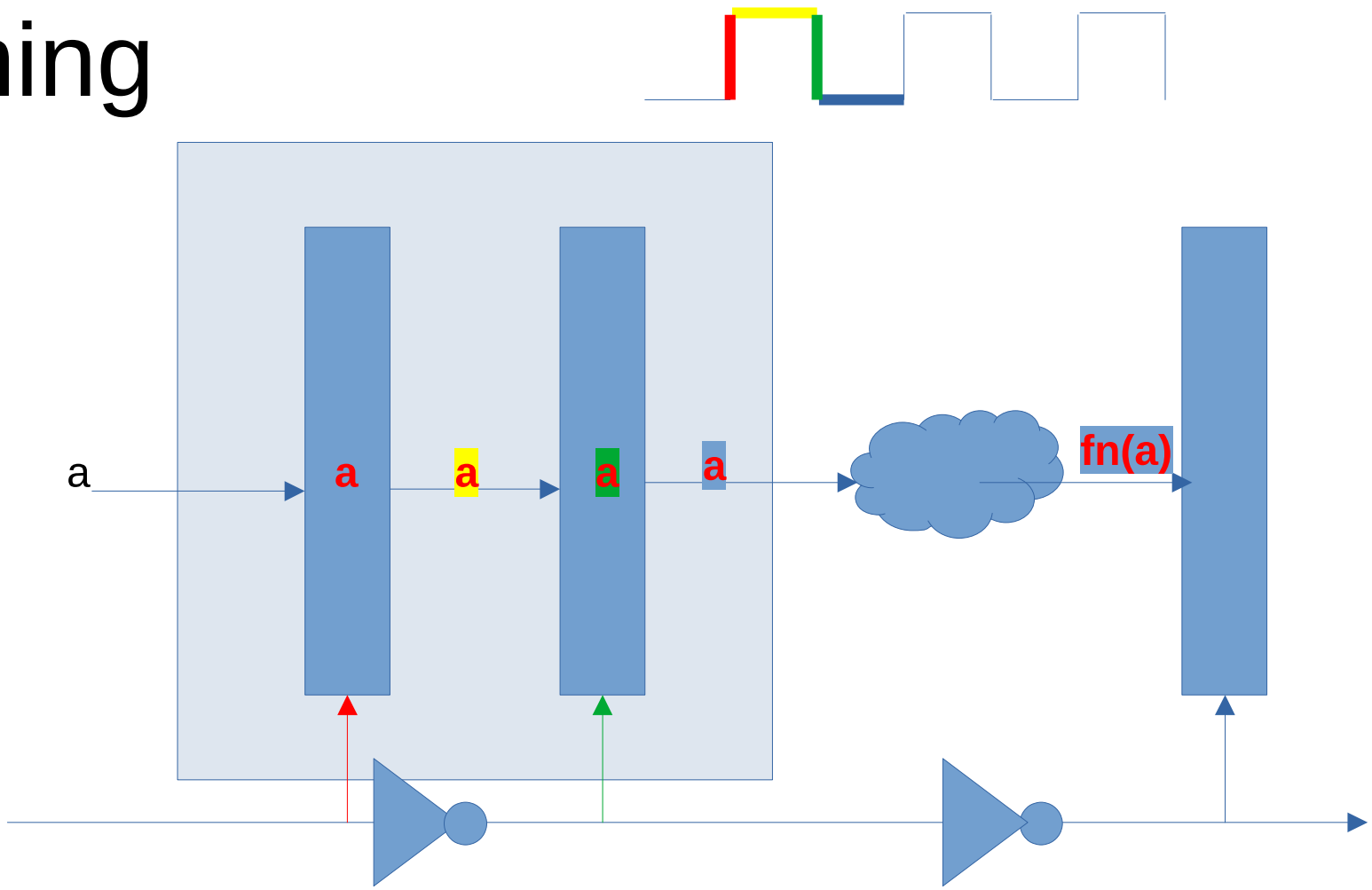
Timing



Timing



Timing



Memory

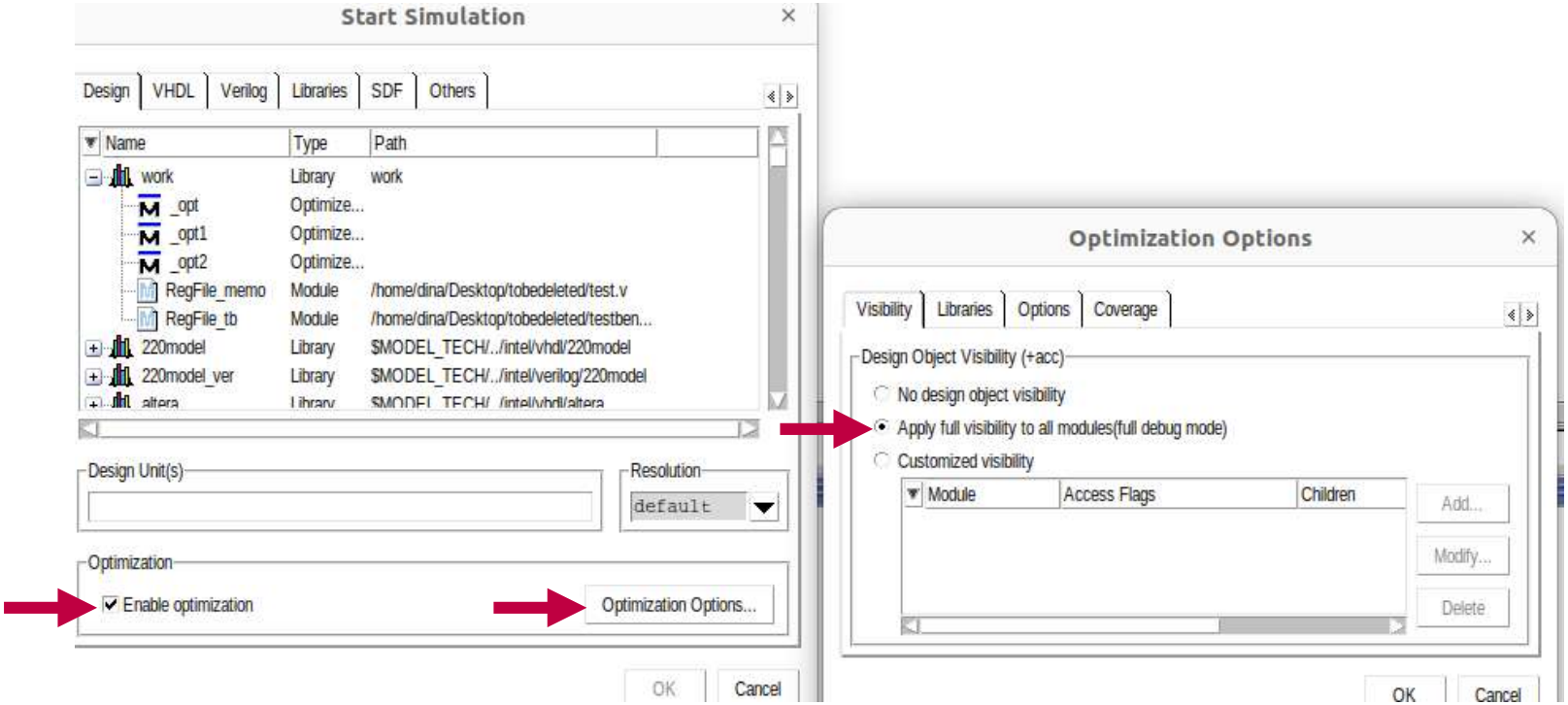
Memory

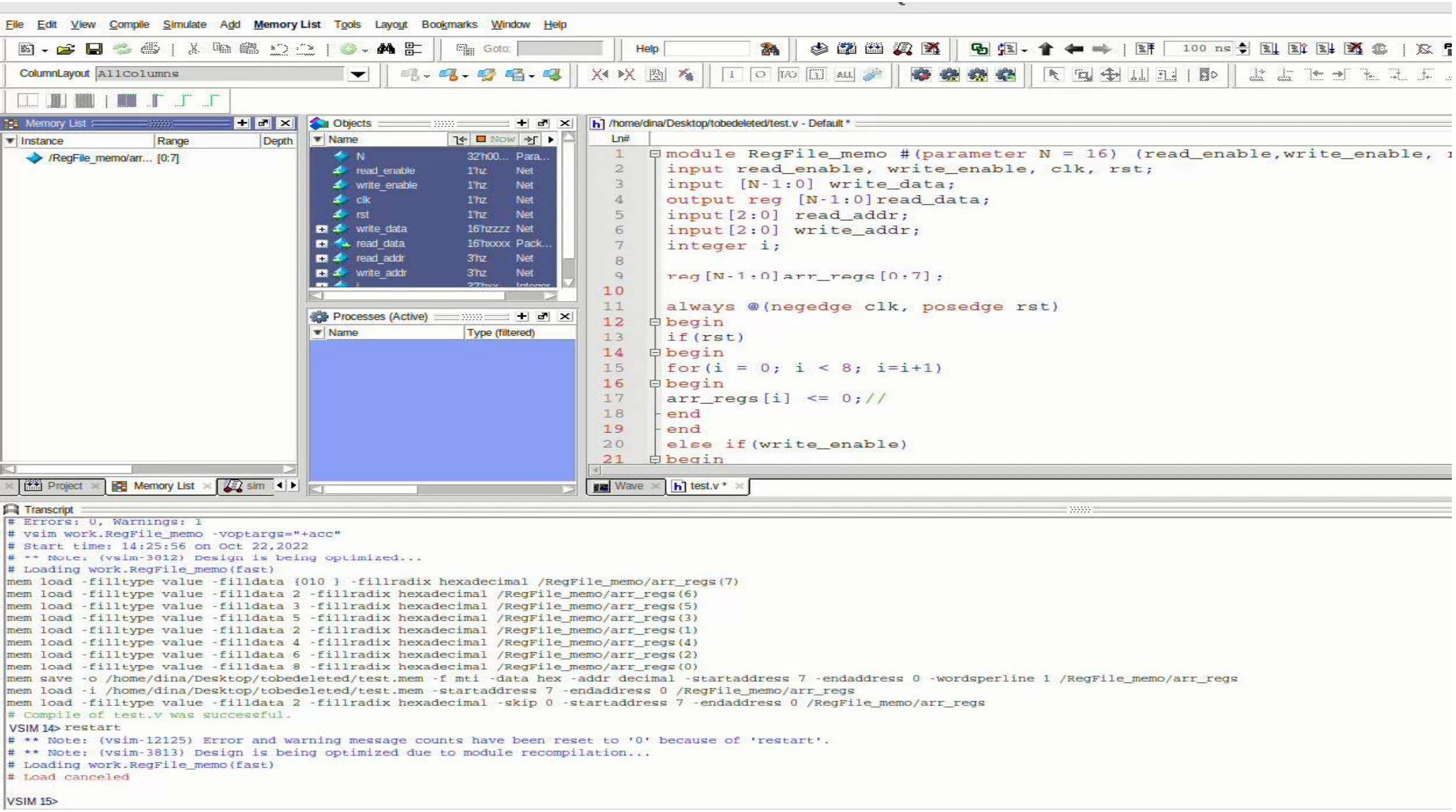
- Add the following option while running

```
vsim <modulename> -voptargs=+acc

#load from file
mem load -i <test.mem> -startaddress 7 -endaddress 0 </moduleName/memName>

#load a data pattern
mem load -filltype value -filldata 2 -fillradix hexadecimal -skip 0 -startaddress 7 -
endaddress 0 /RegFile_memo/arr_regS
```

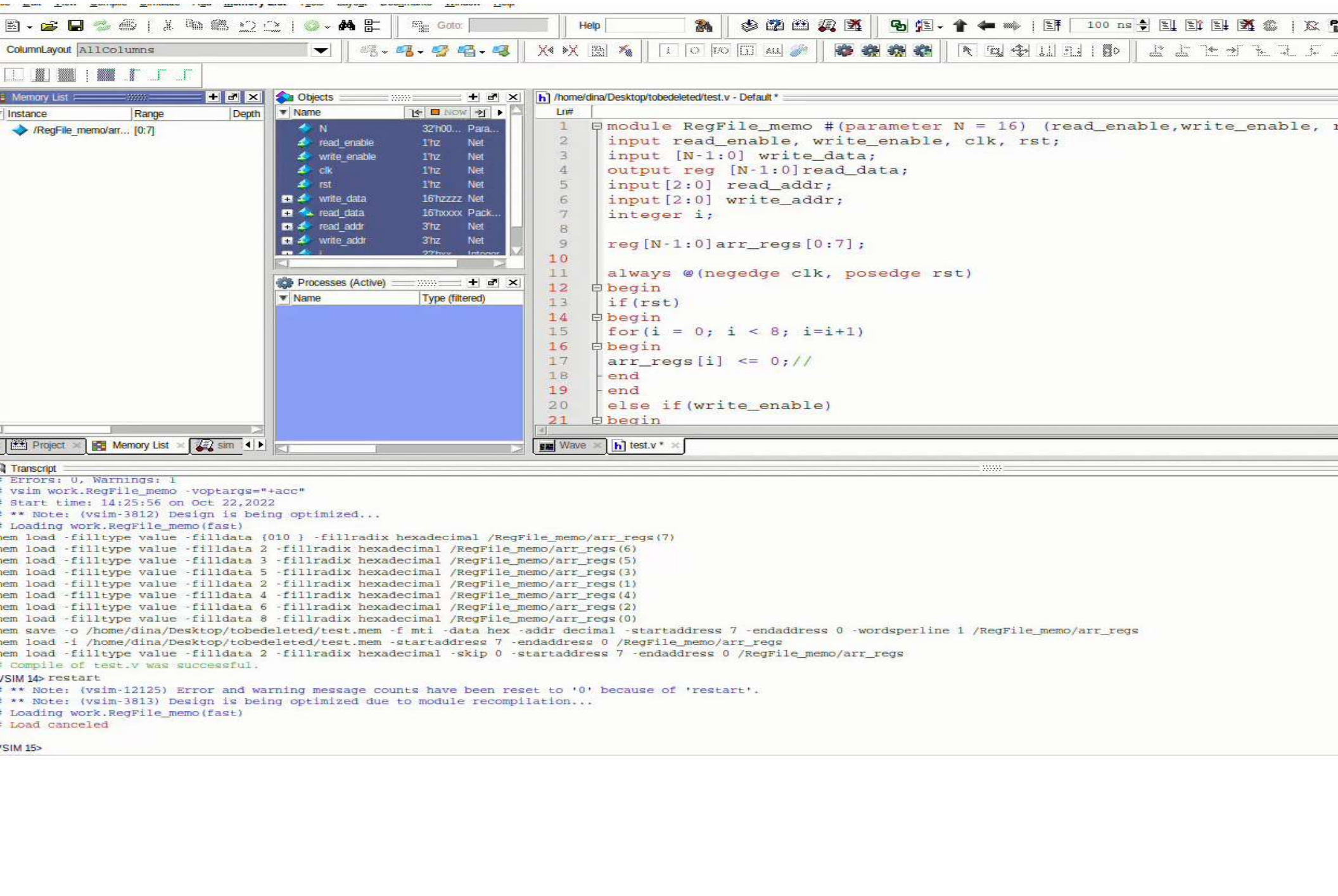
Memory

- Or From UI




File Edit View Compile Simulate Add Memory List Tools Layout Bookmarks Window Help
Memory List
Instance Range Depth
/RegFile_memo/arr... [0:7]
Objects
Name
N 32'h00... Para...
read_enable 1'hz Net
write_enable 1'hz Net
clk 1'hz Net
rst 1'hz Net
write_data 16'hzzzz Net
read_data 16'hxxxx Pack...
read_addr 3'hz Net
write_addr 3'hz Net
Processes (Active)
Name Type (filtered)
/home/dina/Desktop/tobedeleted/test.v - Default *
Ln#
1 module RegFile_memo #(parameter N = 16) (read_enable,write_enable,
2 input read_enable, write_enable, clk, rst;
3 input [N-1:0] write_data;
4 output reg [N-1:0]read_data;
5 input[2:0] read_addr;
6 input[2:0] write_addr;
7 integer i;
8
9 reg[N-1:0]arr_regs[0:7];
10
11 always @(negedge clk, posedge rst)
12 begin
13 if(rst)
14 begin
15 for(i = 0; i < 8; i=i+1)
16 begin
17 arr_regs[i] <= 0;//
18 end
19 end
20 else if(write_enable)
21 begin
Project
Memory List
sim
Wave
test.v *
Transcript
Errors: 0, Warnings: 1
vsim work.RegFile_memo -voptargs="+acc"
Start time: 14:25:56 on Oct 22,2022
** Note: (vsim-3812) Design is being optimized...
Loading work.RegFile_memo(fast)
mem load -filltype value -filldata {010 } -fillradix hexadecimal /RegFile_memo/arr_regs(7)
mem load -filltype value -filldata 2 -fillradix hexadecimal /RegFile_memo/arr_regs(6)
mem load -filltype value -filldata 3 -fillradix hexadecimal /RegFile_memo/arr_regs(5)
mem load -filltype value -filldata 5 -fillradix hexadecimal /RegFile_memo/arr_regs(3)
mem load -filltype value -filldata 2 -fillradix hexadecimal /RegFile_memo/arr_regs(1)
mem load -filltype value -filldata 4 -fillradix hexadecimal /RegFile_memo/arr_regs(4)
mem load -filltype value -filldata 6 -fillradix hexadecimal /RegFile_memo/arr_regs(2)
mem load -filltype value -filldata 8 -fillradix hexadecimal /RegFile_memo/arr_regs(0)
mem save -o /home/dina/Desktop/tobedeleted/test.mem -f mti -data hex -addr decimal -startaddress 7 -endaddress 0 -wordsperline 1 /RegFile_memo/arr_regs
mem load -i /home/dina/Desktop/tobedeleted/test.mem -startaddress 7 -endaddress 0 /RegFile_memo/arr_regs
mem load -filltype value -filldata 2 -fillradix hexadecimal -skip 0 -startaddress 7 -endaddress 0 /RegFile_memo/arr_regs
Compile of test.v was successful.
VSIM 14> restart
** Note: (vsim-12125) Error and warning message counts have been reset to '0' because of 'restart'.
** Note: (vsim-3813) Design is being optimized due to module recompilation...
Loading work.RegFile_memo(fast)
Load canceled
VSIM 15>

Debug


Memory List
Instance
Range
Depth
/RegFile_memo/arr... [0:7]
Objects
Name
N 32'h00... Para...
read_enable 1'hz Net
write_enable 1'hz Net
clk 1'hz Net
rst 1'hz Net
write_data 16'hzzzz Net
read_data 16'hxxxx Pack...
read_addr 3'hz Net
write_addr 3'hz Net
Processes (Active)
Name
Type (filtered)
/home/dina/Desktop/tobedeleted/test.v - Default *
Ln#
1 module RegFile_memo #(parameter N = 16) (read_enable,write_enable,
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4 output reg [N-1:0]read_data;
5 input[2:0] read_addr;
6 input[2:0] write_addr;
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11 always @(negedge clk, posedge rst)
12 begin
13 if(rst)
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15 for(i = 0; i < 8; i=i+1)
16 begin
17 arr_regs[i] <= 0;//
18 end
19 end
20 else if(write_enable)
21 begin
Project
Memory List
sim
Wave
test.v *
Transcript
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Start time: 14:25:56 on Oct 22,2022
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Loading work.RegFile_memo(fast)
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mem load -filltype value -filldata 3 -fillradix hexadecimal /RegFile_memo/arr_regs(5)
mem load -filltype value -filldata 5 -fillradix hexadecimal /RegFile_memo/arr_regs(3)
mem load -filltype value -filldata 2 -fillradix hexadecimal /RegFile_memo/arr_regs(1)
mem load -filltype value -filldata 4 -fillradix hexadecimal /RegFile_memo/arr_regs(4)
mem load -filltype value -filldata 6 -fillradix hexadecimal /RegFile_memo/arr_regs(2)
mem load -filltype value -filldata 8 -fillradix hexadecimal /RegFile_memo/arr_regs(0)
mem save -o /home/dina/Desktop/tobedeleted/test.mem -f mti -data hex -addr decimal -startaddress 7 -endaddress 0 -wordsperline 1 /RegFile_memo/arr_regs
mem load -i /home/dina/Desktop/tobedeleted/test.mem -startaddress 7 -endaddress 0 /RegFile_memo/arr_regs
mem load -filltype value -filldata 2 -fillradix hexadecimal -skip 0 -startaddress 7 -endaddress 0 /RegFile_memo/arr_regs
Compile of test.v was successful.
VSIM 14> restart
** Note: (vsim-12125) Error and warning message counts have been reset to '0' because of 'restart'.
** Note: (vsim-3813) Design is being optimized due to module recompilation...
Loading work.RegFile_memo(fast)
Load canceled
VSIM 15>

Thank You