## **Assembler Guide**

Instr.	OP-Code	First Operand	Second Operand	
Memory Instructions (5)				
LDM R_dst, Imm	10010	R_dst <sub>2</sub> R_dst <sub>1</sub> R_dst <sub>0</sub>	l <sub>7</sub> l <sub>6</sub> l <sub>5</sub> l <sub>4</sub> l <sub>3</sub> l <sub>2</sub> l <sub>1</sub> l <sub>0</sub>	
LDD R_src, R_dst	10011	R_dst <sub>2</sub> R_dst <sub>1</sub> R_dst <sub>0</sub>	R_src <sub>2</sub> R_src <sub>1</sub> R_src <sub>0</sub>	
STD R_src, R_dst	10000	R_dst <sub>2</sub> R_dst <sub>1</sub> R_dst <sub>0</sub>	R_src <sub>2</sub> R_src <sub>1</sub> R_src <sub>0</sub>	
PUSH R_dst	10100	R_dst <sub>2</sub> R_dst <sub>1</sub> R_dst <sub>0</sub>	XXXXXXX	
POP R_dst	10111	R_dst <sub>2</sub> R_dst <sub>1</sub> R_dst <sub>0</sub>	XXXXXXX	
Branch Instructions (4)				
JZ R_dst	11000	R_dst <sub>2</sub> R_dst <sub>1</sub> R_dst <sub>0</sub>	XXXXXXX	
JN R_dst	11001	R_dst <sub>2</sub> R_dst <sub>1</sub> R_dst <sub>0</sub>	XXXXXXX	
JC R_dst	11010	R_dst <sub>2</sub> R_dst <sub>1</sub> R_dst <sub>0</sub>	XXXXXXX	
JMP R_dst	10011	R_dst <sub>2</sub> R_dst <sub>1</sub> R_dst <sub>0</sub>	XXXXXXXX	
ALU With Immediate (2)				
SHL R_dst	11110	R_dst <sub>2</sub> R_dst <sub>1</sub> R_dst <sub>0</sub>	l <sub>7</sub> l <sub>6</sub> l <sub>5</sub> l <sub>4</sub> l <sub>3</sub> l <sub>2</sub> l <sub>1</sub> l <sub>0</sub>	
SHR R_dst	11111	R_dst <sub>2</sub> R_dst <sub>1</sub> R_dst <sub>0</sub>	l <sub>7</sub> l <sub>6</sub> l <sub>5</sub> l <sub>4</sub> l <sub>3</sub> l <sub>2</sub> l <sub>1</sub> l <sub>0</sub>	
Port Instructions (2)				
IN R_dst	11100	R_dst <sub>2</sub> R_dst <sub>1</sub> R_dst <sub>0</sub>	XXXXXXX	
OUT R_dst	11101	R_dst <sub>2</sub> R_dst <sub>1</sub> R_dst <sub>0</sub>	xxxxxxx	

Special Instructions (6)					
NOP	00000	xxxxxxx	XXXXXXXX		
SETC	00111	XXXXXXXX	XXXXXXXX		
CLRC	00110	XXXXXXXX	XXXXXXX		
CALL R_dst	00101	R_dst <sub>2</sub> R_dst <sub>1</sub> R_dst <sub>0</sub>	XXXXXXXX		
RET	00010	XXXXXXX	xxxxxxx		
RTI	00011	XXXXXXX	XXXXXXXX		
		ALU (8)			
NOT R_dst	01001	R_dst <sub>2</sub> R_dst <sub>1</sub> R_dst <sub>0</sub>	XXXXXXXX		
ADD R_src, R_dst	01010	R_dst <sub>2</sub> R_dst <sub>1</sub> R_dst <sub>0</sub>	R_src <sub>2</sub> R_src <sub>1</sub> R_src <sub>0</sub>		
SUB R_src, R_dst	01011	R_dst <sub>2</sub> R_dst <sub>1</sub> R_dst <sub>0</sub>	R_src <sub>2</sub> R_src <sub>1</sub> R_src <sub>0</sub>		
AND R_src, R_dst	01100	R_dst <sub>2</sub> R_dst <sub>1</sub> R_dst <sub>0</sub>	R_src <sub>2</sub> R_src <sub>1</sub> R_src <sub>0</sub>		
OR R_src, R_dst	01101	R_dst <sub>2</sub> R_dst <sub>1</sub> R_dst <sub>0</sub>	R_src <sub>2</sub> R_src <sub>1</sub> R_src <sub>0</sub>		
INC R_dst	01110	R_dst <sub>2</sub> R_dst <sub>1</sub> R_dst <sub>0</sub>	XXXXXXXX		
DEC R_dst	01111	R_dst <sub>2</sub> R_dst <sub>1</sub> R_dst <sub>0</sub>	XXXXXXXX		
MOV R_src, R_dst	01000	R_dst <sub>2</sub> R_dst <sub>1</sub> R_dst <sub>0</sub>	R_src <sub>2</sub> R_src <sub>1</sub> R_src <sub>0</sub>		