Mitchell Arndt

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View Online Portfolio: https://marndt26.github.io/

OBJECTIVE

Actively seeking full-time position in microprocessor and distributed memory system architecture

EDUCATION

Purdue University | West Lafayette, IN **August 2021 – Present**
Master of Science in Computer Architecture GPA: 3.92

Purdue University | West Lafayette, IN **August 2018 – December 2021**
Bachelor of Science in Electrical Engineering – Honors College
Computer Science Minor
Certificate of Entrepreneurship and Innovation GPA: 3.96

EXPERIENCE

Purdue SoCET | West Lafayette, IN **January 2022 – Present**
Design/UVM Engineer
- Collaborated with vertically integrated team to design L1/L2 cache hierarchy for RISCV processor to improve memory latency by 400%
- Generated UVM testbench with constrained random input to verify cache correctness before fabrication

Card Connect Paradise| Phoenix, AZ **May 2019 – Present**
Software Consultant
- Invented online payment platform to ameliorate the giving process for charitable organization donors and admin
- Worked with CEO to automate business management tasks like payroll and lead acquisition, increasing productivity

Microchip Technology Inc. | Chandler, AZ **May 2022 – August 2022**
Digital Design & Verification Intern
- Designed/Synthesized SMI Controller for flexible high-speed data comm which enabled legacy device compatibility
- Architected UVM environment to validate SMI design, improving coverage over previous directed testing method

Autonomous Motorsports Purdue | West Lafayette, IN **May 2019 – May 2022**
Electrical Lead Engineer
- Led team members to integrate drive control systems for self-driving race car by generating embedded C firmware to interpret serial commands and output PWM, analog, and digital drive control signals for high-speed navigation
- Created custom PCB using KiCad to route control signals from microcontroller to electrical subsystems

Northrop Grumman | Chandler, AZ **June 2021 – August 2021**
Electrical Engineering Intern in Launch Vehicles Division
- Developed graphical RSS Error Budget Analysis Tool for analog avionics sensors with Python and JavaScript to automate required preflight analyses to eliminate the need for future engineering effort and cut project costs

Purdue Neurotrauma Group | West Lafayette, IN **December 2019 – December 2021**
Research Assistant
- Lead hardware/firmware design efforts for interdisciplinary team to prototype device small enough to fit in football helmet to precisely measure forces involved in football tackling for real-time analysis of a player's neurological safety
- Presented force collection device at Purdue Undergraduate Research Expo, receiving top scores from judging panel

TECHNICAL SKILLS

Programming Languages: System Verilog, C, C++, Python, Full Stack JavaScript, Java, JavaFX, MATLAB

Software Tools: Mentor Questa, Design Compiler, Xcelium, Verdi, Git/GitHub, KiCad, ANTLR, LTspice

LEADERSHIP & PHILANTHROPY

Tau Beta Pi Engineering Honor Society **January 2020 – Present**

Engineering Honors Peer Mentor **August 2019 – August 2020**