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EXPERIMENT 5. INTRODUCTION TO VERILOG

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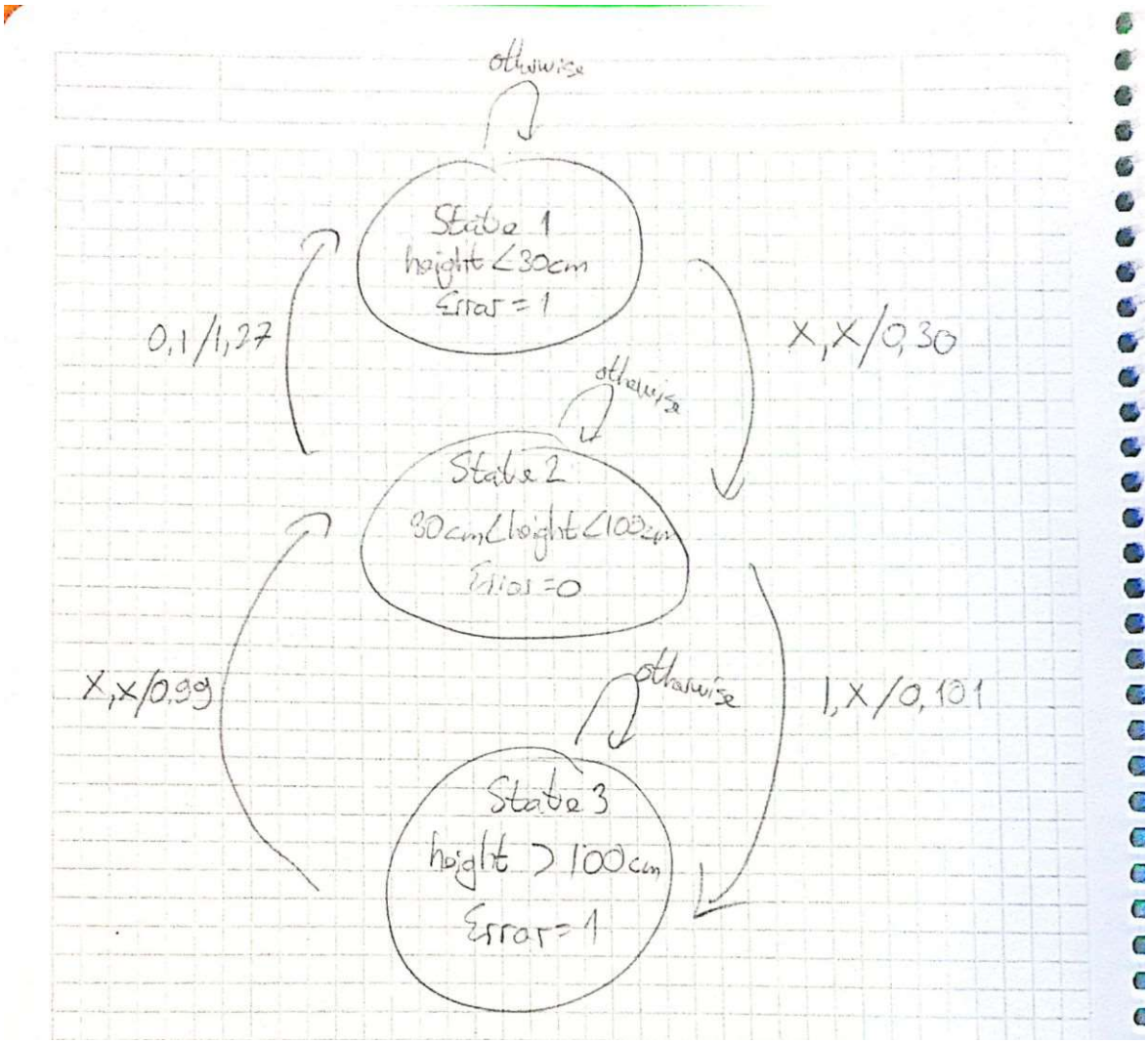
Design Question # : 3

Important Notes:

- You will be expected to provide screenshots of simulation results. You have to take full screenshots for all of them. You can use the full-screen mode of the Snipping Tool for this. **DO NOT crop** any image.
- If the image is too dense or too small that makes it difficult to view, then add zoomed-in images as EXTRAS (again full screenshots).
- You will name your report as "**Exp#_ DesignQuestion#_StudentID.pdf**
- You may make comments if any discrepancy occurs between your results and your expectations. You can write your expectations, possible reasons of that discrepancy, etc. below related section. **In addition to this report, DO NOT FORGET to upload your project files.**

1) Draw the state diagram of your module using paint or powerpoint.


otherwise
State 1
height < 30cm
Error = 1
0,1/1,27
X,X/0,30
otherwise
State 2
30cm < height < 100cm
Error = 0
X,X/0,99
otherwise
1,X/0,101
State 3
height > 100cm
Error = 1

2) Put your Verilog code of the module you have designed.

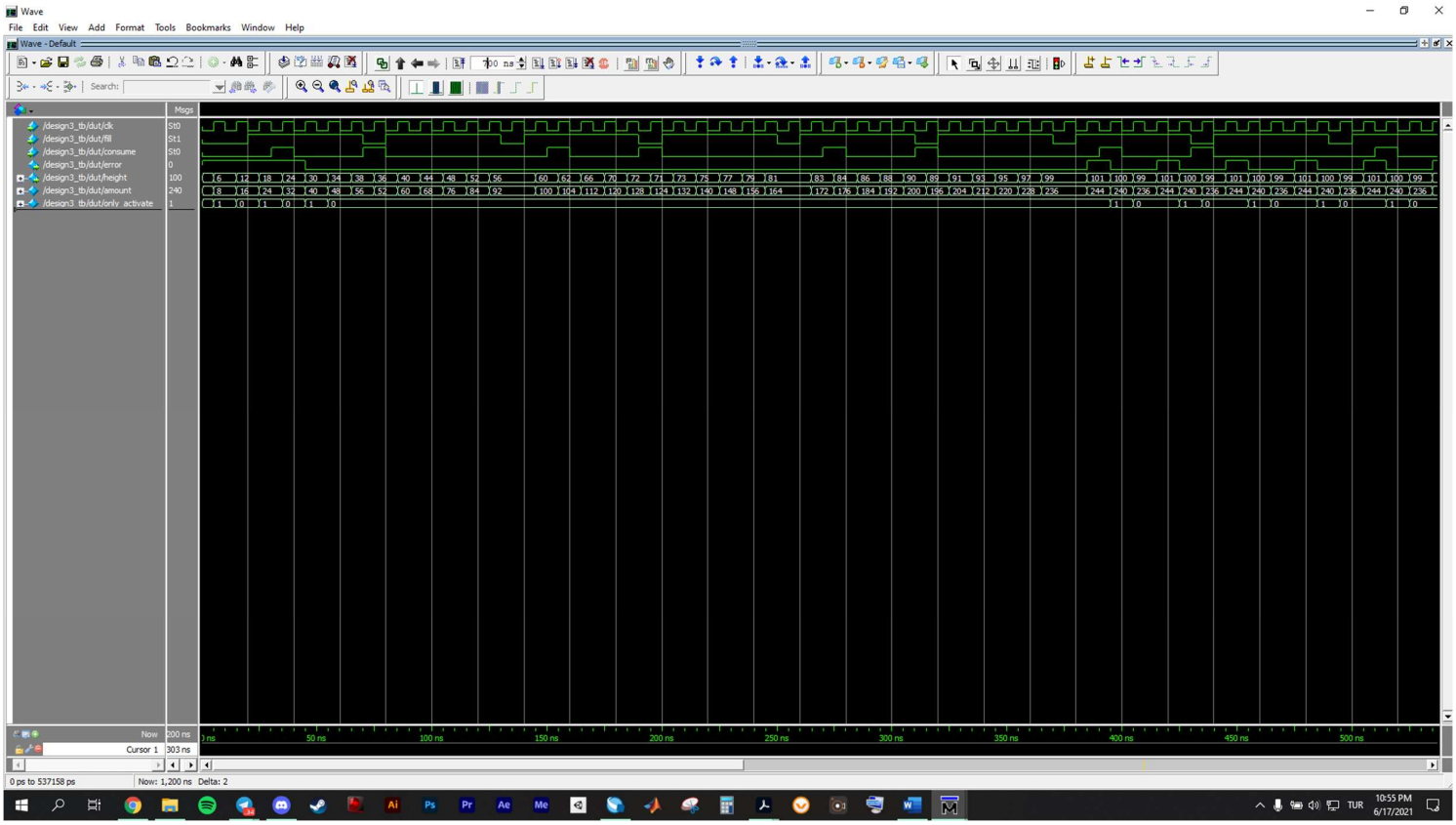
```
module design3(clk, fill, consume, error, height);
input clk, fill, consume ;
output reg error;
output reg [7:0] height;
integer amount=0, only_activate=0;

initial begin
error=1;
height=3'd000;
end

always @(posedge clk)begin

if(only_activate==0)begin

 if(amount<40)begin
 error=1;
 only_activate=1;
 amount = amount + 8;
 end

 else if(amount<=240 && amount>=40)begin
 error = 0;
 amount = amount + 8*fill - 4*consume;
 only_activate = 0;
 end

 else if(amount>240)begin
 error = 1;
 amount = amount - 4;
 only_activate = 1;
 end

 if(amount<=40) begin
 height = (amount/4)*3;
 end
 else if(amount<120 && amount>40) begin
 height = 30 + ((amount-40)/2);
 end
 else if(amount<248 && amount>=120)begin
 height = 30 + 40 + ((amount-120)/4);
  end
 end

.
.
.
.
```

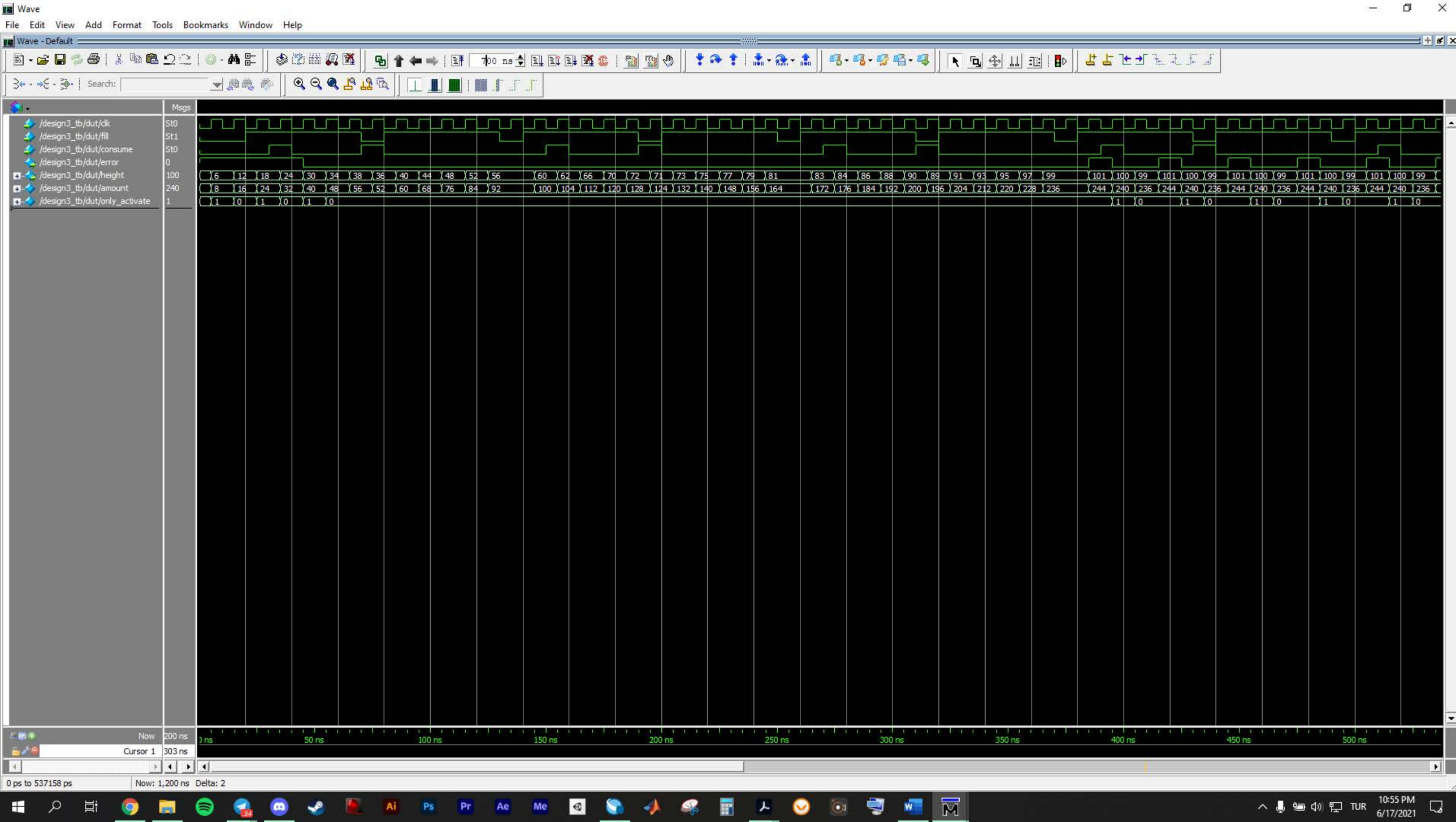
```
.
.
.

else if(only_activate==1)begin

 if(amount<=40)begin
  if(amount>=40)begin
  error=0;
  end
 amount = amount + 8;
 only_activate = 0;
 end

 else if(amount>=240)begin
  if(amount<=240)begin
  error=0;
  end
 amount = amount - 4;
 only_activate = 0;
 end


 if(amount<=40) begin
 height = (amount/4)*3;
 end
 else if(amount<120 && amount>40) begin
 height = 30 + ((amount-40)/2);
 end
 else if(amount<248 && amount>=120)begin
 height = 30 + 40 + ((amount-120)/4);
  end

 end
if(height<30||height>100)begin
 error=1;
 end
 else begin
 error=0;
 end
end

endmodule
```

3) Put your Testbench code of the module you have designed.

```
`timescale 1 ns / 1 ps

module design3_tb();

reg clk, fill, consume;
wire error;
wire [7:0] height;

design3 dut (.clk(clk), .fill(fill), .consume(consume),
.error(error),.height(height));

initial begin
  clk = 0;
  fill = 0;
  consume = 0;
end
// Clock setup
always begin
  clk <= 0; #5 ;  clk <= 1; #5 ;
end
always begin
  #10;
  fill <= 0;
  consume <= 0;
  #10;
  fill <=1;
  consume <=0;
  #10;
  fill <=1;
  consume <=1;
  #10
  fill <=1;
  consume <=0;
  #10
  fill <=1;
  consume <=0;
  #10
  fill <=1;
  consume <=0;
  #10
  fill <= 0;
  consume <= 1;
  #10
  fill <=1;
  consume <=0;
  #10
  fill <=1;
  consume <=0;
  #10;

end

endmodule
```

4) Put the simulation results of the module you have designed.




Wave
File Edit View Add Format Tools Bookmarks Window Help
Wave - Default
Search:
Msgs
/design3_tb/dut/clk St0
/design3_tb/dut/fill St1
/design3_tb/dut/consume St0
/design3_tb/dut/error 0
/design3_tb/dut/height 100
/design3_tb/dut/amount 240
/design3_tb/dut/only_activate 1
Now 200 ns
Cursor 1 303 ns
50 ns 100 ns 150 ns 200 ns 250 ns 300 ns 350 ns 400 ns 450 ns 500 ns
0 ps to 537158 ps
Now: 1,200 ns Delta: 2
TUR
10:55 PM
6/17/2021