# SAM D5x/E5x

# SAM D5x/E5x Family Silicon Errata and Data Sheet Clarification

## SAM D5x/E5x Family Errata

The SAM D5x/E5x family of devices that you have received conform functionally to the current device data sheet (DS60001507), except for the anomalies described in this document.

The silicon issues discussed in the following pages are for silicon revisions with the device and revision IDs listed in Table 1. SAM D5x/E5x Family Silicon Device Identification. The silicon issues are summarized in the Table of Contents following this section.

The errata described in this document will be addressed in future revisions of the SAM D5x/E5x family silicon.

**Note:**  This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current.

Data Sheet clarifications and corrections (if applicable) are located in the section Data Sheet Clarifications, following the discussion of silicon issues.

**Table 1. SAM D5x/E5x Family Silicon Device Identification**

| Part Number | Device Identification (DID[31:0]) | Revision ID (DID.REVISION[3:0]) | | |
|---|---|---|---|---|
| | | A | D | F |
| ATSAME54P19A | 0x61840x01 | 0x0 | 0x3 | 0x5 |
| ATSAME54P20A | 0x61840x00 | | | |
| ATSAME54N19A | 0x61840x03 | | | |
| ATSAME54N20A | 0x61840x02 | | | |
| ATSAME53N20A | 0x61830x02 | | | |
| ATSAME53N19A | 0x61830x03 | | | |
| ATSAME53J18A | 0x61830x06 | | | |
| ATSAME53J19A | 0x61830x05 | | | |
| ATSAME53J20A | 0x61830x04 | | | |
| ATSAME51N19A | 0x61810x01 | | | |
| ATSAME51N20A | 0x61810x00 | | | |
| ATSAME51J18A | 0x61810x03 | | | |
| ATSAME51J19A | 0x61810x02 | | | |
| ATSAME51J20A | 0x61810x04 | | | |
| ATSAMD51P20A | 0x60060x00 | | | |
| ATSAMD51P19A | 0x60060x01 | | | |
| ATSAMD51N19A | 0x60060x03 | | | |
| ATSAMD51N20A | 0x60060x02 | | | |
| ATSAMD51J18A | 0x60060x06 | | | |
| ATSAMD51J19A | 0x60060x05 | | | |
| ATSAMD51J20A | 0x60060x04 | | | |
| ATSAMD51G18A | 0x60060x08 | | | |
| ATSAMD51G19A | 0x60060x07 | | | |
| ATSAME51G18A | 0x61810306 | N/A | 0x3 | 0x5 |
| ATSAME51G19A | 0x61810305 | | | |

**Note:** Refer to the **Device Service Unit** chapter in the current device data sheet (DS60001507) for a detailed information on Device Identification and Revision IDs for your specific device.

# Table of Contents

# 1. Silicon Errata Summary

**Table 1-1. Errata Summary**

| Module | Feature | Item Number | Issue Summary | A | D | F |
|---|---|---|---|---|---|---|
| Analog -to-Digital Converter(ADC) | ADC SYNCBUSY.SWTRIG | 2.1.1 | The ADC SYNCBUSY.SWTRIG gets stuck to '1' after wake-up from Standby Sleep mode. | X | X | X |
| Analog -to-Digital Converter(ADC) | ADC TUE/INL/DNL | 2.1.2 | The ADC TUE/INL/DNL performance is not guaranteed in the following scenarios: <br> • Sampling frequency is above 500 ksps <br> • ADC VREF is different from VDDANA | X | | |
| Analog -to-Digital Converter(ADC) | Reference Buffer Offset Compensation | 2.1.3 | ADC converted data could be erroneous when using the Reference Buffer (REFCTRL.REFSEL = INTREF, INTVCC0, VREFA or VREB) and when Reference Buffer Offset Compensation is enabled (REFCTRL.REFCOMP = 1). | X | X | X |
| Analog -to-Digital Converter(ADC) | DMA Sequencing | 2.1.4 | ADC DMA Sequencing with prescaler>8 (ADC->CTRLA.bit.PRESCALER>2), does not produce the expected channel sequence. | X | X | X |
| Analog -to-Digital Converter(ADC) | DMA Sequencing | 2.1.5 | ADC DMA Sequencing with averaging enabled (AVGCTRL.SAMPLENUM>1) without AVGCTRL bit set (DSEQCTRL.AVGCTRL= 0) in the update sequence does not produce the expected channel sequence. | X | X | X |
| Analog -to-Digital Converter(ADC) | Internal Bandgap Reference | 2.1.6 | If the internal bandgap voltage reference is selected, ADC conversions may never complete. | X | X | X |
| Analog Comparator (AC) | AC Hysteresis | 2.2.1 | Enabling Hysteresis (COMPCTRLn.HYSTEN = 0x1) changes the threshold voltage (VTH-), which could result in unexpected behavior of the Analog Comparator. | X | X | |
| Analog Comparator (AC) | Output | 2.2.2 | In continuous mode the Comparator output may toggle during startup time before the Ready Status bit is set (STATUSB.READY = 1). | X | X | X |
| Analog Comparator (AC) | Standby Sleep Mode | 2.2.3 | A comparison in single shot mode will not be completed when entering in Standby Sleep mode with RUNSTDBY = 0. | X | X | X |
| Analog Comparator (AC) | Debug Mode | 2.2.4 | Continuous comparisons cannot be halted in Debug mode. | X | X | X |
| Configurable Custom Logic (CCL) | Enable Protected Registers | 2.3.1 | The SEQCTRLx and LUCTRLx registers are enable-protected by the CTRL.ENABLE bit, whereas they should be enable-protected by the LUTCTRLx.ENABLE bits. | X | X | X |
| Configurable Custom Logic (CCL) | Sequential Logic | 2.3.2 | LUT output is corrupted after enabling CCL when sequential logic is used. | X | X | X |
| Controller Area Network (CAN) | CAN Edge Filtering | 2.4.1 | When edge filtering is activated (CCCR.EFBI = 1) and when the end of the integration phase coincides with a falling edge at the Rx input pin, it may occur that the CAN synchronizes itself incorrectly and does not correctly receive the first bit of the frame. In this case, the CRC will detect the first bit that was received incorrectly, it will rate the received FD frame as faulty, and an error frame will be send. | X | X | X |
| Controller Area Network (CAN) | Dominant Bit of Intermission | 2.4.2 | When NBTP.NTSEG2 is configured to zero (Phase_Seg2(N) = 1), and when there is a pending transmission request, a dominant third bit of Intermission may cause the CAN to wrongly transmit the first identifier bit dominant instead of recessive, even if this bit was configured as '1' in the Tx Buffer Element of the CAN module. | X | X | X |
| Controller Area Network (CAN) | INTFLAG Status | 2.4.3 | Message transmitted with wrong arbitration and control fields. | X | X | X |
| Controller Area Network (CAN) | DAR Mode | 2.4.4 | Retransmission in DAR mode due to lost arbitration. | X | X | X |

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| Module | Feature | Item Number | Issue Summary | Affected Revisions | | |
|---|---|---|---|---|---|---|
| | | | | A | D | F |
| Controller Area Network (CAN) | High Priority Message (HPM) interrupt | 2.4.5 | Unexpected High Priority Message (HPM) interrupt | X | X | X |
| Controller Area Network (CAN) | TxFIFO | 2.4.6 | Tx FIFO message sequence inversion | X | X | X |
| Controller Area Network (CAN) | Debug Message | 2.4.7 | Debug message handling state machine not reset to Idle state when CCCR.INIT is set. | X | X | X |
| Controller Area Network (CAN) | Reserved | 2.4.8 | Reserved | | | |
| Controller Area Network (CAN) | On Demand | 2.4.9 | The CAN is not compatible with on-demand clock requests. | X | X | X |
| Controller Area Network (CAN) | Debug Mode | 2.4.10 | ECR.CEL, PSR.PXE, PSR.RFDF, PSR.RBRS, PSR.RESI, PSR.DLEC and PSR.LEC bits can be corrupted by a debug access. | X | X | X |
| Controller Area Network (CAN) | Debug Mode | 2.4.11 | An expected clear on read of ECR.CEL, PSR.PXE, PSR.RFDF, PSR.RBRS, PSR.RESI, PSR.DLEC and PSR.LEC bits can be unexpectedly filtered-out when the CPU is halted. | X | X | X |
| Controller Area Network (CAN) | Transmit Message Order Inversion | 2.4.12 | It may happen, depending on the delay between the individual Tx requests, that in the case where multiple Tx Buffers are configured with the same Message ID the Tx Buffers are not transmitted in order of the Tx Buffer number (lowest number first). | X | X | X |
| Controller Area Network (CAN) | Tx (Queue) Buffers | 2.4.13 | Use of multiple dedicated Tx Buffers or Tx Queue buffers configured with same Message | X | X | X |
| Controller Area Network (CAN) | Transmit Cancellation | 2.4.14 | Frame transmitted despite confirmed transmit cancellation. | X | X | X |
| Clock Failure Detector (CFD) | CFD with XOSC/XOSC32K Oscillator | 2.5.1 | When the CFD is enabled for the XOSC/XOSC32K oscillator and the oscillator input signal is stuck at 1, the clock failure detection works correctly but the switch to the safe clock will fail. | X | | |
| Clock Failure Detector (CFD) | XOSC Ready bit not cleared | 2.5.2 | When the XOSC Clock Failure Detector is enabled and a failure is detected, the XOSC Ready bit is not cleared. | X | X | X |
| Clock Failure Detector (CFD) | False Clock Failure Detection | 2.5.3 | Re-enabling the Clock Failure Detector when the XOSC is enabled can lead to a false Clock Failure Detection. | X | X | X |
| Clock Failure Detector (CFD) | False Clock Failure Detection | 2.5.4 | Re-enabling the Clock Failure Detector when the XOSC32K is enabled can lead to a false Clock Failure Detection. | X | X | X |
| Device | Reverse Current in VDDIOB Domain | 2.6.1 | For the device with 100-pin, 120-pin, and 128-pin counts, when VDDIOB is supplied with the voltage less than VDDIO - 0.7V, reverse current in VDDIOB cluster is observed. | X | | |
| Device | Internal Pull-up on the RESET Pin | 2.6.2 | The internal pull-up of the RESET pin is not functional. | X | | |
| Device | Detection of a Debugger Probe | 2.6.3 | The detection of a debugger probe could fail if the "BOD33 Disable" fuse is cleared (i.e., BOD33 is enabled). | X | X | |
| Device | VBAT Mode | 2.6.4 | VBAT mode is not functional. | X | | |
| Device | Internal Reference | 2.6.5 | When the internal reference is used with the DAC and ADC, their outputs become non-linear when the operating temperature is less than 0°C. | X | | |
| Device | Device Operation for Temperature < -20°C | 2.6.6 | If the operating temperature is less than -20°C, the device does not start. | X | X | X |
| Device | Overconsumption in Standby | 2.6.7 | An overconsumption can happen when entering in standby sleep mode when some peripherals are enabled with run in standby disabled. | X | X | X |
| Device | VDDANA Analog Cluster | 2.6.8 | Any and all I/O as well as digital alternate functions on VDDANA analog cluster must be confined as inputs only. | X | X | X |

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| Module | Feature | Item Number | Issue Summary | Affected Revisions | | |
|---|---|---|---|---|---|---|
| | | | | A | D | F |
| Device | Standby Mode | 2.6.9 | STANDBY low power mode is not supported and should not be used in new designs. | X | X | |
| Device Service Unit | CRC32 | 2.7.1 | DSU CRC32 will not complete when targeting NVM memory space while the NVM cache is disabled. | X | X | X |
| Device Service Unit | Coresight | 2.7.2 | During Coresight discovery, the TPIU and ETB ROM tables content reads as 0. Debugger may conclude that TPIU and ETB are unavailable and indicate that trace is not available. | X | X | X |
| 48 MHz Digital Frequency-Locked Loop (DFLL48M) | COARSE or FINE Calibration Values During the Locking Sequence | 2.8.1 | If the DFLL48M reaches the maximum or minimum COARSE or FINE calibration values during the locking sequence, an out of bounds interrupt will be generated. | X | X | X |
| 48 MHz Digital Frequency-Locked Loop (DFLL48M) | STATUS.DFLLRDY Bit in Close Loop Mode | 2.8.2 | In Close Loop mode, the STATUS.DFLLRDY bit does not rise before lock fine occurs. Therefore, the information about DFLL ready to start Close Loop mode is not available. | X | X | X |
| 48 MHz Digital Frequency-Locked Loop (DFLL48M) | DFLLVAL.FINE Value When DFLL48M Re-enabled | 2.8.3 | If the DFLL is disabled and then re-enabled, the DFLLVAL.FINE value is ignored by the DFLL module, which will then start its lock fine process at another frequency. | X | | |
| 48 MHz Digital Frequency-Locked Loop (DFLL48M) | Lose Lock After Wake (LLAW) Usage | 2.8.4 | When the Lose Lock After Wake (DFLLCTRLB.LLAW) is set, the DFLL may maintain lock (STATTUS.DFLLLOCK = 1) after the DFLL is disabled. If the DFLL lock (STATUS.DFLLLOCK = 1) is maintained when the DFLL is reconfigured and then enabled, some bits may not be properly set. | X | X | X |
| 48 MHz Digital Frequency-Locked Loop (DFLL48M) | DFLL48M Status flags | 2.8.5 | The STATUS.DFLLLCKF and STATUS.DFLLLCKC status bits are not automatically cleared when disabling the DFLL while it is running in close loop mode. | X | X | X |
| 48 MHz Digital Frequency-Locked Loop (DFLL48M) | DFLL48M Status flags | 2.8.6 | DFLL48M Status flags may have unexpected values during DFLL48 registers (DFLLCTRLA, DFLLCTRLB, DFLLMUL, DFLLVAL) configuration. | X | X | X |
| 48 MHz Digital Frequency-Locked Loop (DFLL48M) | Lose Lock After Wake (LLAW) Usage | 2.8.7 | Changing Lose Lock After Wake (DFLLCTRLB.LLAW) when the DFLL is not completely stopped can produce a corruption of the closed loop controller and the lock status. | X | X | X |
| Digital-to-Analog Converter (DAC) | RESERVED | 2.9.1 | RESERVED | | | |
| Digital-to-Analog Converter (DAC) | VDDANA as the DAC Reference | 2.9.2 | The selection of VDDANA as the DAC reference in DAC.CTRLB.REFSEL is non-functional. | X | | |
| Digital-to-Analog Converter (DAC) | DAC on Negative Input AIN3 | 2.9.3 | No analog compare will be done on Comparator 1 (AC1) when using the DAC on negative input AIN3. | X | | |
| Digital-to-Analog Converter (DAC) | Interpolation Mode | 2.9.4 | If the Interpolation mode is enabled (with filter integrated to the DAC), the last data from the filter is missing, hence the DAC final output value does not correspond to the DAC input value. | X | X | X |
| Digital-to-Analog Converter (DAC) | Reference | 2.9.5 | The reference select of the DAC (CTRLB.REFSEL) will default to a '0' if the DAC Software Reset (CTRLA.SWRST) is used to reset the module. | X | X | X |
| Digital-to-Analog Converter (DAC) | First Conversion | 2.9.6 | When the internal bandgap reference is selected as reference voltage, the DAC Startup Ready bits value is not correct for the first DAC Conversion after device power-up or after wake-up from Standby Low-Power mode. | X | X | X |
| Digital-to-Analog Converter (DAC) | Refresh Mode | 2.9.7 | The DAC Conversion Refresh mode is not functional. | X | X | X |
| Direct Memory Access Controller (DMAC) | Linked Descriptors | 2.10.1 | When at least one channel using linked descriptors is already active, a channel Fetch Error (FERR) could occur on enabling a channel with no linked descriptor or the second descriptor (index 1) of the channel being enabled could be fetched by one of the already active channels using linked descriptors. | X | X | |

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| Module | Feature | Item Number | Issue Summary | Affected Revisions | | |
|---|---|---|---|---|---|---|
| | | | | A | D | F |
| Direct Memory Access Controller (DMAC) | Channel Priority | 2.10.2 | When using channels with different priority levels, the highest priority channel could stall at the end of its current block. | X | | |
| Direct Memory Access Controller (DMAC) | DMAC in Debug Mode | 2.10.3 | In debug mode, DMAC does not restart after a debug halt when DBGCTRL.DBGRUN=0. | X | | |
| Ethernet MAC (GMAC) | Ethernet Functionality in 64-pin Packages | 2.11.1 | Ethernet functionality in 64-pin packages is not available. | X | | |
| External Interrupt Controller (EIC) | Edge Detection | 2.12.1 | When enabling EIC, SYNCBUSY.ENABLE is released before EIC is fully enabled. Edge detection can be done only after three cycles of the selected GCLK (GCLK_EIC or CLK_ULP32K). | X | X | X |
| External Interrupt Controller (EIC) | Asynchronous Edge Detection | 2.12.2 | When the asynchronous edge detection is enabled and the system is in Standby mode, only the first edge will be detected. The following edges are ignored until the system wakes up. | X | X | X |
| Fractional Digital Phase-Locked Loop (FDPLL) | Input Clock on FDPLLn | 2.13.1 | Several FDPLL unlocks could occur while the output frequency is stable. | X | X | |
| Fractional Digital Phase-Locked Loop (FDPLL) | FDPLL Ratio in DPLLnRATIO | 2.13.2 | When changing the FDPLL ratio in DPLLnRATIO register on-the-fly, STATUS.DPLLnLDRTO will not beset when the ratio update will be completed. | X | X | X |
| Non-Volatile Memory Controller (NVMCTRL) | NVM Read Corruption | 2.14.1 | NVM reads could be corrupted when mixing NVM reads with Page Buffer writes. | X | X | |
| Non-Volatile Memory Controller (NVMCTRL) | SmartEEPROM Buffered Mode | 2.14.2 | SmartEEPROM Buffered mode is not recommended | X | X | X |
| Non-Volatile Memory Controller (NVMCTRL) | Debugger Illegal Accesses | 2.14.3 | Debugger illegal NVMCTRL address space read transactions return invalid data. Debugger illegal NVMCTRL address space write transactions are silently ignored. | X | X | X |
| Peripheral Access Controller (PAC) | PAC Protection Error in FREQM | 2.15.1 | FREQM reads on the Control B register (FREQM.CTRLB) generate a PAC protection error. | X | X | X |
| Peripheral Access Controller (PAC) | PAC Protection Error in CCL | 2.15.2 | Writing the Software Reset bit in the Control A register (CTRLASWRST) will trigger a PAC protection error. | X | X | X |
| I/O Pin Controller (PORT) | PORT Read/Write Attempts on Non-Implemented Registers | 2.16.1 | PORT read/write attempts on non-implemented registers, including addresses beyond the last implemented register group (PA, PB,...), do not generate a PAC protection error. | X | X | X |
| I/O Pin Controller (PORT) | PORT Pull-Up/Pull-Down Resistor | 2.16.2 | The pull-down on PA24/PA25 are activated during power-up and when Sleep mode is OFF. On all other pins, except those in the VSWOUT cluster, the pull-up is activated during power-up and when Sleep mode is OFF. | X | | |
| Real-Time Counter (RTC) | Write Corruption | 2.17.1 | A 8-bit or 16-bit write access for a 32-bit register, or 8-bit write access for a 16-bit register can fail for the following registers: <br>• The COUNT register in COUNT32 mode <br>• The COUNT register in COUNT16 mode <br>• The CLOCK register in CLOCK mode | X | X | X |
| Real-Time Counter (RTC) | Count Read Sync Enable Synchronization Busy | 2.17.2 | When CTRLA.COUNTSYNC is enabled, the first COUNT value is not correctly synchronized and therefore it is a wrong value. | X | X | X |
| Real-Time Counter (RTC) | Tamper Input Filter | 2.17.3 | Majority debouncing, as part of RTC tamper detection, does not work, when enabled by setting Debouncer Majority Enable bit CTRLB.DEBMAJ. | X | X | X |
| Real-Time Counter (RTC) | Tamper Detection | 2.17.4 | Upon enabling the RTC, a false tamper detection could be reported by the RTC. | X | X | X |
| Real-Time Counter (RTC) | Tamper Detection Timestamp | 2.17.5 | If an external reset occurs during a tamper detection, the TIMESTAMP register will not be updated when next tamper detection is triggered. | X | X | X |

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| Module | Feature | Item Number | Issue Summary | Affected Revisions | | |
|---|---|---|---|:---:|:---:|:---:|
| | | | | A | D | F |
| Real-Time Counter (RTC) | PRESCALER | 2.17.6 | When the tamper or debouncing features (TAMPCTRL) are enabled, periodic interrupts and events are generated when the prescaler is OFF (CTRLA.PRESCALER=0). | X | X | X |
| Real-Time Counter (RTC) | Tamper Detection Timestamp | 2.17.7 | The INTFLAG.TAMPER bit is not reset by reading the TIMESTAMP register. | X | X | X |
| Real-Time Counter (RTC) | General Purpose Registers | 2.17.8 | General Purpose Registers n (GPn) are reset on tamper detection even if GPTRST = 0. | X | X | X |
| Real-Time Counter (RTC) | Battery Backup Mode | 2.17.9 | Entering Battery Backup mode without waiting for SYNCBUSY.ENABLE and SYNCBUSY.COUNTSYNC synchronization completion may freeze these bits status. | X | X | X |
| Real-Time Counter (RTC) | Active Layer Protection | 2.17.10 | When the RTC is configured in Active Layer Protection mode (TAMPCTRL.INACT = 0x3) and the RTC CTRLA.ENABLE bit is not set, a tamper can be detected and a timestamp captured. The TAMPID register and INTFLAG.TAMPER bit may not be set. | X | X | X |
| Serial Communication Interface (SERCOM) | SERCOM-USART: USART Auto-Baud Mode | 2.18.1 | In USART Auto-Baud mode, missing stop bits are not recognized as inconsistent sync (ISF) or framing (FERR) errors. | X | X | X |
| Serial Communication Interface (SERCOM) | SERCOM-USART: Collision Detection | 2.18.2 | In USART operating mode with Collision Detection enabled (CTRLB.COLDEN=1), the SERCOM will not abort the current transfer as expected if a collision is detected and if the SERCOM APB Clock is lower than the SERCOM Generic Clock. | X | X | X |
| Serial Communication Interface (SERCOM) | SERCOM-USART: Debug Mode | 2.18.3 | In USART operating mode, if DBGCTRL.DBGSTOP=1, data transmission is not halted after entering Debug mode. | X | X | X |
| Serial Communication Interface (SERCOM) | SERCOM-SPI: 32-bit Extension Mode | 2.18.4 | When 32-bit Extension mode is enabled and data to be sent is not in multiples of 4 bytes (which means the length counter must be enabled), additional bytes will be sent over the line. | X | X | X |
| Serial Communication Interface (SERCOM) | SERCOM-UART: TXINV and RXINV Bits | 2.18.5 | The TXINV and RXINV bits in the CTRLA register have inverted functionality. | X | X | X |
| Serial Communication Interface (SERCOM) | SERCOM-I$^2$C: SDAHOLD Timing | 2.18.6 | SDAHOLD timing of the SERCOM-I$^2$C does not match the value shown in the current device data sheet. | X | X | X |
| Serial Communication Interface (SERCOM) | SERCOM-I$^2$C: Repeated Start in High-Speed Host Write Operation | 2.18.7 | For High-Speed Host Write operations, writing CTRLB.CMD = 0x1 issues a STOP command instead of a Repeated Start making repeated start not possible in that mode. | X | X | X |
| Serial Communication Interface (SERCOM) | SERCOM-I$^2$C: Repeated Start in High-Speed Host Read Operation | 2.18.8 | For High-Speed Host Read operations, sending a NACK (CTRLB.CMD = 0x2) forces a STOP to be issued making repeated start not possible in that mode. | X | X | X |
| Serial Communication Interface (SERCOM) | SERCOM-I$^2$C: STATUS.CLKHOLD Bit in Host and Client Modes | 2.18.9 | The STATUS.CLKHOLD bit in host and client modes can be written whereas it is a read-only status bit. | X | X | X |
| Serial Communication Interface (SERCOM) | SERCOM-I$^2$C: I$^2$C in Client Mode | 2.18.10 | In I$^2$C mode, LENERR, SEXTOUT, LOWTOUT, COLL and BUSERR bits are not cleared when INTFLAG.AMATCH is cleared. | X | X | X |
| Serial Communication Interface (SERCOM) | SERCOM-I$^2$C: Client Mode with DMA | 2.18.11 | In I$^2$C Client Transmitter mode, at the reception of a NACK, if there is still data to be sent in the DMA buffer, the DMA will push a data to the DATA register. | X | X | X |
| Serial Communication Interface (SERCOM) | SERCOM-I$^2$C: I$^2$C Client in DATA32B Mode | 2.18.12 | When SERCOM is configured as an I$^2$C client in 32-bit Data Mode (DATA32B=1) and the I$^2$C host reads from the I$^2$C client (client transmitter) and outputs its NACK (indicating no more data is needed), the I$^2$C client still receives a DRDY interrupt. | X | X | X |
| Serial Communication Interface (SERCOM) | SERCOM-I$^2$C: 10-bit Addressing Mode | 2.18.13 | 10-bit addressing in I$^2$C Client mode is not functional. | X | X | X |
| Serial Communication Interface (SERCOM) | SERCOM-I$^2$C: Repeated Start | 2.18.14 | When the Quick command is enabled (CTRLB.QCEN=1), software can issue a repeated Start by writing either CTRLB.CMD or ADDR.ADDR bit fields. | X | X | X |

| | | | | Affected Revisions | | |
|---|---|---|---|---|---|---|
| Module | Feature | Item Number | Issue Summary | A | D | F |
| Serial Communication Interface (SERCOM) | SERCOM-SPI: Data Preload | 2.18.15 | In SPI Client mode with Client Data Preload Enabled, the client transmitter may discard some data if the host cannot keep the SPI Select pin low until the end of transmission. | X | X | X |
| Serial Communication Interface (SERCOM) | Repeated Start | 2.18.16 | For Host Write operations (excluding High-Speed mode), in 10-bit addressing mode, writing CTRLB.CMD = 0x1 does not issue correctly a Repeated Start command. | X | X | X |
| Serial Communication Interface (SERCOM) | SERCOM-USART: Wakeup | 2.18.17 | The USART does not wake-up the device on Error (INTFLAG.ERROR=1) interrupt. | X | X | X |
| Serial Communication Interface (SERCOM) | SERCOM-USART: LENGTH | 2.18.18 | When the USART is used in 32-bit mode with hardware handshaking (CTS/RTS) the TXC interrupt flag (INTFLAG.TXC) may be set before transmission has completed. The TXC interrupt flag may incorrectly be set regardless of Data Length Enable (LENGTH.LENEN) is set to '0' or '1'. | X | X | X |
| Serial Communication Interface (SERCOM) | SERCOM-USART: Overconsumption in Standby mode | 2.18.19 | Unexpected over-consumption in standby mode | X | X | X |
| Serial Communication Interface (SERCOM) | Wake-up Interrupt | 2.18.20 | The Data Register Empty (DRE) wake-up interrupt is not de-asserted when the register interrupt is cleared (INTFLAG.DRE=0). | X | X | X |
| Serial Communication Interface (SERCOM) | Client Data Preload | 2.18.21 | Preloading a new SPI data before going into Standby Sleep mode, may lead to extra power consumption. | X | X | X |
| Serial Communication Interface (SERCOM) | Hardware SPI Select Control | 2.18.22 | When Hardware SPI Select Control is enabled, the SPI Select ($\overline{SS}$) pin goes high after each byte transfer. | X | X | X |
| Serial Communication Interface (SERCOM) | SERCOM-I$^2$C: Automatic Acknowledge | 2.18.23 | The I$^2$C Client Automatic Acknowledge feature (CTRLB.AACKEN = 1) is not supported when doing a repeated start. | X | X | X |
| Serial Communication Interface (SERCOM) | SERCOM-I$^2$C: Wakeup | 2.18.24 | When an unexpected STOP occurs on the I$^2$C bus the STATUS.BUSERR & INTFLAG.ERROR bits are set but may not wake the system from sleep mode. An unexpected START will not produce this issue. | X | X | X |
| Serial Communication Interface (SERCOM) | Software Reset | 2.18.25 | Software Reset (CTRLA.SWRST=1) is not functional when the SERCOM is not enabled (CTRAL.ENABLE=0). | X | X | X |
| Supply Controller (SUPC) | Buck Converter Mode | 2.19.1 | Digital Phase-Locked Loop (FDPLL200Mx2) and Digital Frequency-Locked Loop (DFLL48M) PLL's cannot be used with main voltage regulator in Buck converter mode. | X | X | X |
| Supply Controller (SUPC) | BOD33 Hysteresis | 2.19.2 | The hysteresis feature of the 3.3V BOD is not functional while the device is in STANDBY sleep mode. | X | X | X |
| Timer/Counter (TC) | PERBUF/CCBUFx Register | 2.20.1 | When clearing the STATUS.PERBUFV/STATUS.CCBUFx flag, the SYNCBUSY flag is released before the PERBUF/CCBUFx register is restored to its appropriate value. | X | X | X |
| Timer/Counter (TC) | Retrigger | 2.20.2 | If a Retrigger event occurs at the Channel Compare Match [n] time, the next Waveform Output [n] is missing or disturbed. | X | X | X |
| Timer/Counter (TC) | PER register (8-bit mode) | 2.20.3 | In 8-bit Mode, PER register updates using the DMA are not possible in standby mode. | X | X | X |
| Timer/Counter for Control Applications (TCC) | TCC with EVSYS in SYNC/RESYNC Mode | 2.21.1 | TCC peripheral is not compatible with an EVSYS channel in SYNC or RESYNC mode. | X | X | X |
| Timer/Counter for Control Applications (TCC) | Dithering Mode with External Retrigger Events | 2.21.2 | Using TCC in Dithering mode with external retrigger events can lead to an unexpected stretch of right aligned pulses, or shrink of left-aligned pulses. | X | X | X |
| Timer/Counter for Control Applications (TCC) | ALOCK Feature | 2.21.3 | ALOCK feature is not functional. | X | X | X |

| Module | Feature | Item Number | Issue Summary | Affected Revisions | | |
|---|---|---|---|---|---|---|
| | | | | A | D | F |
| Timer/Counter for Control Applications (TCC) | LUPD feature in Down-Counting mode | 2.21.4 | In down-counting mode, the Lock Update bit (CTRLB.LUPD) does not protect against a PER register update from the PERBUF register. | X | X | X |
| Timer/Counter for Control Applications (TCC) | Re-trigger in RAMP2 Operations | 2.21.5 | Re-trigger in RAMP2 operations is not supported if a prescaler is used and the re-trig of the counter is done on the next GCLK. | X | X | X |
| Timer/Counter for Control Applications (TCC) | Re-trigger | 2.21.6 | If a Retrigger event occurs at the Channel Compare Match [n] time, the next Waveform Output [n] is missing or disturbed. | X | X | X |
| Timer/Counter for Control Applications (TCC) | RAMP2 operations | 2.21.7 | Timer/Counter counting down mode (CTRLBCLR.DIR = CTRLBSET.DIR = 1) is not supported in RAMP2 operations. | X | X | X |
| Timer/Counter for Control Applications (TCC) | Dithering Mode | 2.21.8 | Retrigger in RAMP2 operations is not supported in Dithering Mode. | X | X | X |
| Timer/Counter for Control Applications (TCC) | STATUS Register Access | 2.21.9 | 8-bit or 16-bit writes to the STATUS register are forbidden. | X | X | X |
| Timer/Counter for Control Applications (TCC) | DMA One-Shot Trigger Mode | 2.21.10 | TCC Counter Overflow (OVF) DMA Trigger in DMA One-Shot Trigger Mode is not functional for Critical RAMP2C and RAMP2CS operation modes. | X | X | X |
| PDEC | Reserved | 2.22.1 | - | | | |
| PDEC | Angular and Revolution Counters | 2.22.2 | With index input enabled i.e., EVCTRL.EVEI[2] and operating in X4/X2 mode, angular and revolution counters are incremented/decremented by two separate and unsynchronized sources. | X | X | X |
| PDEC | Counter Operating Mode | 2.22.3 | Counting Events is not functional in COUNTER operating mode. | X | X | X |
| PDEC | Counter Operating Mode | 2.22.4 | Start, restart or retrigger on event is not functional in COUNTER operating mode. | X | X | X |
| PDEC | Direction Change | 2.22.5 | A direction change detection (INTFLAG.DIR = 1) updates the STATUS.DIR bit with a variable delay. | X | X | X |
| PDEC | Hall Mode | 2.22.6 | A windows error (WINERR) can be reported after a START command execution, or when leaving standby (with RUNSTDBY = 0). | X | X | X |
| PDEC | Hall Mode | 2.22.7 | In HALL mode, WINERR Error interrupt (INTFLAG.WINERR = 1) can rise several times on a low-speed window error detection. | X | X | X |
| PDEC | Error Flags | 2.22.8 | An error detection (INTFLAG.ERR = 1) updates the STATUS Error flags (HERR, WINERR, MPERR, IDXERR, QERR) with a variable delay. | X | X | X |
| Voltage Reference System | Temperature sensor | 2.23.1 | Temperature sensors are not supported. | X | X | X |
| EVSYS | Synchronous Mode | 2.24.1 | Spurious Overrun Interrupt when the generic clock for a channel is always on. | X | X | X |
| EVSYS | Software Events | 2.24.2 | Software Events are not supported in Synchronous and Resynchronized modes. | X | X | X |
| EVSYS | Synchronous/Resynchronized Modes | 2.24.3 | In synchronous and resynchronized modes, spurious event detections can be generated when registers in peripherals connected to the AHB-APB bridge on which the EVSYS is connected are accessed. | X | X | X |
| TRNG | Over Consumption | 2.25.1 | When TRNG is disabled, some internal logic could continue to operate causing an over consumption. | X | X | X |

| | | | | | Affected Revisions | | |
|---|---|---|---|---|---|---|---|
| Module | Feature | Item Number | Issue Summary | | A | D | F |
| OSC32KCTRL | Clock Switch Back Feature Limitation | 2.26.1 | In the case an application can recover the XOSC32K from a Clock Failure Detection, the application can switch back to the XOSC32K clock (CFDCTRL.SWBACK = 1). | | X | X | X |
| OSCCTRL | Clock Switch Back Feature Limitation | 2.27.1 | In the case an application can recover the XOSC from a Clock Failure Detection, the application can switch back to the XOSC clock using Clock Switch Back feature (XOSCCTRL.SWBEN = 1). | | X | X | X |

**Notes:**

- Cells with 'X' indicates the issue is present in this revision of the silicon.
- Cells with '-' indicates this silicon revision does not exist for this issue.
- The blank cell indicates the issue has been corrected or does not exist in this revision of the silicon.

## 2.    Silicon Errata Issues

The following errata issues apply to the SAM D5x/E5x family of devices.

**Note:** Cells with an 'X' indicates the issue is present in this revision of the silicon.
Cells with a dash ('-') indicate this silicon revision does not exist for this issue.

Blank cells indicate the issue has been corrected or does not exist in this revision of the silicon.

### 2.1    Analog-to-Digital Converter (ADC)

#### 2.1.1    ADC SYNCBUSY.SWTRIG

The ADC SYNCBUSY.SWTRIG gets stuck to '1' after wake-up from Standby Sleep mode.

**Workaround**
Ignore the ADC SYNCBUSY.SWTRIG status when waking up from Sleep mode.

**Affected Silicon Revisions**

| A | D | F | | | | | |
|---|---|---|---|---|---|---|---|
| X | X | X | | | | | |

#### 2.1.2    ADC TUE/INL/DNL Performance

The ADC TUE/INL/DNL performance is not guaranteed in the following scenarios:
- Sampling frequency is above 500 ksps AND
- ADC $V_{REF}$ is different from VDDANA

**Workaround**
None.

**Affected Silicon Revisions**

| A | D | F | | | | | |
|---|---|---|---|---|---|---|---|
| X | | | | | | | |

#### 2.1.3    Reference Buffer Offset Compensation

ADC converted data could be erroneous when using the Reference Buffer (REFCTRL.REFSEL = INTREF, INTVCC0, VREFA or VREB) and when Reference Buffer Offset Compensation is enabled (REFCTRL.REFCOMP = 1).

**Workaround**
The first five conversions must be ignored. All further ADC module conversions are accurate.

**Affected Silicon Revisions**

| A | D | F | | | | | |
|---|---|---|---|---|---|---|---|
| X | X | X | | | | | |

#### 2.1.4    DMA Sequencing

ADC DMA Sequencing with prescaler > 8 (ADC->CTRLA.bit.PRESCALER>2) does not produce the expected channel sequence.

**Workaround**

Keep the prescaler setting to a maximum of 8, and use the GCLK Generator divider if more prescaling is needed.

**Affected Silicon Revisions**

| A | D | F | | | | | |
|---|---|---|---|---|---|---|---|
| X | X | X | | | | | |

### 2.1.5 DMA Sequencing

ADC DMA sequencing with averaging enabled (AVGCTRL.SAMPLENUM>1) without the AVGCTRL bit set (DSEQCTRL.AVGCTRL= 0) in the update sequence does not produce the expected channel sequence.

**Workaround**

Add the AVGCTRL register in the register update list (DSEQCTRL.AVGCTRL= 1) and set the desired value in this list.

**Affected Silicon Revisions**

| A | D | F | | | | | |
|---|---|---|---|---|---|---|---|
| X | X | X | | | | | |

### 2.1.6 Internal Bandgap Reference

If the internal bandgap voltage reference is selected (REFCTRL.REFSEL = 0x0), ADC conversions may never complete (INTFLAG.RESRDY = 0).

**Workaround**

If CTRLA.ONDEMAND = 0: Add a delay of minimum 40 µs between the enable of the ADC (CTRLA.ENABLE) and the start of the first conversion.

If an ADC conversion is triggered by an input event, the delay must be introduced between the enable of the ADC and the enable of the ADC EVSYS channel.

If CTRLA.ONDEMAND = 1: There is no workaround.

**Affected Silicon Revisions**

| A | D | F | | | | | |
|---|---|---|---|---|---|---|---|
| X | X | X | | | | | |

## 2.2 Analog Comparator (AC)

### 2.2.1 AC Hysteresis

Enabling Hysteresis (COMPCTRLn.HYSTEN = 0x1) changes the threshold voltage (VTH-), which could result in unexpected behavior of the Analog Comparator.

**Workaround**

None.

**Affected Silicon Revisions**

| A | D | F | | | | | |
|---|---|---|---|---|---|---|---|
| X | X | | | | | | |

### 2.2.2 Output

In Continuous mode the comparator output may toggle during startup time before the Ready Status bit is set (STATUSB.READY = 1).

**Workaround**
None.

**Affected Silicon Revisions**

| A | D | F | | | | | |
|---|---|---|---|---|---|---|---|
| X | X | X | | | | | |

### 2.2.3 Standby Sleep Mode

A comparison in single shot mode will not be completed when entering in Standby Sleep mode with RUNSTDBY = 0.

**Workaround**
Set RUNSTBDY = 1 before entering in Standby mode or wait for Standby exit to start a new comparison.

**Affected Silicon Revisions**

| A | D | F | | | | | |
|---|---|---|---|---|---|---|---|
| X | X | X | | | | | |

### 2.2.4 Debug Mode

Continuous comparisons cannot be halted in Debug mode.

**Workaround**
None.

**Affected Silicon Revisions**

| A | D | F | | | | | |
|---|---|---|---|---|---|---|---|
| X | X | X | | | | | |

## 2.3 Configurable Custom Logic (CCL)

### 2.3.1 Enable Protected Registers

The SEQCTRLx and LUCTRLx registers are enable-protected by the CTRL.ENABLE bit, whereas they must be enable-protected by the LUTCTRLx.ENABLE bits.

**Workaround**
None.

**Affected Silicon Revisions**

| A | D | F | | | | | |
|---|---|---|---|---|---|---|---|
| X | X | X | | | | | |

### 2.3.2 Sequential Logic Reference

LUT Output is corrupted after enabling CCL when sequential logic is used.

**Workaround**

Write the CTRL register twice when enabling the CCL.

**Affected Silicon Revisions**

| A | D | F | | | | | |
|---|---|---|---|---|---|---|---|
| X | X | X | | | | | |

## 2.4    Controller Area Network (CAN)

### 2.4.1    CAN Edge Filtering

When edge filtering is activated (CCCR.EFBI = 1) and when the end of the integration phase coincides with a falling edge at the Rx input pin, it may occur that the CAN synchronizes itself incorrectly and does not correctly receive the first bit of the frame. In this case, the CRC will detect the first bit that was received incorrectly, it will rate the received FD frame as faulty, and an error frame will be send.

The issue only occurs when there is a falling edge at the Rx input pin (CAN_RX) within the last time quantum (tq) before the end of the integration phase. The last time quantum of the integration phase is at the sample point of the 11th recessive bit of the integration phase. When edge filtering is enabled, the bit timing logic of the CAN sees the Rx input signal delayed by the edge filtering. When the integration phase ends, edge filtering is automatically disabled. This affects the reset of the FD CRC registers at the beginning of the frame. The Classical CRC register is not affected, hence this issue does not affect the reception of Classical frames.

In CAN communication, the CAN module may enter an integrating state (either by resetting the CCCR.INIT or by protocol exception event) while a frame is active on the bus. In this case, the 11 recessive bits are counted between the acknowledge bit and the following start of frame. All nodes have synchronized at the beginning of the dominant acknowledge bit. This means that the edge of the following start of frame bit cannot fall on the sample point, therefore the issue does not occur. The issue occurs only when the CAN is by local errors, mis-synchronized with regard to the other nodes.

Glitch filtering as specified in ISO 11898-1:2015 is fully functional.

Edge filtering was introduced for applications where the data bit time is at least 2-tq (of nominal bit time) long. In that case, edge filtering requires at least two consecutive dominant time quanta before the counter counting the 11 recessive bits for idle detection is restarted. This means edge filtering covers the theoretical case of occasional 1-tq long dominant spikes on the CAN bus that would delay idle detection. Repeated dominant spikes on the CAN bus would disturb all CAN communication, so the filtering to speed up idle detection would not help network performance.

When this rare event occurs, the CAN sends an error frame and the sender of the affected frame retransmits the frame. When the retransmitted frame is received, the CAN has left the integration phase and the frame will be received correctly. Edge filtering is only applied during the integration phase and it is never used during normal operation. Because the integration phase is very short with respect to "active communication time", the impact on total error frame rate is negligible. The issue has no impact on data integrity.

The CAN enters the integration phase under the following conditions:
*   When CCCR.INIT is set to '0' after start-up
*   After a protocol exception event (only when CCCR.PXHD = 0)

**Scope:**

The erratum is limited to FD frame reception when edge filtering is active (CCCR.EFBI = 1) and when the end of the integration phase coincides with a falling edge at the Rx input pin.

**Effects:**

The calculated CRC value does not match the CRC value of the received FD frame and the CAN module sends an error frame. After retransmission the frame is received correctly.

**Workaround:**

Disable edge filtering or wait on retransmission in the event that this rare event occurs.

**Affected Silicon Revisions**

| A | D | F | | | | | |
|---|---|---|---|---|---|---|---|
| X | X | X | | | | | |

## 2.4.2  Dominant Bit of Intermission

When NBTP.NTSEG2 is configured to zero (Phase_Seg2(N) = 1), and when there is a pending transmission request, a dominant third bit of intermission may cause the CAN to wrongly transmit the first identifier bit dominant instead of recessive, even if this bit was configured as '1' in the Tx Buffer Element of the CAN module.

**Workaround**

A phase buffer segment 2 of length '1' (Phase_Seg2(N) = 1) is not sufficient to switch to the first identifier bit after the sample point in intermission where the dominant bit was detected.

The CAN protocol according to ISO 11898-1 defines that a dominant third bit of intermission causes a pending transmission to be started immediately. The received dominant bit is handled as if the CAN has transmitted a Start-of-Frame (SoF) bit.

The ISO 11898-1 specifies the minimum configuration range for Phase_Seg2(N) to be 2..8 tq. Therefore, excluding a Phase_Seg2(N) of '1' will not affect CAN conformance.

*Effects:*

If NBTP.NTSEG2 = 0, it may occur that the CAN transmits the first identifier bit dominant instead of recessive.

Update configuration range of NBTP.NTSEG2 from 0..127 tq to 1..127 tq in the CAN documentation.

**Affected Silicon Revisions**

| A | D | F | | | | | |
|---|---|---|---|---|---|---|---|
| X | X | X | | | | | |

## 2.4.3  Message Transmitted with Wrong Arbitration and Control Fields

**Description:**

Under the following conditions a message with wrong ID, format, and DLC is transmitted:

- The CAN is in the "Receiver" (PSR.ACT ≠0b10) state, hence no pending transmission
- A new transmission is requested before the third bit of intermission is reached
- The CAN bus is sampled dominant at the third bit of intermission which is treated as SoF (See ISO11898-1:2015, "Section 10.4.2.2")

Under the conditions above, the following might happen:

- The shift register is not loaded with ID, format, and DLC of the requested message
- The CAN will start arbitration with wrong ID, format, and DLC on the next bit
- If the ID wins arbitration, a CAN message with a valid CRC is transmitted
- If this message is acknowledged, the ID stored in the Tx event FIFO is the ID of the requested Tx message and not the ID of the message transmitted on the CAN bus, hence no error is detected by the transmitting CAN

**Scope:**

The erratum is limited when CAN is in the "Receiver" (PSR.ACT = 0b10) state with no pending transmission (register TXBRP == 0) and a new transmission is requested before the third bit of intermission is reached and this third bit of intermission is seen dominant.

When a transmission is requested by the CPU by writing to TXBAR, the Tx message handler performs an internal arbitration and loads the pending transmit message with the highest priority into its output buffer and then sets the transmission request for the CAN Protocol Controller. The problem occurs only when the transmission request for the CAN Protocol Controller is activated in the critical time window between the sample points of the second and third bit of intermission and if that third bit of intermission is seen dominant.

This dominant level at the third bit of intermission may result from an external disturbance or may be transmitted by another node with a significantly faster clock.

**Effects:**

In the described case it may happen that the shift register is not loaded with arbitration and control field of the message to be transmitted. The frame is transmitted with wrong ID, format, and DLC but with the data field of the requested message. The message is transmitted in correct CAN (FD) frame format with a valid CRC.

If the message loses arbitration or is disturbed by an error, it is retransmitted with correct arbitration and control fields.

**Workarounds**

- **Workaround 1:** Request a new transmission only if another transmission is already pending (that is, register TXBRP ≠ 0) or when the CAN is not in the "Receiver" (when PSR.ACT ≠ 0b10) state. To avoid activating the transmission request in the critical time window between the sample points of the second and third bit of intermission, the application software can evaluate the Rx interrupt flags, such as IR.DRX, IR.RF0N, and IR.RF1N, which are set at the last bit of EoF when a received and accepted message becomes valid. The last bit of EoF is followed by third bits of intermission. Therefore the critical time window has safely terminated three bit times after the Rx interrupt. Now a transmission may be requested by writing to TXBAR. After the interrupt, the application has to take care that the transmission request for the CAN Protocol Controller is activated before the critical window of the following reception is reached.
- **Workaround 2:** If a transmission is to be requested while no other transmission request is already pending and the CAN bus is not idle, set the CCCR.INIT bit (which stops the CAN protocol controller), set the transmission request and clear the CCCR.INIT bit. The message currently being received when the CCCR.INIT bit is set will be lost, but no errors (or error frames) will be generated and the CAN protocol controller will re-integrate into the CAN communication immediately at the 11 recessive bits of the next End-of-Frame including intermission.
- **Workaround 3:** It is also possible to keep the number of pending transmissions always at > 0 by frequently requesting a message, then the condition "no pending transmission" is never met. The frequently requested message may be given a low priority, losing arbitration to all other messages.

**Affected Silicon Revisions**

| A | D | F | | | | | |
|---|---|---|---|---|---|---|---|
| X | X | X | | | | | |

### 2.4.4 DAR Mode

When the CAN is configured in DAR mode (CCCR.DAR = 1) the automatic retransmission for transmitted messages that have been disturbed by an error or have lost arbitration is disabled. When the transmission attempt is not successful, the Tx Buffer's Transmission Request bit (TXBRP.TRPn) will be cleared and the Tx Buffer's Cancellation Finished bit (TXBCF.CFn) will be set.

When the transmitted message loses arbitration at one of the first two identifier bits, chances are that instead of the bits of the actually transmitted Tx Buffer, the TXBRP.TRPn and TXBCF.CFn bits of the previously started Tx Buffer (or Tx Buffer 0 if there is no previous transmission attempt) are written (TXBRP.TRPn = 0, TXBCF.CFn = 1).

If in this case the TXBRP.TRPn bit of the Tx Buffer that lost arbitration at the first two identifier bits are not cleared, retransmission is attempted. When the CAN loses arbitration again at the immediately following retransmission, then actually and previously transmitted Tx Buffer are the same and this Tx Buffer's TXBRP.TRPn bit is cleared and its TXBCF.CFn bit is set.

**Scope:**

The erratum is limited to the case when the CAN loses arbitration at one of the first two transmitted identifier bits while in DAR mode. The problem does not occur when the transmitted message is disturbed by an error.

**Effects:**

In this case, it might happen that the TXBRP.TRPn bit is cleared after the second transmission attempt instead of the first. Additionally it may happen that the TXBRP.TRPn bit of the previously started Tx Buffer is cleared, if it has been set again. As in this case the previously started Tx Buffer has lost CAN internal arbitration against the active

Tx Buffer, its message has a lower identifier priority. It would also have lost arbitration on the CAN bus at the same position.

**Workaround**

None.

**Affected Silicon Revisions**

| A | D | F | | | | | |
|---|---|---|---|---|---|---|---|
| X | X | X | | | | | |

## 2.4.5 High-Priority Message (HPM) interrupt

There are two configurations where the issue occurs:

**Configuration A:**

- At least one Standard Message ID Filter Element is configured with priority flag set (S0.SFEC = 0b100/0b101/0b110)
- No Extended Message ID Filter Element configured
- Non-matching extended frames are accepted (GFC.ANFE = 0b00/0b01)

The HPM interrupt flag IR.HPM is set erroneously on reception of a non-high-priority extended message under the following conditions:

1. A standard HPM frame is received and accepted by a filter with priority flag set (that is, Interrupt flag IR.HPM is set as expected).
2. An extended frame is received and accepted because of the GFC.ANFE configuration (that is, Interrupt flag IR.HPM is set erroneously).

**Configuration B:**

- At least one Extended Message ID filter element is configured with priority flag set (F0.EFEC = 0b100/0b101/0b110)
- No Standard Message ID filter element is configured
- Non matching standard frames are accepted (GFC.ANFS = 0b00/0b01)

The HPM interrupt flag IR.HPM is set erroneously on reception of a non high-priority standard message under the following conditions:

1. An extended HPM frame is received and accepted by a filter with priority flag set (that is, Interrupt flag IR.HPM is set as expected).
2. A standard frame is received and accepted because of the GFC.ANFS configuration (that is, Interrupt flag IR.HPM is set erroneously).

**Scope:**

The erratum is limited to the following configurations:

**Configuration A:**

No Extended Message ID filter element is configured and non matching extended frames are accepted due to Global Filter Configuration (GFC.ANFE = 0b00/0b01).

**Configuration B:**

No Standard Message ID Filter Element configured and non-matching standard frames are accepted due to Global Filter Configuration (GFC.ANFS = 0b00/0b01).

**Effects:**

Interrupt flag IR.HPM is set erroneously at the reception of a frame with:

- Configuration A: Extended Message ID
- Configuration B: Standard Message ID

**Workaround**
**Configuration A:**

Setup an Extended Message ID filter element with the following configuration:

- F0.EFEC = 001/010: Select Rx FIFO for storage of extended frames
- F0.EFID1 = any value: The value is not relevant as all ID bits are masked out by F1.EFID2
- F1.EFT = 10: Classic filter, F0.EFID1 = filter, F1.EFID2 = mask
- F1.EFID2 = 0: All bits of the received extended ID are masked out

Now all extended frames are stored in Rx FIFO '0' or Rx FIFO '1' depending on the configuration of F0.EFEC.

**Configuration B:**

Setup an Standard Message ID filter element with the following configuration:

- S0.SFEC = 001/010: Select Rx FIFO for storage of standard frames
- S0.SFID1 = any value: The value is not relevant as all ID bits are masked out by S0.SFID2
- S0.SFT = 10: Classic filter, S0.SFID1 = filter, S0.SFID2 = mask
- S0.SFID2 = 0: All bits of the received standard ID are masked out

Now all standard frames are stored in Rx FIFO '0' or Rx FIFO '1' depending on the configuration of S0.SFEC.

**Affected Silicon Revisions**

| A | D | F | | | | | |
|---|---|---|---|---|---|---|---|
| X | X | X | | | | | |

## 2.4.6 Tx FIFO message sequence inversion

Assuming that there are two Tx FIFO messages in the output pipeline of the Tx Message Handler. Transmission of Tx FIFO message 1 is started:

Position 1: Tx FIFO message 1 (transmission ongoing)

Position 2: Tx FIFO message 2

Position 3: Free FIFO bugger

During the transmission of Tx FIFO message 1, a non Tx FIFO message with a higher CAN priority is requested. Due to its priority it will be inserted into the output pipeline. The TxMH performs "message scans" to keep the output pipeline up to date with the highest priority messages from the message RAM.

After the following two message scans, the output pipeline has the following content:

Position 1: Tx FIFO message 1 (transmission ongoing)

Position 2: non Tx FIFO message with higher CAN priority

Position 3: Tx FIFO message 2

If the transmission of Tx FIFO message 1 is not successful (lost arbitration or CAN bus error) it is pushed from the output pipeline by the non Tx FIFO message with higher CAN priority. The following scan again inserts Tx FIFO message 1 into the output pipeline at position 3:

Position 1: non Tx FIFO message with higher CAN priority (transmission ongoing)

Position 2: Tx FIFO message 2

Position 3: Tx FIFO message 1

This results in Tx FIFO message 2 being in the output pipeline in front of Tx FIFO message 1 and they are transmitted in that order, resulting in a message sequence inversion.

**Scope:**

The erratum describes the case when the CAN uses both, dedicated Tx Buffers and a Tx FIFO (TXBC.TFQM = 0) and the messages in the Tx FIFO do not have the highest internal CAN priority. The described sequence inversion

may also happen between two non Tx FIFO messages (Tx Queue or dedicated Tx Buffers) that have the same CAN identifier and that should be transmitted in the order of their buffer numbers (not the intended use).

**Effects:**

In the described case it may happen that two consecutive messages from the Tx FIFO exchange their positions in the transmit sequence.

**Workarounds**

When transmitting messages from a dedicated Tx Buffer with higher priority than the messages in the Tx FIFO, choose one of the following workarounds:

**Workaround 1**

Use two dedicated Tx Buffers, for example, use Tx Buffers 4 and 5 instead of the Tx FIFO.

The Transmit Loop below replaces the function that fills the Tx FIFO.

Write the message to Tx Buffer 4

Transmit Loop:

- Request Tx Buffer 4 - write TXBAR.A4
- Write message to Tx Buffer 5
- Wait until transmission of Tx Buffer 4 completed - IR.TC, read TXBTO.TO4
- Request Tx Buffer 5 - write TXBAR.A5
- Write message to Tx Buffer 4
- Wait until transmission of Tx Buffer 5 completed - IR.TC, read TXBTO.TO5

**Workaround 2**

Ensure that only one Tx FIFO element is pending for transmission at any time.

The Tx FIFO elements may be filled at any time with messages to be transmitted, but their transmission requests are handled separately. Each time a Tx FIFO transmission has completed and the Tx FIFO becomes empty (IR.TFE = 1), the next Tx FIFO element is requested.

**Workaround 3**

Use only a Tx FIFO. Send the message with the higher priority also from Tx FIFO.

Drawback: The higher priority message has to wait until the preceding messages in the Tx FIFO are sent.

**Affected Silicon Revisions**

| A | D | F | | | | | |
|---|---|---|---|---|---|---|---|
| X | X | X | | | | | |

### 2.4.7 Debug Message

In case the CCCR.INIT bit is set by the Host by writing to the CCCR register or when the M_CAN enters BusOff state, the debug message handling state machine stays in its current state instead of being reset to Idle state. Setting CCCR.CCE does not change RXF1S.DMS.

**Scope:**

The erratum is limited to the case when the Debug on CAN Support feature is active. Regular operation is not affected. In regular operation the debug message handling state machine always remains in Idle state.

**Effects:**

In the described case the debug message handling state machine is stopped and remains in the current state signaled by RXF1S.DMS. In case the RXF1S.DMS = 11, the output `m_can_dma_req` remains active.

**Workaround**

In case the debug message handling state machine has stopped while RXF1S.DMS = 01 or RXF1S.DMS = 10, it can be reset to Idle state by hardware reset or by reception of debug messages after CCCR.INIT is reset to '0'.

In case the debug message handling state machine has stopped while RXF1S.DMS = 11 with `m_can_dma_req` active, it can be reset to Idle state by hardware reset or by activating input `m_can_dma_ack`.

**Affected Silicon Revisions**

| A | D | F | | | | | |
|---|---|---|---|---|---|---|---|
| X | X | X | | | | | |

## 2.4.8 Reserved

## 2.4.9 On Demand

The CAN is not compatible with on-demand clock requests.

**Workaround**

Clear the ONDEMAND bit to zero for the oscillator source that provides the GCLK to the CAN.

**Affected Silicon Revisions**

| A | D | F | | | | | |
|---|---|---|---|---|---|---|---|
| X | X | X | | | | | |

## 2.4.10 Debug Mode

The ECR.CEL, PSR.PXE, PSR.RFDF, PSR.RBRS, PSR.RESI, PSR.DLEC and PSR.LEC bits can be corrupted by a debug access.

**Workaround**

Do not read the ECR, PSR registers with a debugger when the CPU is not halted in debug, otherwise debug access will clear those bits.

**Affected Silicon Revisions**

| A | D | F | | | | | |
|---|---|---|---|---|---|---|---|
| X | X | X | | | | | |

## 2.4.11 Debug Mode

An expected clear on read of the ECR.CEL, PSR.PXE, PSR.RFDF, PSR.RBRS, PSR.RESI, PSR.DLEC and PSR.LEC bits can be unexpectedly filtered-out when the CPU is halted.

**Workaround**

Do not halt the CPU if other hosts in the application are accessing the ECR or PSR registers.

**Affected Silicon Revisions**

| A | D | F | | | | | |
|---|---|---|---|---|---|---|---|
| X | X | X | | | | | |

### 2.4.12 Transmit Message Order Inversion

It may happen, depending on the delay between the individual Tx requests, that in the case where multiple Tx Buffers are configured with the same message ID, the Tx Buffers are not transmitted in order of the Tx Buffer number (lowest number first).

**Scope:**

The erratum is limited to the case when multiple Tx Buffers are configured with the same message ID.

**Effects:**

In the case described it may happen that Tx Buffers configured with the same message ID and pending Tx request are not transmitted with lowest Tx Buffer number first (message order inversion).

**Workaround**

First write the group of Tx messages with same message ID to the message RAM and then afterwards request transmission of all these messages concurrently by a single write access to TXBAR.

**Affected Silicon Revisions**

| A | D | F | | | | | |
|---|---|---|---|---|---|---|---|
| X | X | X | | | | | |

### 2.4.13 Tx (Queue) Buffers

**Scope:**

Use of multiple dedicated Tx Buffers or Tx Queue buffers configured with same message ID.

**Effects:**

If the dedicated Tx buffers with the same message ID are not requested in ascending order or at the same time or in case of multiple Tx Queue buffers with the same message ID, it cannot be guaranteed, that these messages are transmitted in ascending order with lowest buffer number first.

**Workaround**

In case a defined order of transmission is required the Tx FIFO will be used for transmission of messages with the same message ID. Alternatively dedicated Tx buffers with same message ID will be requested in ascending order with lowest buffer number first or by a single write access to TXBAR. Alternatively a single Tx Buffer can be used to transmit those messages one after the other.

**Affected Silicon Revisions**

| A | D | F | | | | | |
|---|---|---|---|---|---|---|---|
| X | X | X | | | | | |

### 2.4.14 Transmit Cancellation

If all of the following events have occurred:

- Transmission of the TX Buffer nn was not successful.
- The automatic retransmission mechanism has started to resend the TX Buffer nn and is currently sending the first four identifier bits.
- The user attempts to cancel the transaction by setting the TXBCR.CRnn bit.

The hardware will send a signal stating that the transaction or transmission was successfully canceled even when it has not been TXBCF.CFnn = 1 and TXBRP.TRPnn = 0. The hardware also states that frame was not transmitted on the bus TXBTO.TOnn = 0.

Other than what is signaled by TXBCF.CFnn and TXBTO.TOnn, the transmission continues until the complete frame has been sent on the CAN bus.

If the transmission is successful, the TXBTO.TOnn bit will be set. In this case new data is written to the TX Buffer nn while the transmission is still ongoing. A frame with inconsistent data may appear on the bus.

**Scope:**

This problem is limited to the case of transmit cancellation of CAN FD messages with more than eight data bytes, while automatic retransmission is enabled (CCCR.DAR = '0'). Transmit cancellation of Classical CAN messages and CAN FD messages with up to eight data bytes is not affected.

**Effects:**

When the TXBRP.TRPnn bit of the TX Buffer nn is reset by an incomplete transmit cancellation, this TX Buffer is reported to be free. If the software now writes new data to this TX Buffer while a transmission is still ongoing, this new data may be loaded into the protocol controller, leading to a data inconsistency of the transmitted frame. This means that the transmitted frame consists partly of the data available at start of frame, and data written to the TX Buffer during the ongoing transmission.

**Workaround**

Do not use transmit cancellation for CAN FD messages with more than eight data bytes.

Alternatively wait for the duration of the expected transmission time of the canceled TX Buffer before writing new data to that TX Buffer.

**Affected Silicon Revisions**

| A | D | F | | | | | |
|---|---|---|---|---|---|---|---|
| X | X | X | | | | | |

## 2.5 Clock Failure Detector (CFD)

### 2.5.1 CFD with XOSC/XOSC32K Oscillator

When the CFD is enabled for the XOSC/XOSC32K oscillator and the oscillator input signal is stuck at 1, the clock failure detection works correctly but the switch to the safe clock will fail.

**Workarounds**

Two possible workarounds are as follows:
1. If the main clock source comes from the XOSC/XOSC32K oscillator, the only workaround is indirect (i.e., using the WDT in firmware and switch to safe clock source in firmware at WDT reset).
2. Because the clock failure detection is functional, once the STATUS.CLKFAIL is set, and if the STATUS.CLKSW is not set, manually switch to safe clock from firmware by changing the configurations of the Generic Clock Generators that use the XOSC/XOSC32K oscillator as a clock source to use another source clock instead.

**Affected Silicon Revisions**

| A | D | F | | | | | |
|---|---|---|---|---|---|---|---|
| X | | | | | | | |

### 2.5.2 XOSC Ready Bit not Cleared

When the XOSC Clock Failure Detector is enabled (XOSCCTRL.CFDEN = 1) and a failure is detected (STATUS.XOSCFAIL = 1), the XOSC Ready bit is not cleared (STATUS.XOSCRDY = 1).

**Workaround**

STATUS.XOSCFAIL must always be checked before STATUS.XOSCRDY, and STATUS.XOSCRDY must always be ignored when STATUS.XOSCFAIL = 1.

**Affected Silicon Revisions**

| A | D | F | | | | | |
|---|---|---|---|---|---|---|---|
| X | X | X | | | | | |

### 2.5.3 False Clock Failure Detection

Disabling the Clock Failure Detector (XOSCCTRL.CFDEN = 0) and re-enabling it (XOSCCTRL.CFDEN = 1) when the XOSC is enabled (XOSCCTRL.ENABLE = 1), can lead to a false Clock Failure Detection.

**Workaround**

Follow these steps to re-enable the Clock Failure Detector:

1. Disable the XOSC (XOSCCTRL.ENABLE = 0).
2. Disable the Clock Failure Detector (XOSCCTRL.CFDEN = 0).
3. Re-enable the Clock Failure Detector (XOSCCTRL.CFDEN = 1).
4. Re-enable the XOSC (XOSCCTRL.ENABLE = 1).

**Affected Silicon Revisions**

| A | D | F | | | | | |
|---|---|---|---|---|---|---|---|
| X | X | X | | | | | |

### 2.5.4 False Clock Failure Detection

Disabling the Clock Failure Detector (CFDCTRL.CFDEN = 0) and re-enabling it (CFDCTRL.CFDEN = 1) when the XOSC32K is enabled (XOSC32K.ENABLE = 1), can lead to a false Clock Failure Detection.

**Workaround**

Follow these steps to re-enable the Clock Failure Detector:

1. Disable the XOSC32K (XOSC32K.ENABLE = 0).
2. Disable the Clock Failure Detector (CFDCTRL.CFDEN = 0).
3. Re-enable the Clock Failure Detector (CFDCTRL.CFDEN = 1).
4. Re-enable the XOSC32K (XOSC32K.ENABLE = 1).

**Affected Silicon Revisions**

| A | D | F | | | | | |
|---|---|---|---|---|---|---|---|
| X | X | X | | | | | |

## 2.6 Device

### 2.6.1 Reverse Current in VDDIOB Domain

For the device with 100-pin, 120-pin, and 128-pin counts when VDDIOB is supplied with the voltage less than VDDIO - 0.7V, reverse current in VDDIOB cluster is observed.

**Workaround**

None. Pin PB13 must be tied to ground.

**Affected Silicon Revisions**

| A | D | F | | | | | |
|---|---|---|---|---|---|---|---|
| X | | | | | | | |

## 2.6.2 Internal Pull-up on the RESET Pin

The internal pull-up of the RESET pin is not functional.

**Workaround**

An external 100K pull-up must be added on the RESET pin.

**Affected Silicon Revisions**

| A | D | F | | | | | |
|---|---|---|---|---|---|---|---|
| X | | | | | | | |

## 2.6.3 Detection of a Debugger Probe

The detection of a debugger probe could fail if the "BOD33 Disable" fuse is cleared (i.e., BOD33 is enabled).

**Workaround**

To secure the detection of debugger probes, enable BOD33 using the SUPC.BOD33 register instead of the "BOD33 Disable" fuse. The "BOD33 Disable" fuse must be kept set.

**Affected Silicon Revisions**

| A | D | F | | | | | |
|---|---|---|---|---|---|---|---|
| X | X | | | | | | |

## 2.6.4 VBAT Mode

$V_{BAT}$ mode is not functional.

**Workaround**

None.

**Affected Silicon Revisions**

| A | D | F | | | | | |
|---|---|---|---|---|---|---|---|
| X | | | | | | | |

## 2.6.5 Internal Reference

When the internal reference is used with the DAC and ADC, their outputs become non-linear when the operating temperature is less than 0°C.

**Workaround**

The internal reference must be used only for positive temperatures (i.e., above 0°C).

**Affected Silicon Revisions**

| A | D | F | | | | | |
|---|---|---|---|---|---|---|---|
| X | | | | | | | |

### 2.6.6 Device Operation for Temperature < -20°C

If the operating temperature is less than -20°C, the device does not start.

**Workaround**

Apply an external reset pulse at power-up when $V_{DD}$ is higher than 2V, or keep reset line low while $V_{DD}$ is lower than 2V.

**Affected Silicon Revisions**

| Device | A | D | F | | | | |
|---|---|---|---|---|---|---|---|
| Package Grade U with EFP | - | | | | | | |
| Package Grade U without EFP | X | X | X | | | | |
| Other Package Grades | X | | | | | | |

**Note:** EFP refers to Extended Flash Performance and is only available for package grade U = -40°C to +85°C Matte Sn Plating (Industrial). For additional information, refer to the device data sheet.

### 2.6.7 Overconsumption in Standby

An overconsumption can happen when entering in Standby Sleep mode when the following peripherals are enabled (CTRLA.ENABLE = 1) with run in Standby disabled (CTRLA.RUNSTDBY = 0):

- DFLL48M
- RTC
- TC
- TCC
- ADC
- PDEC
- SERCOM

**Workaround**

Disable the concerned peripherals when entering in Standby Sleep mode.

**Affected Silicon Revisions**

| A | D | F | | | | |
|---|---|---|---|---|---|---|
| X | X | X | | | | |

### 2.6.8 VDDANA Analog Cluster

Any and all I/O as well as digital alternate functions on VDDANA analog cluster must be confined as inputs only. Refer to the "Table 6-34. GPIO Clusters" for the list per package of pins powered by VDDANA.

**Note:** The IOSET configurations for the concerned digital alternate output functions must be considered (refer to "6.2.8 IOSET Configurations").

**Workaround**

None.

**Affected Silicon Revisions**

| A | D | F | | | | |
|---|---|---|---|---|---|---|
| X | X | X | | | | |

### 2.6.9 Standby Low-Power Mode

Standby Low-Power mode is not supported and should not be used in new designs.

**Workaround**

The Idle Low-Power mode must be considered if Hibernate or Backup Sleep modes are not an option.

Idle Sleep mode must be tuned by applying low-power techniques like waiting for any peripheral pending transactions to complete and switching on a slow clock source before entering the Low-Power mode.

**Affected Silicon Revisions**

| A | D | F | | | | |
|---|---|---|---|---|---|---|
| X | X | | | | | |

## 2.7 Device Service Unit (DSU)

### 2.7.1 CRC32

The DSU CRC32 will not complete when targeting NVM memory space while the NVM cache is disabled.

**Workaround**

Be sure to always enable the NVM cache when performing a DSU CRC32 request targeting the NVM memory space.

**Affected Silicon Revisions**

| A | D | F | | | | |
|---|---|---|---|---|---|---|
| X | X | X | | | | |

### 2.7.2 Coresight

During Coresight discovery (that allows a debugger to identify the available on-chip debug resources), the TPIU and ETB ROM table content (containing component and device IDs) read as 0. Debugger may conclude that TPIU and ETB are unavailable and indicate that trace is not available.

**Workaround**

None.

**Affected Silicon Revisions**

| A | D | F | | | | |
|---|---|---|---|---|---|---|
| X | X | X | | | | |

## 2.8 48 MHz Digital Frequency-Locked Loop (DFLL48M)

### 2.8.1 COARSE or FINE Calibration Values During the Locking Sequence

If the DFLL48M reaches the maximum or minimum COARSE or FINE calibration values during the locking sequence, an out of bounds interrupt will be generated. These interrupts will be generated even if the final calibration values at DFLL48M lock are not at maximum or minimum, and might therefore be false out of bounds interrupts.

**Workaround**

Check that lock bits, DFLLLCKC and DFLLLCKF, in the OSCCTRL Interrupt Flag Status and Clear register (INTFLAG) are both set before enabling the DFLLOOB interrupt.

**Affected Silicon Revisions**

| A | D | F | | | | | |
|---|---|---|---|---|---|---|---|
| X | X | X | | | | | |

### 2.8.2    STATUS.DFLLRDY Bit in Close Loop Mode

In Close Loop mode, the STATUS.DFLLRDY bit does not rise before lock fine occurs. Therefore, the information about DFLL ready to start Close Loop mode is not available.

**Workaround**

None.

**Affected Silicon Revisions**

| A | D | F | | | | | |
|---|---|---|---|---|---|---|---|
| X | X | X | | | | | |

### 2.8.3    DFLLVAL.FINE Value When DFLL48M Re-enabled

If the DFLL is disabled and then re-enabled, the DFLLVAL.FINE value is ignored by the DFLL module, which will then start its lock fine process at another frequency.

**Workaround**

Before writing the final configuration in the DFLLCTRLB register, the DFLL module must be re-enabled in Open Loop mode to read and rewrite the DFLLVAL register.

1. `OSCCTRL->DFLLMUL.reg = X; // Write new DFLLMULL configuration`
2. `OSCCTRL.DFLLCTRLB.reg = 0; // Select Open loop configuration`
3. `OSCCTRL.DFLLCTRLA.bit.ENABLE = 1; // Enable DFLL`
4. `OSCCTRL.DFLLVAL.reg = OSCCTRL->DFLLVAL.reg; // Reload DFLLVAL register`
5. `OSCCTRL.DFLLCTRLB.reg = X; // Write final DFLL configuration`

**Affected Silicon Revisions**

| A | D | F | | | | | |
|---|---|---|---|---|---|---|---|
| X | | | | | | | |

### 2.8.4    Lose Lock After Wake (LLAW) Usage

When the Lose Lock After Wake (DFLLCTRLB.LLAW) is set, the DFLL may maintain lock (STATTUS.DFLLLOCK = 1) after the DFLL is disabled. If the DFLL lock (STATUS.DFLLLOCK = 1) is maintained when the DFLL is reconfigured and then enabled, some bits may not be properly set.

**Workaround**

When reconfiguring the DFLL wait for the lock status to set to '0' (STATUS.DFLLLOCK = 0) after disabling the DFLL (DFLLCTRLA.ENABLE = 0).

**Affected Silicon Revisions**

| A | D | F | | | | | |
|---|---|---|---|---|---|---|---|
| X | X | X | | | | | |

### 2.8.5    DFLL48M Status Flags

The STATUS.DFLLLCKF and STATUS.DFLLLCKC status bits are not automatically cleared when disabling the DFLL while it is running in Close Loop mode.

**Workaround**

Once the DFLL is disabled, clear the OSCCTRL.DFLLCTRLB.MODE bit to reset the lock bits of the DFLLSTATUS register.

**Affected Silicon Revisions**

| A | D | F | | | | | |
|---|---|---|---|---|---|---|---|
| X | X | X | | | | | |

### 2.8.6 DFLL48M Status Flags

DFLL48M Status flags may have unexpected values during the DFLL48 registers (DFLLCTRLA, DFLLCTRLB, DFLLMUL, DFLLVAL) configuration.

**Workaround**

Clear DFLL48M Status before and after enabling the DFLL48M (DFLLCTRLA.ENABLE = 1).

**Affected Silicon Revisions**

| A | D | F | | | | | |
|---|---|---|---|---|---|---|---|
| X | X | X | | | | | |

### 2.8.7 Lose Lock After Wake (LLAW) Usage

Changing Lose Lock After Wake (DFLLCTRLB.LLAW) when the DFLL is not completely stopped can produce a corruption of the closed loop controller and its lock status.

**Workaround**

The DFLLCTRLB.LLAW bit update must be done as follows:

1. Disable the DFLL (DFLLCTRLA.ENABLE = 0).
2. Wait for synchronization (DFLLSYNC.ENABLE = 0).
3. Wait for STATUS.DFLLRDY = 0.
4. Update the DFLLCTRLB.LLAW bit.

**Affected Silicon Revisions**

| A | D | F | | | | | |
|---|---|---|---|---|---|---|---|
| X | X | X | | | | | |

## 2.9 Digital-to-Analog Converter (DAC)

### 2.9.1 RESERVED

### 2.9.2 VDDANA as the DAC Reference

The selection of VDDANA as the DAC reference in DAC.CTRLB.REFSEL is non-functional.

**Workaround**

The VDDANA must be connected externally to a $V_{REF}$ pin and DAC.CTRLB.VREFAU must be selected.

**Affected Silicon Revisions**

| A | D | F | | | | | |
|:---:|:---:|:---:|:---:|:---:|:---:|:---:|:---:|
| X | | | | | | | |

### 2.9.3 DAC on Negative Input AIN3

No analog compare will be done on Comparator 1 (AC1) when using the DAC on negative input AIN3.

**Workaround**
Use the internal VDD scaler.

**Affected Silicon Revisions**

| A | D | F | | | | | |
|:---:|:---:|:---:|:---:|:---:|:---:|:---:|:---:|
| X | | | | | | | |

### 2.9.4 Interpolation Mode

If the Interpolation mode is enabled (with filter integrated to the DAC), the last data from the filter is missing, and therefore, the DAC final output value does not correspond to the DAC input value.

Although interrupt events are generated at the end of conversion (EOC), the EOC occurs before the final value from the filter and is of no use in the application.

**Workaround**
None.

**Affected Silicon Revisions**

| A | D | F | | | | | |
|:---:|:---:|:---:|:---:|:---:|:---:|:---:|:---:|
| X | X | X | | | | | |

### 2.9.5 Reference

The reference select of the DAC (CTRLB.REFSEL) will default to a '0' if the DAC Software Reset (CTRLA.SWRST) is used to reset the module.

**Workaround**
None.

**Affected Silicon Revisions**

| A | D | F | | | | | |
|:---:|:---:|:---:|:---:|:---:|:---:|:---:|:---:|
| X | X | X | | | | | |

### 2.9.6 First Conversion

When the internal bandgap reference (INTREF) is selected as reference voltage (CTRLB.REFSEL = 0x3), the DAC Startup Ready bits value (STATUS.READY0, STATUS.READY1) is not correct for the first DAC Conversion after device power-up or after wake-up from Standby Low-Power mode.

**Workaround**
Disregard STATUS.READY0 and STATUS.READY1 bits for the first DAC conversion and check instead that the Data Buffer 0/1 Empty bits are set (INTFLAG.EMPTY0 = 1, INTFLAG.EMPTY1 = 1), as this process also checks the DAC readiness exhaustively. It will ensure the DAC is ready for the first conversion after device power-up or after wake-up from Standby Low-Power mode.

**Affected Silicon Revisions**

| A | D | F | | | | | |
|---|---|---|---|---|---|---|---|
| X | X | X | | | | | |

### 2.9.7 Refresh Mode

The DAC Conversion Refresh mode is not functional.

**Workaround**

A conversion must be started at least every 10 µs to guarantee DAC performances specification.

**Affected Silicon Revisions**

| A | D | F | | | | | |
|---|---|---|---|---|---|---|---|
| X | X | X | | | | | |

## 2.10 Direct Memory Access Controller (DMAC)

### 2.10.1 Linked Descriptors

When at least one channel using linked descriptors is already active, a channel Fetch Error (FERR) could occur on enabling a channel with no linked descriptor or the second descriptor (index 1) of the channel being enabled could be fetched by one of the already active channels using linked descriptors. These errors can occur when a channel is being enabled during the link request of another channel and if the channel number of the channel being enabled is lower than the channel already active.

**Workaround**

When enabling a channel while other channels using linked descriptors are already active, the channel number of the new channel to enable must be greater than the other channel numbers.

**Affected Silicon Revisions**

| A | D | F | | | | | |
|---|---|---|---|---|---|---|---|
| X | X | | | | | | |

### 2.10.2 Channel Priority

When using channels with different priority levels, the highest priority channel could stall at the end of its current block.

When this occurs, the channel is seen as active with BTCNT = 0 in the ACTIVE register with Busy and Pending flag set in the CHSTATUSn register. This condition also prevents the other channels from executing.

**Workaround**

None.

**Affected Silicon Revisions**

| A | D | F | | | | | |
|---|---|---|---|---|---|---|---|
| X | | | | | | | |

### 2.10.3 DMAC in Debug Mode

In Debug mode, DMAC does not restart after a debug halt when DBGCTRL.DBGRUN = 0.

**Workaround**

Set DBGCTRL.DBGRUN to 1 so that the DMAC continues normal operation when the CPU is halted by an external debugger.

**Affected Silicon Revisions**

| A | D | F | | | | | |
|---|---|---|---|---|---|---|---|
| X | | | | | | | |

## 2.11 Ethernet MAC (GMAC)

### 2.11.1 Ethernet Functionality in 64-pin Packages

Ethernet functionality in 64-pin packages is not available.

**Workaround**

None.

**Affected Silicon Revisions**

| A | D | F | | | | | |
|---|---|---|---|---|---|---|---|
| X | | | | | | | |

## 2.12 External Interrupt Controller (EIC)

### 2.12.1 Edge Detection

When enabling EIC, SYNCBUSY.ENABLE is released before EIC is fully enabled. Edge detection can be done only after three cycles of the selected GCLK (GCLK_EIC or CLK_ULP32K).

**Workaround**

None.

**Affected Silicon Revisions**

| A | D | F | | | | | |
|---|---|---|---|---|---|---|---|
| X | X | X | | | | | |

### 2.12.2 Asynchronous Edge Detection

When the asynchronous edge detection is enabled and the system is in Standby mode, only the first edge will be detected. The following edges are ignored until the system wakes up.

**Workaround**

Use the asynchronous edge detection with debouncer enabled. It is recommended to set the DPRESCALER.PRESCALER and DPRESCALER.TICKON to have the lowest frequency possible. To reduce the power consumption, set the EIC GCLK frequency as low as possible or select the ULP32K clock (EIC CTRLA.CKSEL set).

**Affected Silicon Revisions**

| A | D | F | | | | | |
|---|---|---|---|---|---|---|---|
| X | X | X | | | | | |

## 2.13 Fractional Digital Phase-Locked Loop (FDPLL)

### 2.13.1 Input Clock on FDPLLn

FDPLL unlocks could occur while the output frequency is stable.

**Workaround**

Enable the lock bypass (OSCCTRL.DPLLCTRLB.LBYPASS = 1) and wake up fast (OSCCTRL.DPLLCTRLB.WUF = 1) to avoid losing FDPLL clock output during a false unlock status. The workaround does not avoid false unlock indications but it disables the gating of the FDPLL clock output by the lock status. Therefore, the clock is issued even if the FDPLL status shows unlocked. The Clock Ready bit (OSCCTRL.DPLLSTATUS.CLKRDY) can be monitored by the application to ensure activity is present on the FDPLLn output, but clock ready does not provide any indication of FDPLLn Lock nor frequency. A 10 ms delay is also suggested after the clock ready bit is set to allow the DPLL to achieve the target frequency.

**Pseudo Code**

Set OSCCTRL.DPLLCTRLB.WUF = 1 and OSCCTRL.DPLLCTRLB.LBYPASS = 1

Set DPLLCTRLA.ENABLE = 1

Wait (OSCCTRL.DPLLSTATUS.CLKRDY == 1)

Delay (10 ms)

Set Source for GCLK with DPLL

**Affected Silicon Revisions**

| A | D | F | | | | | |
|---|---|---|---|---|---|---|---|
| X | X | | | | | | |

### 2.13.2 FDPLL Ratio in DPLLnRATIO

When changing the FDPLL ratio in DPLLnRATIO register on-the-fly, STATUS.DPLLnLDRTO will not be set when the ratio update will be completed.

**Workaround**

Wait for the interruption flag INTFLAG.DPLLnLDRTO instead.

**Affected Silicon Revisions**

| A | D | F | | | | | |
|---|---|---|---|---|---|---|---|
| X | X | X | | | | | |

## 2.14 Non-Volatile Memory Controller (NVMCTRL)

### 2.14.1 NVM Read Corruption

NVM reads could be corrupted when mixing NVM reads with Page Buffer writes.

**Workaround**

Disable cache lines before writing to the Page Buffer when executing from NVM or reading data from NVM while writing to the Page Buffer. Cache lines are disabled by writing a one to CTRLA.CACHEDIS0 and CTRLA.CACHEDIS1.

**Affected Silicon Revisions**

| A | D | F | | | | | |
|---|---|---|---|---|---|---|---|
| X | X | | | | | | |

## 2.14.2 SmartEEPROM Buffered Mode is not Recommended

SmartEEPROM Buffered write mode benefits in terms of wear leveling and timings come with strong restrictions. The SmartEEPROM address space must be written linearly, and no read must be issued to the SmartEEPROM Page (SEEP) under modification. As those restrictions are difficult to implement (because they heavily depends on application: for instance, the application must ensure that no host in the system accesses this space) and effects on wear leveling and timings are difficult to measure and are not predictable, it is recommended not to use the SmartEEPROM buffered write mode.

**Workaround**
None.

**Affected Silicon Revisions**

| A | D | F | | | | | |
|---|---|---|---|---|---|---|---|
| X | X | X | | | | | |

## 2.14.3 Debugger Illegal Accesses

Debugger illegal NVMCTRL address space read transactions return invalid data.

Debugger illegal NVMCTRL address space write transactions are silently ignored.

**Workaround**
None.

**Affected Silicon Revisions**

| A | D | F | | | | | |
|---|---|---|---|---|---|---|---|
| X | X | X | | | | | |

## 2.15 Peripheral Access Controller (PAC)

## 2.15.1 PAC Protection Error in FREQM

FREQM reads on the Control B register (FREQM.CTRLB) generate a PAC protection error.

**Workaround**
None.

**Affected Silicon Revisions**

| A | D | F | | | | | |
|---|---|---|---|---|---|---|---|
| X | X | X | | | | | |

### 2.15.2 PAC Protection Error in CCL

Writing the Software Reset bit in the Control A register (CTRLASWRST) will trigger a PAC protection error.

**Workaround**

Clear the CCL PAC error each time a CCL software reset is executed.

**Affected Silicon Revisions**

| A | D | F | | | | | |
|---|---|---|---|---|---|---|---|
| X | X | X | | | | | |

## 2.16 I/O Pin Controller (PORT)

### 2.16.1 PORT Read/Write Attempts on Non-Implemented Registers

PORT read/write attempts on non-implemented registers, including addresses beyond the last implemented register group (PA, PB,...), do not generate a PAC protection error.

**Workaround**

None.

**Affected Silicon Revisions**

| A | D | F | | | | | |
|---|---|---|---|---|---|---|---|
| X | X | X | | | | | |

### 2.16.2 PORT Pull-Up/Pull-Down Resistor

The pull-down on PA24/PA25 are activated during power-up and when Sleep mode is OFF. On all other pins, except those in the VSWOUT cluster, the pull-up is activated during power-up and when Sleep mode is OFF.

**Workaround**

None.

**Affected Silicon Revisions**

| A | D | F | | | | | |
|---|---|---|---|---|---|---|---|
| X | | | | | | | |

## 2.17 Real-Time Counter (RTC)

### 2.17.1 Write Corruption

A 8-bit or 16-bit write access for a 32-bit register, or 8-bit write access for a 16-bit register can fail for the following registers:
- COUNT register in COUNT32 mode
- COUNT register in COUNT16 mode
- CLOCK register in CLOCK mode

**Workaround**

Write the registers with:

- A 32-bit write access for COUNT register in COUNT32 mode, CLOCK register in CLOCK mode
- A 16-bit write access for the COUNT register in COUNT16 mode

**Affected Silicon Revisions**

| A | D | F | | | | | |
|---|---|---|---|---|---|---|---|
| X | X | X | | | | | |

### 2.17.2   COUNTSYNC

When CTRLA.COUNTSYNC is enabled, the first COUNT value is not correctly synchronized and thus it is a wrong value.

**Workaround**

After enabling COUNTSYNC, read the COUNT register until its value is changed when compared to its first value read. After this, all consequent value read from the COUNT register is valid.

**Affected Silicon Revisions**

| A | D | F | | | | | |
|---|---|---|---|---|---|---|---|
| X | X | X | | | | | |

### 2.17.3   Tamper Input Filter

Majority debouncing, as part of RTC tamper detection, does not work when enabled by setting the Debouncer Majority Enable bit, CTRLB.DEBMAJ.

**Workaround**
None.

**Affected Silicon Revisions**

| A | D | F | | | | | |
|---|---|---|---|---|---|---|---|
| X | X | X | | | | | |

### 2.17.4   Tamper Detection

Upon enabling the RTC tamper detection feature, a false tamper detection can be reported by the RTC.

**Workarounds**
Use any one of the following workarounds:

- **Workaround 1**: Configure TAMPER detection as ONLY falling edge.
- **Workaround 2**: If the user software has to use TAMPER detection as rising edge, it must ignore the tamper interrupts generated after enabling the RTC tamper detection, and until 10 RTC clock periods.

**Affected Silicon Revisions**

| A | D | F | | | | | |
|---|---|---|---|---|---|---|---|
| X | X | X | | | | | |

### 2.17.5   Tamper Detection Timestamp

If an external reset occurs during a tamper detection, the TIMESTAMP register will not be updated when next tamper detection is triggered.

**Workarounds**

Enable RTC tamper interrupt and copy the timestamp from the RTC CLOCK register to one of the following destinations:

- SRAM
- GPx registers in RTC
- BKUPx registers in RTC

**Affected Silicon Revisions**

| A | D | F | | | | | |
|---|---|---|---|---|---|---|---|
| X | X | X | | | | | |

## 2.17.6 Prescaler

When the tamper or debouncing features (TAMPCTRL) are enabled, periodic interrupts and events are generated when the prescaler is OFF (CTRLA.PRESCALER = 0).

**Workaround**

When the prescaler is OFF (CTRLA.PRESCALER = 0), clear the Periodic Interval n Event Output Enable bits (EVCTRL.PEREOn = 0 [n = 7...0]) and respective Periodic Interval n Interrupt Enable (INTENCLR.PERn = 1 [n = 7...0]) bits.

**Affected Silicon Revisions**

| A | D | F | | | | | |
|---|---|---|---|---|---|---|---|
| X | X | X | | | | | |

## 2.17.7 Tamper Detection Timestamp

The INTFLAG.TAMPER bit is not reset by reading the TIMESTAMP register.

**Workaround**

Clear the INTFLAG.TAMPER bit by writing a '1' to this bit when the Timestamp value has been read from the TIMESTAMP register.

**Affected Silicon Revisions**

| A | D | F | | | | | |
|---|---|---|---|---|---|---|---|
| X | X | X | | | | | |

## 2.17.8 General Purpose Registers

General Purpose Registers n (GPn) are reset on tamper detection even if GPTRST = 0.

**Workaround**

None.

**Affected Silicon Revisions**

| A | D | F | | | | | |
|---|---|---|---|---|---|---|---|
| X | X | X | | | | | |

## 2.17.9 Battery Backup Mode

Entering Battery Backup mode without waiting for SYNCBUSY.ENABLE and SYNCBUSY.COUNTSYNC synchronization completion may freeze the status of these bits.

**Workaround**

Ensure that both SYNCBUSY.ENABLE and SYNCBUSY.COUNTSYNC synchronization is completed (SYNCBUSY.ENABLE = 0 and SYNCBUSY.COUNTSYNC = 0) before enabling Battery Backup mode (refer to the section "Entering Battery Backup Mode" in the product data sheet).

**Affected Silicon Revisions**

| A | D | F | | | | | |
|---|---|---|---|---|---|---|---|
| X | X | X | | | | | |

## 2.17.10 Active Layer Protection

When the RTC is configured in Active Layer Protection mode (TAMPCTRL.INACT = 0x3), and the RTC CTRLA.ENABLE bit is not set, a tamper can be detected and a timestamp captured. The TAMPID register and the INTFLAG.TAMPER bit may not be set.

**Workaround**

When the RTC is configured in Active Layer Protection mode, after setting the CTRLA.ENABLE control bit, the user must wait for 10 RTC clock periods. Then the user must clear the TAMPID register, clear the INTFLAG.TAMPER bit and do a dummy read of the TIMESTAMP register to remove the lock condition on the TIMESTAMP register.

**Affected Silicon Revisions**

| A | D | F | | | | | |
|---|---|---|---|---|---|---|---|
| X | X | X | | | | | |

## 2.18 Serial Communication Interface (SERCOM)

### 2.18.1 SERCOM-USART: Auto-Baud Mode

In USART Auto-Baud mode, missing stop bits are not recognized as inconsistent sync (ISF) or framing (FERR) errors.

**Workaround**

None.

**Affected Silicon Revisions**

| A | D | F | | | | | |
|---|---|---|---|---|---|---|---|
| X | X | X | | | | | |

### 2.18.2 SERCOM-USART: Collision Detection

In USART operating mode with Collision Detection enabled (CTRLB.COLDEN = 1), the SERCOM will not abort the current transfer as expected if a collision is detected and if the SERCOM APB clock is lower than the SERCOM generic clock.

**Workaround**

The SERCOM APB clock must always be higher than the SERCOM generic clock to support collision detection.

**Affected Silicon Revisions**

| A | D | F | | | | | |
|---|---|---|---|---|---|---|---|
| X | X | X | | | | | |

### 2.18.3 SERCOM-USART: Debug Mode

In USART operating mode, if DBGCTRL.DBGSTOP = 1, data transmission is not halted after entering Debug mode.

**Workaround**
None.

**Affected Silicon Revisions**

| A | D | F | | | | | |
|---|---|---|---|---|---|---|---|
| X | X | X | | | | | |

### 2.18.4 SERCOM-SPI: 32-bit Extension Mode

When 32-bit Extension mode is enabled and data to be sent is not in multiples of 4 bytes, which means the length counter must be enabled, and additional bytes will be sent over the line.

**Workarounds**
Use any one of the following workarounds:
1. Write the Inter-Character Spacing bits (CTRLC.ICSPACE) to a non-zero-value.
2. Do not use length counter in firmware by keeping the data to be sent is in multiples of 4 bytes.

**Affected Silicon Revisions**

| A | D | F | | | | | |
|---|---|---|---|---|---|---|---|
| X | X | X | | | | | |

### 2.18.5 SERCOM-UART: TXINV and RXINV Bits

The TXINV and RXINV bits in the CTRLA register have inverted functionality.

**Workaround**
In software interpret the TXINV bit as a functionality of RXINV, and conversely, interpret the RXINV bit as a functionality of TXINV.

**Affected Silicon Revisions**

| A | D | F | | | | | |
|---|---|---|---|---|---|---|---|
| X | X | X | | | | | |

### 2.18.6 SERCOM-I$^2$C: SDAHOLD Timing

SDAHOLD timing of the SERCOM-I$^2$C does not match the value shown in the current device data sheet. The following table shows the specified and real values of SDA Hold timing.

**Table 2-1. SDA Hold Timing**

| SDA Hold Time Value | Specified SDA Hold Time | Real SDA Hold Time |
|---|---|---|
| 0x0 | Disabled | Disabled |
| 0x1 | 50 ns to 100 ns | 20 ns to 40 ns |
| 0x2 | 300 ns to 600 ns | 100 ns to 250 ns |
| 0x3 | 400 ns to 800 ns | 150 ns to 350 ns |

**Workaround**
None.

**Affected Silicon Revisions**

| A | D | F | | | | | |
|---|---|---|---|---|---|---|---|
| X | X | X | | | | | |

## 2.18.7 SERCOM-I$^2$C: Repeated Start in High-Speed Host Write Operation

For High-Speed Host Write operations, writing CTRLB.CMD = 0x1 issues a STOP command instead of a Repeated Start making repeated start not possible in that mode.

**Workaround**
None.

**Affected Silicon Revisions**

| A | D | F | | | | | |
|---|---|---|---|---|---|---|---|
| X | X | X | | | | | |

## 2.18.8 SERCOM-I$^2$C: Repeated Start in High-Speed Host Read Operation

For High-Speed Host Read operations, sending a NACK (CTRLB.CMD = 0x2) forces a STOP to be issued making repeated start not possible in that mode.

**Workaround**
None.

**Affected Silicon Revisions**

| A | D | F | | | | | |
|---|---|---|---|---|---|---|---|
| X | X | X | | | | | |

## 2.18.9 SERCOM-I$^2$C: STATUS.CLKHOLD Bit in Host and Client Modes

The STATUS.CLKHOLD bit in host and client modes can be written whereas it is a read-only status bit.

**Workaround**
Do not clear STATUS.CLKHOLD bit to preserve the current clock hold state.

**Affected Silicon Revisions**

| A | D | F | | | | | |
|---|---|---|---|---|---|---|---|
| X | X | X | | | | | |

## 2.18.10 SERCOM-I$^2$C: I$^2$C in Client Mode

In I$^2$C mode, LENERR, SEXTOUT, LOWTOUT, COLL and BUSERR bits are not cleared when INTFLAG.AMATCH is cleared.

**Workaround**
Manually clear status bits LENERR, SEXTOUT, LOWTOUT, COLL and BUSERR by writing these bits to 1 when set.

**Affected Silicon Revisions**

| A | D | F | | | | | |
|---|---|---|---|---|---|---|---|
| X | X | X | | | | | |

## 2.18.11 SERCOM-I²C: Client Mode with DMA

In I²C Client Transmitter mode, at the reception of a NACK, if there is still data to be sent in the DMA buffer, the DMA will push a data to the DATA register. Because a NACK was received, the transfer on the I²C bus will not occur causing the loss of this data.

### Workaround
Configure the DMA transfer size to the number of data to be received by the I²C host. DMA cannot be used if the number of data to be received by the host is not known.

### Affected Silicon Revisions

| A | D | F | | | | | |
|---|---|---|---|---|---|---|---|
| X | X | X | | | | | |

## 2.18.12 SERCOM-I²C: I²C Client in DATA32B Mode

When SERCOM is configured as an I²C client in 32-bit Data Mode (DATA32B = 1) and the I²C host reads from the I²C client (client transmitter) and outputs its NACK (indicating no more data is needed), the I²C client still receives a DRDY interrupt.

If the CPU does not write a new data to the I²C client DATA register, I²C client will pull SDA line, which will result in stalling the bus permanently.

### Workarounds
1. Write a dummy data to data register when a NACK is received from the host.
2. Use command #2 (SERCOMx->I2CS.CTRLB.bit.CMD = 2) when a NACK is received from the host.

> **Important:** Because STATUS.RXNACK always indicates the last received ACK, to determine when a NACK is received from the I²C host, the I²C client software needs to consider I2CS.STATUS.RXNACK only on the second DRDY interrupt after receiving the AMATCH interrupt.

### Affected Silicon Revisions

| A | D | F | | | | | |
|---|---|---|---|---|---|---|---|
| X | X | X | | | | | |

## 2.18.13 SERCOM-I²C: 10-bit Addressing Mode

10-bit addressing in I²C Client mode is not functional.

### Workaround
None.

### Affected Silicon Revisions

| A | D | F | | | | | |
|---|---|---|---|---|---|---|---|
| X | X | X | | | | | |

## 2.18.14 SERCOM-I²C: Repeated Start

When the Quick command is enabled (CTRLB.QCEN = 1), software can issue a repeated Start by writing either CTRLB.CMD or ADDR.ADDR bit fields. If in these conditions, SCL Stretch Mode is CTRLA.SCLSM = 1, a bus error will be generated.

**Workaround**
Use Quick Command mode (CTRLB.QCEN = 1) only if SCL Stretch Mode is CTRLA.SCLSM = 0.

**Affected Silicon Revisions**

| A | D | F | | | | | |
|---|---|---|---|---|---|---|---|
| X | X | X | | | | | |

## 2.18.15  SERCOM-SPI: Data Preload

In SPI Client mode with Client Data Preload Enabled (CTRLB.PLOADEN = 1), the client transmitter may discard some data if the host cannot keep the SPI Select pin low until the end of transmission.

**Workaround**
In SPI Client mode, the SPI Select pin ($\overline{SS}$) must be kept low by the host until the end of the transmission if the Client Data Preload feature is used (CTRLB.PLOADEN = 1).

**Affected Silicon Revisions**

| A | D | F | | | | | |
|---|---|---|---|---|---|---|---|
| X | X | X | | | | | |

## 2.18.16  SERCOM I²C: Repeated Start

For Host Write operations (excluding High-Speed mode), in 10-bit addressing mode, writing CTRLB.CMD = 0x1 does not issue a Repeated Start command correctly.

**Workaround**
Write the same 10-bit address with the same direction bit to the ADDR.ADDR register to generate properly a Repeated Start.

**Affected Silicon Revisions**

| A | D | F | | | | | |
|---|---|---|---|---|---|---|---|
| X | X | X | | | | | |

## 2.18.17  SERCOM-USART: Wakeup

The USART does not wake-up the device on Error Interrupt (INTFLAG.ERROR = 1).

**Workaround**
Configure the USART to wake-up the device on the RX Complete Interrupt (INTENSET.RXC = 1) in order to check the PERR/FERR status (STATUS.PERR = 1 or STATUS.FERR = 1).

**Affected Silicon Revisions**

| A | D | F | | | | | |
|---|---|---|---|---|---|---|---|
| X | X | X | | | | | |

## 2.18.18  SERCOM-USART: LENGTH

When the USART is used in 32-bit mode with hardware handshaking (CTS/RTS), the TXC interrupt flag (INTFLAG.TXC) may be set before transmission has completed. The TXC interrupt flag may incorrectly be set regardless of Data Length Enable (LENGTH.LENEN) is set to '0' or '1'.

**Workaround**
None.

**Affected Silicon Revisions**

| A | D | F | | | | | |
|---|---|---|---|---|---|---|---|
| X | X | X | | | | | |

## 2.18.19 SERCOM-USART: Overconsumption in Standby mode

When SERCOM USART CTRLA.RUNSTDBY= 0 and the Receiver is disabled (CTRLB.RXEN= 0), the clock request to the GCLK generator feeding the SERCOM will stay asserted during Standby mode, leading to unexpected over-consumption.

**Workaround**
Configure CTRLA.RXPO and CTRLA.TXPO in order to use the same SERCOM PAD for RX and TX or add an external pull-up on the RX pin.

**Affected Silicon Revisions**

| A | D | F | | | | | |
|---|---|---|---|---|---|---|---|
| X | X | X | | | | | |

## 2.18.20 SERCOM-USART, SERCOM-SPI: Wake-up Interrupt

The Data Register Empty (DRE) wake-up interrupt is not de-asserted when the register interrupt is cleared (INTFLAG.DRE = 0).

The issue occurs if the DRE interrupt is enabled (INTSET.DRE = 1) when the device enters in Standby Sleep mode.

**Workaround**
Do not enable DRE interrupt (INTSET.DRE = 1) before entering in Standby Sleep mode.

**Affected Silicon Revisions**

| A | D | F | | | | | |
|---|---|---|---|---|---|---|---|
| X | X | X | | | | | |

## 2.18.21 SERCOM-SPI: SPI Data Preload

Preloading a new SPI data (CTRLB.PLOADEN = 1) before going into Standby Sleep mode, may lead to extra power consumption.

**Workaround**
None.

**Affected Silicon Revisions**

| A | D | F | | | | | |
|---|---|---|---|---|---|---|---|
| X | X | X | | | | | |

## 2.18.22 SERCOM-SPI: Hardware SPI Select Control

When Hardware SPI Select Control is enabled (CTRLB.MSSEN = 1), the SPI Select ($\overline{SS}$) pin goes high after each byte transfer even if a new data is ready to be sent.

**Workaround**
Set CTRLB.MSSEN = 0 and handle the SPI Select ($\overline{SS}$) pin by software.

**Affected Silicon Revisions**

| A | D | F | | | | | |
|---|---|---|---|---|---|---|---|
| X | X | X | | | | | |

### 2.18.23 SERCOM-I2C: Automatic Acknowledge

The I$^2$C Client Automatic Acknowledge feature (CTRLB.AACKEN = 1) is not supported when doing a repeated start.

**Workaround**
Do not use the AACKEN feature, implement a AMATCH handler instead.

**Affected Silicon Revisions**

| A | D | F | | | | | |
|---|---|---|---|---|---|---|---|
| X | X | X | | | | | |

### 2.18.24 SERCOM-I2C: No Wakeup upon Unexpected STOP

When an unexpected STOP occurs on the I$^2$C bus, the STATUS.BUSERR and INTFLAG.ERROR bits are set but may not wake the system from Sleep mode. An unexpected START will not produce this issue.

**Workaround**
None.

**Affected Silicon Revisions**

| A | D | F | | | | | |
|---|---|---|---|---|---|---|---|
| X | X | X | | | | | |

### 2.18.25 Software Reset

Software Reset (CTRLA.SWRST = 1) is not functional when the SERCOM is not enabled (CTRAL.ENABLE = 0).

**Workaround**
None.

**Affected Silicon Revisions**

| A | D | F | | | | | |
|---|---|---|---|---|---|---|---|
| X | X | X | | | | | |

## 2.19 Supply Controller (SUPC)

### 2.19.1 Buck Converter Mode

Buck Converter mode is not supported when using PLLs. As a result, the information given in Table 54-9 "Active Current Consumption - Active Mode" data for Buck converter mode with FDPLL and DFLL configurations is not valid and must be disregarded.

**Workaround**
Use the LDO Regulator mode when using FDPLL and DFLL configurations.

**Affected Silicon Revisions**

| A | D | F | | | | | |
|---|---|---|---|---|---|---|---|
| X | X | X | | | | | |

### 2.19.2 BOD33 Hysteresis

The hysteresis feature of the 3.3V BOD is not functional while the device is in STANDBY sleep mode.

**Workaround**
None.

**Affected Silicon Revisions**

| A | D | F | | | | | |
|---|---|---|---|---|---|---|---|
| X | X | X | | | | | |

## 2.20 Timer/Counter (TC)

### 2.20.1 PERBUF/CCBUFx Register

When clearing the STATUS.PERBUFV/STATUS.CCBUFx flag, the SYNCBUSY flag is released before the PERBUF/CCBUFx register is restored to its appropriate value.

**Workaround**
Successively clear the STATUS.PERBUFV/STATUS.CCBUFx flag twice to ensure that the PERBUF/CCBUFx register value is restored before updating it.

**Affected Silicon Revisions**

| A | D | F | | | | | |
|---|---|---|---|---|---|---|---|
| X | X | X | | | | | |

### 2.20.2 Retrigger

If a Retrigger event (EVCTRL.EVACTn = 0x1, RETRIGGER) occurs at the Channel Compare Match [n] time, the next Waveform Output [n] is corrupted.

**Workaround**
Use two channels to store their two successive (n and n+1) CC register values and combine their related waveform outputs to make signal redundancy.

**Affected Silicon Revisions**

| A | D | F | | | | | |
|---|---|---|---|---|---|---|---|
| X | X | X | | | | | |

### 2.20.3 PER register (8-bit mode)

In 8-bit mode, the PER register updates using the DMA are not possible in Standby mode.

**Workaround**
None.

**Affected Silicon Revisions**

| A | D | F | | | | | |
|---|---|---|---|---|---|---|---|
| X | X | X | | | | | |

## 2.21 Timer/Counter for Control Applications (TCC)

### 2.21.1 TCC with EVSYS in SYNC/RESYNC Mode

TCC peripheral is not compatible with an EVSYS channel in SYNC or RESYNC mode.

**Workaround**

Use TCC with an EVSYS channel in ASYNC mode.

**Affected Silicon Revisions**

| A | D | F | | | | | |
|---|---|---|---|---|---|---|---|
| X | X | X | | | | | |

### 2.21.2 Dithering Mode with External Retrigger Events

Using TCC in Dithering mode with external retrigger events can lead to an unexpected stretch of right-aligned pulses, or shrink of left-aligned pulses.

**Workaround**

Do not use retrigger events or actions when the TCC module is configured in Dithering mode.

**Affected Silicon Revisions**

| A | D | F | | | | | |
|---|---|---|---|---|---|---|---|
| X | X | X | | | | | |

### 2.21.3 ALOCK Feature

The ALOCK feature is not functional.

**Workaround**

None.

**Affected Silicon Revisions**

| A | D | F | | | | | |
|---|---|---|---|---|---|---|---|
| X | X | X | | | | | |

### 2.21.4 LUPD feature in Down-Counting Mode

In Down-Counting mode, the Lock Update bit (CTRLB.LUPD) does not protect against a PER register update from the PERBUF register.

**Workaround**

None.

**Affected Silicon Revisions**

| A | D | F | | | | | |
|---|---|---|---|---|---|---|---|
| X | X | X | | | | | |

### 2.21.5 Re-trigger in RAMP2 Operations

Re-trigger in RAMP2 operations (RAMP2, RAMP2A, RAMP2C, RAMP2CS) is not supported if a prescaler is used (CTRLA.PRESCALER ! = 0) and the re-trigger of the counter is done on the next GCLK (CTRLA.PRESCSYNC = GCLK or CTRLA.PRESCSYNC = RESYNC).

**Workaround**
Configure the re-trigger of the counter on the next prescaler clock (CTRLA.PRESCSYNC = PRESC).

**Affected Silicon Revisions**

| A | D | F | | | | | |
|---|---|---|---|---|---|---|---|
| X | X | X | | | | | |

### 2.21.6 Re-trigger

If a Re-trigger event (EVCTRL.EVACTn = 0x1, RETRIGGER) occurs at the Channel Compare Match [n] time, the next Waveform Output [n] is corrupted.

**Workaround**
Use two channels to store their two successive (n and n+1) CC register values and combine their related waveform outputs to make signal redundancy.

**Affected Silicon Revisions**

| A | D | F | | | | | |
|---|---|---|---|---|---|---|---|
| X | X | X | | | | | |

### 2.21.7 RAMP2 Operations

Timer/Counter Counting-down mode (CTRLBCLR.DIR = CTRLBSET.DIR = 1) is not supported in RAMP2 operations (RAMP2, RAMP2A, RAMP2C, RAMP2CS).

**Workaround**
Use Timer/Counter Counting-up mode (CTRLBCLR.DIR = CTRLBSET.DIR = 0).

**Affected Silicon Revisions**

| A | D | F | | | | | |
|---|---|---|---|---|---|---|---|
| X | X | X | | | | | |

### 2.21.8 Dithering Mode

Retrigger in RAMP2 operations is not supported in Dithering mode.

**Workaround**
None.

**Affected Silicon Revisions**

| A | D | F | | | | | |
|---|---|---|---|---|---|---|---|
| X | X | X | | | | | |

### 2.21.9 STATUS Register Access

8-bit or 16-bit writes to the STATUS register are forbidden.

**Workaround**
None.

**Affected Silicon Revisions**

| A | D | F | | | | | |
|---|---|---|---|---|---|---|---|
| X | X | X | | | | | |

### 2.21.10 Sequence State

The TCC Counter Overflow (OVF) DMA Trigger in DMA One-Shot Trigger Mode (CTRLA.DMAOS = 1) is not functional for Critical RAMP2C and RAMP2CS operation modes.

**Workaround**
None.

**Affected Silicon Revisions**

| A | D | F | | | | | |
|---|---|---|---|---|---|---|---|
| X | X | X | | | | | |

## 2.22 Position Decoder (PDEC)

### 2.22.1 Reserved

### 2.22.2 Angular and Revolution Counters

With index input enabled, that is EVCTRL.EVEI[2] and operating in X4/X2 mode, angular and revolution counters are incremented/decremented by two separate and unsynchronized sources (phases and index). This can lead to generating erroneous MC0 and MC1 events.

**Workaround**
If the application use case permits, operate PDEC in X4S/X2S mode by setting CTRLA.CONF[2:0] = 0b001/ 0b011. In this mode, the revolution counter is incremented/decremented by a single source, that is angular counter overflow/underflow.

If the application use case restricts operation in X4/X2 mode, then disable index input event, that is EVCTRL.EVEI[2] = 0. This ensures that revolution counter is incremented/decremented by a single source, that is angular counter overflow/underflow. First occurrence of the index pulse can be detected using an external interrupt input and angular counter value can be reset in the corresponding interrupt service routine.

**Affected Silicon Revisions**

| A | D | F | | | | | |
|---|---|---|---|---|---|---|---|
| X | X | X | | | | | |

### 2.22.3 Counter Operating Mode

Counting Events (EVCTRL.EVACT = 0x2) is not functional in COUNTER operating mode (CTRLA.MODE = 0x2).

**Workaround**
None.

**Affected Silicon Revisions**

| A | D | F | | | | | |
|---|---|---|---|---|---|---|---|
| X | X | X | | | | | |

### 2.22.4 Counter Operating Mode

Start, restart, or retrigger on event (EVCTRL.EVACT = 0x1) is not functional in COUNTER operating mode (CTRLA.MODE = 0x2).

**Workaround**
None.

**Affected Silicon Revisions**

| A | D | F | | | | | |
|---|---|---|---|---|---|---|---|
| X | X | X | | | | | |

### 2.22.5 Direction Change

A direction change detection (INTFLAG.DIR = 1) updates the STATUS.DIR bit with a variable delay.

**Workaround**
Don't consider the STATUS.DIR bit status when using the INTFLAG.DIR bit.

**Affected Silicon Revisions**

| A | D | F | | | | | |
|---|---|---|---|---|---|---|---|
| X | X | X | | | | | |

### 2.22.6 Hall Mode

A Windows Error (WINERR) flag can be reported after a START command execution, or when leaving standby (with RUNSTDBY = 0).

**Workaround**
Ignore the Windows Error (WINERR) flag in Hall mode after a START command execution, or when leaving standby.

**Affected Silicon Revisions**

| A | D | F | | | | | |
|---|---|---|---|---|---|---|---|
| X | X | X | | | | | |

### 2.22.7 Hall Mode

In HALL mode, the WINERR Error interrupt (INTFLAG.WINERR = 1) can rise several times on a low-speed window error detection.

**Workaround**

Disable the WINERR (INTCLR.WINERR = 1) at first error detection, then re-enable it once the error root cause at the application level is solved.

**Affected Silicon Revisions**

| A | D | F | | | | | |
|---|---|---|---|---|---|---|---|
| X | X | X | | | | | |

### 2.22.8 Error Flags

An Error Detection (INTFLAG.ERR=1) updates the STATUS Error flags (HERR, WINERR, MPERR, IDXERR, QERR) with a variable delay.

**Workaround**

Poll the STATUS Error flags until one of these bits is set.

**Affected Silicon Revisions**

| A | D | F | | | | | |
|---|---|---|---|---|---|---|---|
| X | X | X | | | | | |

## 2.23 Voltage Reference System (VREF)

### 2.23.1 Temperature Sensor

Both internal temperature sensors, TSENSP and TSENSC, are not supported and should not be used.

**Workaround**

None.

**Affected Silicon Revisions**

| A | D | F | | | | | |
|---|---|---|---|---|---|---|---|
| X | X | X | | | | | |

## 2.24 Event System (EVSYS)

### 2.24.1 Synchronous Mode

In Synchronous mode, spurious overrun interrupts can be generated when the generic clock for a channel is always ON (CHANNEL.ONDEMAND = 0).

**Workaround**

Set Generic Clock on Demand feature by setting CHANNEL.ONDEMAND = 1.

**Affected Silicon Revisions**

| A | D | F | | | | | |
|---|---|---|---|---|---|---|---|
| X | X | X | | | | | |

### 2.24.2 Software

Software Events are not supported in Synchronous and Resynchronized modes.

**Workaround**

Use software events in Asynchronous mode.

**Affected Silicon Revisions**

| A | D | F | | | | | |
|---|---|---|---|---|---|---|---|
| X | X | X | | | | | |

### 2.24.3 Synchronous/Resynchronized Modes

In synchronous mode, including RESYNC mode, spurious event detections can be generated when accessing peripherals used in conjunction with the EVSYS.

**Workaround**

To avoid spurious EVSYS detections, EVSYS must be write protected by configuring the WRCTRL register in the PAC before being used.

**Affected Silicon Revisions**

| A | D | F | | | | | |
|---|---|---|---|---|---|---|---|
| X | X | X | | | | | |

## 2.25 True Random Number Generator (TRNG)

### 2.25.1 Over Consumption

When TRNG is disabled, some internal logic could continue to operate causing an over consumption.

**Workaround**

Disable the TRNG module twice:

- CTRLA.ENABLE = 0;
- CTRLA.ENABLE = 0;

**Affected Silicon Revisions**

| A | D | F | | | | | |
|---|---|---|---|---|---|---|---|
| X | X | X | | | | | |

## 2.26 OSC32KCTRL

### 2.26.1 Clock Switch Back Feature Limitation

If an application can recover the XOSC32K from a Clock Failure Detection, the application can switch back to the XOSC32K clock (CFDCTRL.SWBACK = 1).

Entering Low-Power Sleep mode is not possible if the clock switch back cannot complete due to a persistent failure.

**Workaround**

Disable the Clock Failure Detector (CFDCTRL.CFDEN = 0).

**Affected Silicon Revisions**

| A | D | F | | | | | |
|---|---|---|---|---|---|---|---|
| X | X | X | | | | | |

## 2.27 Oscillator Controller (OSCCTRL)

### 2.27.1 Clock Switch Back Feature Limitation

If an application can recover the XOSC from a Clock Failure Detection, the application can switch back to the XOSC clock using Clock Switch Back feature (XOSCCTRL.SWBEN = 1).

Entering Low-Power Sleep mode is not possible if the clock switch back cannot complete due to a persistent failure.

**Workaround**
Disable the Clock Failure Detector (XOSCCTRL.CFDEN = 0).

**Affected Silicon Revisions**

| A | D | F | | | | | |
|---|---|---|---|---|---|---|---|
| X | X | X | | | | | |

# 3. Data Sheet Clarifications

The following typographic corrections and clarifications are to be noted for the device data sheet (DS60001507**J**), and are showed in **BOLD** type:

## 3.1 I/O Pins Maximum Output Current Table 54-13

Table 54-13 has been updated to add a new column for backup pins in Normal mode.

**Table 3-1. I/O Pins Maximum Output Current**

| Symbol | Parameter | Conditions | Backup Pins in Backup Mode | Normal Mode (all IO pins) | Normal Mode (all IO except Backup pins) | Normal mode (Backup pins) | Units |
|---|---|---|---|---|---|---|---|
| | | | | DRVSTR = 0 | DRVSTR = 1 | DRVSTR = 1 | |
| $I_{OL}$ | Maximum Output low-level current | $1.71V <= V_{DD} < 3.0V$ | 0.005 | 0.5 | 3 | **3** | mA |
| | | $3.0V <= V_{DD} <= 3.63V$ | 0.01 | 2 | 8 | **8** | |
| $I_{OH}$ | Maximum Output high-level current | $1.71V <= V_{DD} < 3.0V$ | 0.005 | 0.5 | 3 | **2** | |
| | | $3.0V <= V_{DD} <= 3.63V$ | 0.01 | 2 | 8 | **6** | |

# 4.  Appendix A: Revision History

**Rev. P (08/2022)**

The following updates were implemented in this revision along with numerous typographical corrections:

- Updated the silicon revision throughout the document to F
- Deprecated DAC errata for Smoothing of the Output Signal in Differential Mode

The following errata were added in this revision:

- ADC: Internal Bandgap Reference 2.1.6
- CAN: Transmit Cancellation 2.4.14
- Device: Standby Mode 2.6.9
- DAC: Refresh Mode 2.9.7
- NVMCTRL: Debugger Illegal Accesses 2.14.3
- TCC: STATUS Register Access 2.21.9
- TCC: Sequence State 2.21.10
- EVSYS: Synchronous/Resynchronized Modes 2.24.3
- OSC32KCTRL: Clock Switch Back Feature Limitation 2.26.1
- OSCCTRL: Clock Switch Back Feature Limitation 2.27.1

The following Data Sheet Clarifications were added in this revision:

- I/O Pins Maximum Output Current Table 54-13

**Rev. N (02/2022)**

The following updates were implemented in this revision along with numerous typographical corrections:

- Updated the silicon revision throughout the document to E.

The following errata were added in this revision:

- CAN: Tx (Queue) Buffers 2.4.13
- Device: VDDANA Analog Cluster 2.6.8
- DSU: Coresight 2.7.2
- NVMCTRL: SMARTEEPROM Buffered Mode 2.14.2
- SERCOM: SERCOM-I2C Wakeup 2.18.24
- SERCOM: Software Reset 2.18.25

The following errata had wording updated:

- FDPLL: Low-Frequency Input Clock on FDPLLn 2.13.1

**Rev. M (06/2021)**

The following updates were implemented in this revision along with numerous typographical corrections:

- RTC: Tamper Detection 2.17.4 was updated with new Workaround information
- Terminology for "Master," and "Slave," was updated to "Host," and "Client" respectively. This change may not be reflected in all associated Microchip Documentation. For more information, contact a Microchip Representative.
- Added the following Errata:
    - CAN: Transmit Message Order Inversion
    - Device: Overconsumption in Standby 2.6.7
    - DFLL48M: Lose Lock After Wake Bit 2.8.7
    - RTC: Battery backup Mode 2.17.9
    - RTC: Active Layer Protection 2.17.10
    - SERCOM-I2C: Automatic Acknowledge
    - TC: PER Register (8-bit mode) 2.20.3
    - PDEC: Counter Operating Mode 2.22.3

- PDEC: Counter Operating Mode 2.22.4
- PDEC: Direction Change Different
- PDEC: Hall Mode
- PDEC: Hall Mode
- PDEC: Error Flags

**Rev. L (01/2021)**

The following errata had updates to their titles for clarification:

- SERCOM I2C: Repeated Start in High-Speed Master Write Operation
- SERCOM I2C: Repeated Start in High-Speed Master Write Operation
- SERCOM I2C: STATUS.CLKHOLD Bit in Master and Slave Modes
- SERCOM-USART: Wakeup
- SERCOM-USART: LENGTH
- SERCOM-USART: Overconsumption in Standby Mode

The following Errata were added in this revision:

- 2.2.3 AC: Standby Sleep Mode
- 2.2.4 AC: Debug Mode
- 2.4.7 CAN: Debug Message
- 2.4.8 CAN: Bus Errors
- 2.4.9 CAN: On Demand
- 2.4.10 CAN: Debug Mode
- 2.4.11 CAN: Debug Mode
- 2.5.2 CFD: Ready Bit Not Cleared
- 2.5.3 CFD: False Clock Failure Detection
- 2.5.4 CFD: False Clock Failure Detection
- 2.8.5 DFLL48M: DFLL48M Status Flags
- 2.8.6 DFLL48M: DFLL48M Status Flags
- 2.9.6 DAC: First Conversion
- 2.17.7 RTC: Tamper Detection Timestamp
- 2.17.8 RTC: General Purpose Registers
- 2.18.20 SERCOM: Wake-up Interrupt
- 2.18.21 SERCOM-SPI: Slave Data Preload
- 2.18.22 SERCOM-SPI: Hardware Slave Select Control
- 2.20.2 TC: Retrigger
- 2.21.5 TCC: Re-trigger in RAMP2 Operations
- 2.21.6 TCC: Re-Trigger
- 2.21.7 TCC: RAMP2 Operations
- 2.21.8 TCC: Dithering Mode
- 2.22.2 PDEC: Angular and Revolution Counters
- 2.24.1 EVSYS: Synchronous Mode
- 2.24.2 EVSYS: Software
- 2.25.1 TRNG: Over consumption

**Rev. K (05/2020)**

The following Silicon Errata was removed as the issue does not exist:

- 2.22.1 X2 Mode

The following silicon errata were updated:

- 2.6.6 Device Operation for Temperature was updated with a table denoting those packages affected by the issue

The following silicon errata was added:

- 2.18.19 USART

Obsolete Data Sheet Clarifications were removed.

**Rev. J (11/2019)**
Added new silicon errata for Temperature Sensor.

**Rev. H (7/2019)**
The Silicon errata for Device Operation for Temperature was updated with text denoting which silicon versions it applies to.

**Rev. G (6/2019)**
The Errata Summary Table and The affected silicon revision tables in 2. Silicon Errata Issues have been updated to reflect the addition of EFP and Non-EFP silicon revisions.
The following Silicon issues were added:

- 2.1. Analog-to-Digital Converter (ADC):
  - DMA Sequencing
  - DMA Sequencing
- 2.2. Analog Comparator (AC): Output
- 2.8. 48 MHz Digital Frequency-Locked Loop (DFLL48M): LLAW
- 2.9. Digital-to-Analog Converter (DAC): Reference
- 2.17. Real-Time Counter (RTC): Prescaler
- 2.18. Serial Communication Interface (SERCOM):
  - SERCOM-USART: Wakeup
  - SERCOM-USART: Length

**Rev F. (2/2019)**
The following Silicon Issues were updated:

- FDPLL: Low-Frequency Input Clock on FDPLLn

The following Data Sheet Clarifications were added:

- Update to Initialization, Enabling, Disabling, and Resetting
- Update to Loop Divider Ratio Updates

**Rev. E (11/2018)**
The following silicon issues were added:

- SERCOM I$^2$C
  - SEERCOM I2C: Repeated Start
- CAN-FD
  - Messages Transmitted with Wrong Arbitration and Control Fields
  - DAR Mode
  - High-Priority Message (HPM) Interrupt
  - TX FIFO Message Sequence Inversion
- DMAC
  - Channel Priority
  - DMAC in Debug Mode
- RTC
  - COUNTSYNC
  - Tamper Input Filter
  - Tamper Detection
  - Tamper Detection Timestamp

- SUPC
  - BOD33 Hysteresis
- TCC
  - ALOCK Feature
  - LUPD Feature in Down-Counting Mode

The following Data Sheet Clarifications were added:
- Table 54-35 Flash Timing Characteristics was updated.
- BOD12 Register Information was updated.


**Rev. D (08/2018)**

The current device data sheet revision letter was updated.

The following silicon issues were added:

- Configurable Custom Logic (CCL):
  - Enable Protected Registers
  - Sequential Logic Reference
- Device:
  - Reverse Current in VDDIOB Domain
- SERCOM:
  - Repeated Start in High-Speed Master Write Operation
  - Repeated Start in High-Speed Master Read Operation
  - STATUS.CLKHOLD Bit in Master and Slave Modes
- Supply Controller (SUPC):
  - Buck Converter Mode
- TCC:
  - TCC with EVSYS in SYNC/RESYNC Mode


**Rev. C (04/2018)**

The current device data sheet revision letter was updated.

The following silicon issues were added:
- Analog-to-Digital Converter (ADC):
  - Reference Buffer Offset Compensation
- Peripheral Access Controller (PAC):
  - PAC Protection
  - PAC Protection
- Real-Time Counter (RTC):
  - Write Corruption
- SERCOM-I2C:
  - Slave Mode with DMA
  - I$^2$C Slave in DATA32B Mode
  - I$^2$C Slave Mode in 10-bit Address
  - Repeated Start
- SERCOM-SPI
  - Data Preload
- SERCOM-UART:
  - Collision Detection

All Data Sheet Clarifications were removed.


**Rev. B (10/2017)**

This revision includes the following additions:

Silicon Issues
- Ethernet Functionality in 64-pin Packages

Data Sheet Clarifications
- ADC Operating Conditions
- GMAC IEEE 802.3AZ Energy Efficient Support
- SERCOM Baud Rate Equations
- SERCOM in SPI Mode Timing
- TQFP 64-pin Package
- DAC Operating Conditions

**Rev. A (7/2017)**
Initial release of this document.

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