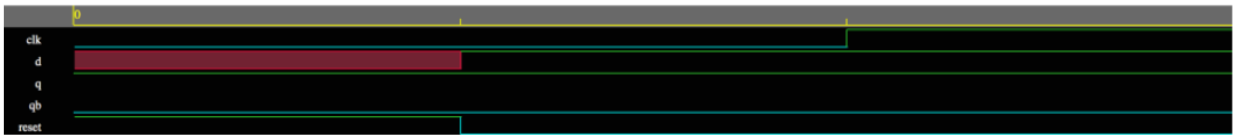
Lab 5

Deadline: 31 December 2023, 23:59 PM.

In this lab, you will build a system verilog module and its test bench in Edaplayground or Modelsim. I recommend you to use EDAplayground which can be accessed from www. Edaplayground.com . You need to create an account to use it. It is all free.

Lets say you are given the figure representing the waveforms of clk, d, q,qp, and reset signals after a system verilog module namely design.sv and its testbench namely testbench.sv are run.



Your task in this lab is to fill in the required parts of the design.sv and testbench.sv files. The required parts are stated using comments in these files. Submitting your work: Place all your design.sv and testbench.sv files in a SINGLE folder, name it as StudentName_ID_Lab5, compress it and upload to the LMS.