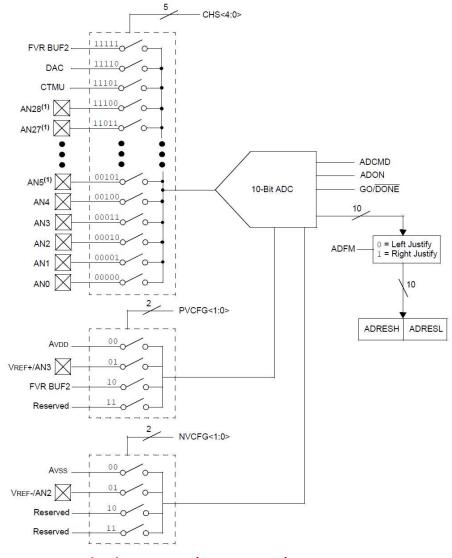


MICROCONTROLLERS LAB - ADC





- PIC 18F45K22 has 1 ADC
- Successive Approximation Register (SAR) ADC
- 32 multiplexed analog inputs
- Internal/External references
- Internal settable or External clocks
- 10 bit result
- End of conversion can trigger and interrupt event



Always read the datasheet before using ADC! Chap. 17 (pag. 288),

and revise its interrupt registers (PIR1, PIE1, IPR1)



Acquisition Chain



TACQ = Amplifier Settling Time + Hold Capacitor Charging Time + Temperature Coefficient = TAMP + TC + TCOFF $= 5\mu s + TC + [(Temperature - 25^{\circ}C)(0.05\mu s/^{\circ}C)] = 5\mu s + 1.20\mu s + [(50^{\circ}C - 25^{\circ}C)(0.05\mu s/^{\circ}C)]$ 3.5V- $= 7.45 \mu s$ $T_{CONV} = T_{ACOT} + 11T_{AD} + T_{CY}$ 3.0V 2.5V 2.0V 1.5V- $T_{ACQ} < T_{ACQT}$ 10 100 $T_{ADC} = 11 \cdot T_{AD}$ Rss $(k\Omega)$ ACQT[2:0] **Vref+** S/H Ain₀ Wait T_{CY} for discharge C_H **ADC** Vin [7:0] [9:8] **SAR** 10 bit 13,5pF Ain31 $1/T_{AD}$ **Vref-**CHS[4:0] **ADRES** ADCS[4:0] MUX NB F_{OSC} is MCU in Ide T_{CY} is $4/F_{OSC}$ $F_{OSC}/2$ $F_{OSC}/64$ F_{RC}

Time Diagram

FIGURE 17-3: A/D CONVERSION TAD CYCLES (ACQT<2:0> = 000, TACQ = 0)

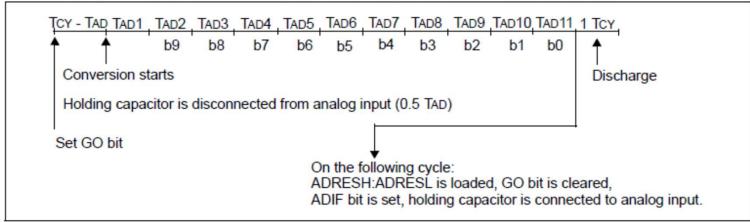
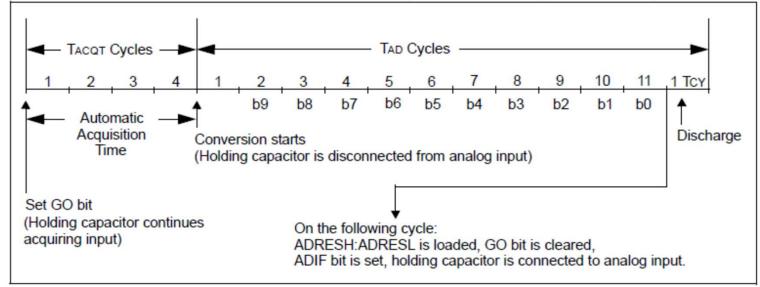


FIGURE 17-4: A/D CONVERSION TAD CYCLES (ACQT<2:0> = 010, TACQ = 4 TAD)



Settings



Set analog input

ADCON0.CHS<4:0>

Set TAD

ADCON2.ADCS<2:0>

Configure voltage references

ADCON1.PVCFG<1:0>

ADCON1.NVCFG<1:0>

Select ACQT

ADCON2.ACQT<2:0>

Set justification

ADCON2.ADFM

Turn on the ADC

ADCON0.ADON

Start A/D conversion

ADCON0.GO/DONE = 1

Interrupt/Polling

Interrupt PIR1.ADIF

Polling ADCON0.GO/DONE

- Stop A/D conversion (GO/DONE = 0)
- 10 bits result after Tconv

ADRESH

ADRESL

Registers

REGISTER 17-1: ADCON0: A/D CONTROL REGISTER 0

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
_			CHS<4:0>			GO/DONE	ADON
bit 7 bit 0							

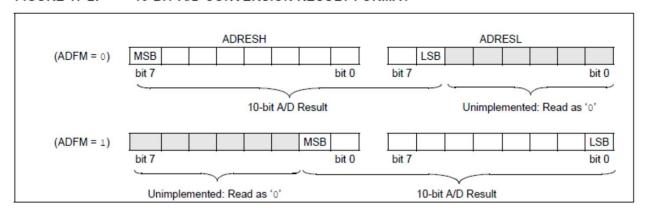
REGISTER 17-2: ADCON1: A/D CONTROL REGISTER 1

R/W-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
TRIGSEL	_	_	_	PVCFG<1:0>		NVCFG<1:0>	
bit 7							bit 0

REGISTER 17-3: ADCON2: A/D CONTROL REGISTER 2

R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
ADFM	_		ACQT<2:0>			ADCS<2:0>	
bit 7	-	•					bit 0

FIGURE 17-2: 10-BIT A/D CONVERSION RESULT FORMAT



Interrupt vs Polling



Interrupt

- ADC Interrupt Priority (IPR1.ADIP), not used
- Set ADC Interrupt Enable (PIE1.ADIE=1)
- Clear ADC Interrupt Flag (PIR1.ADIF=0)
- Enable Peripheral interrupt (INTCON.PEIE=1)
- Set Global Interrupt Enable (INTCON.GIE = 1)
- Wait interrupt in ISR
- Check ADC Interrupt Flag
- Clear ADC Interrupt Flag (PIR1.ADIF=0), exit ISR

Polling

Polling GO/DONE = 0