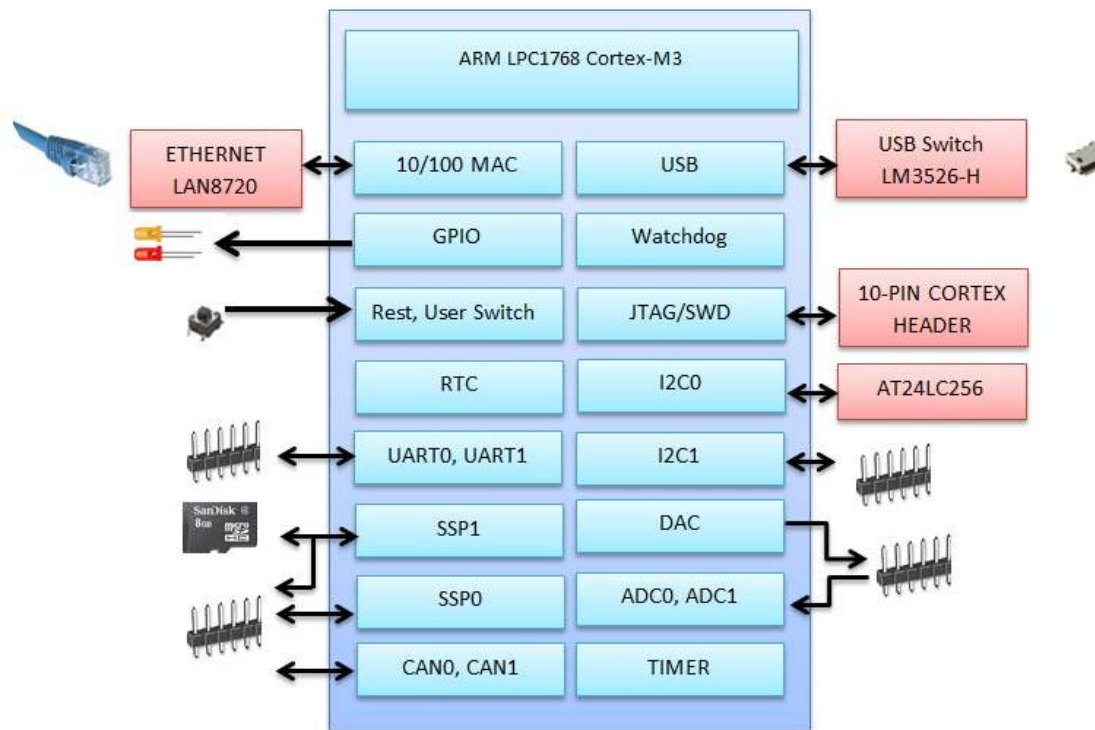


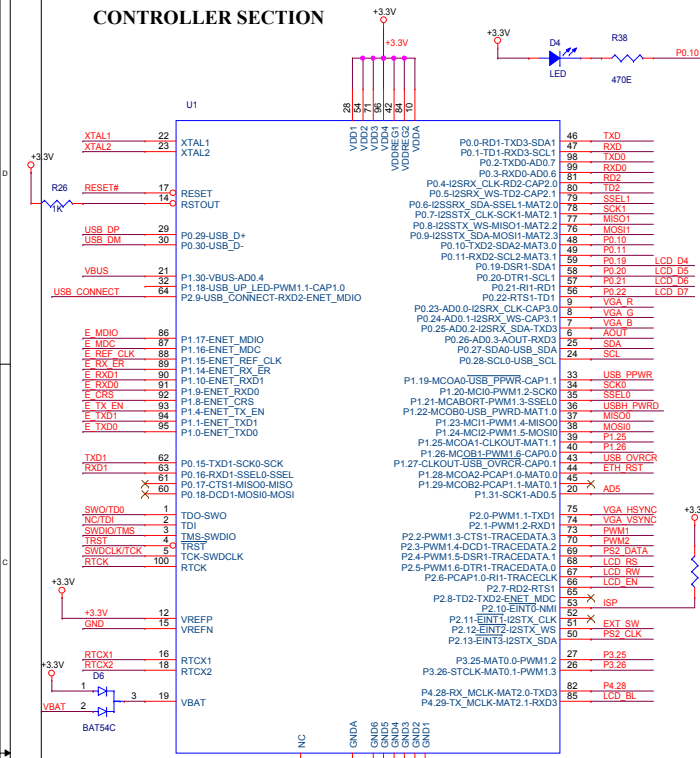
Design Overview



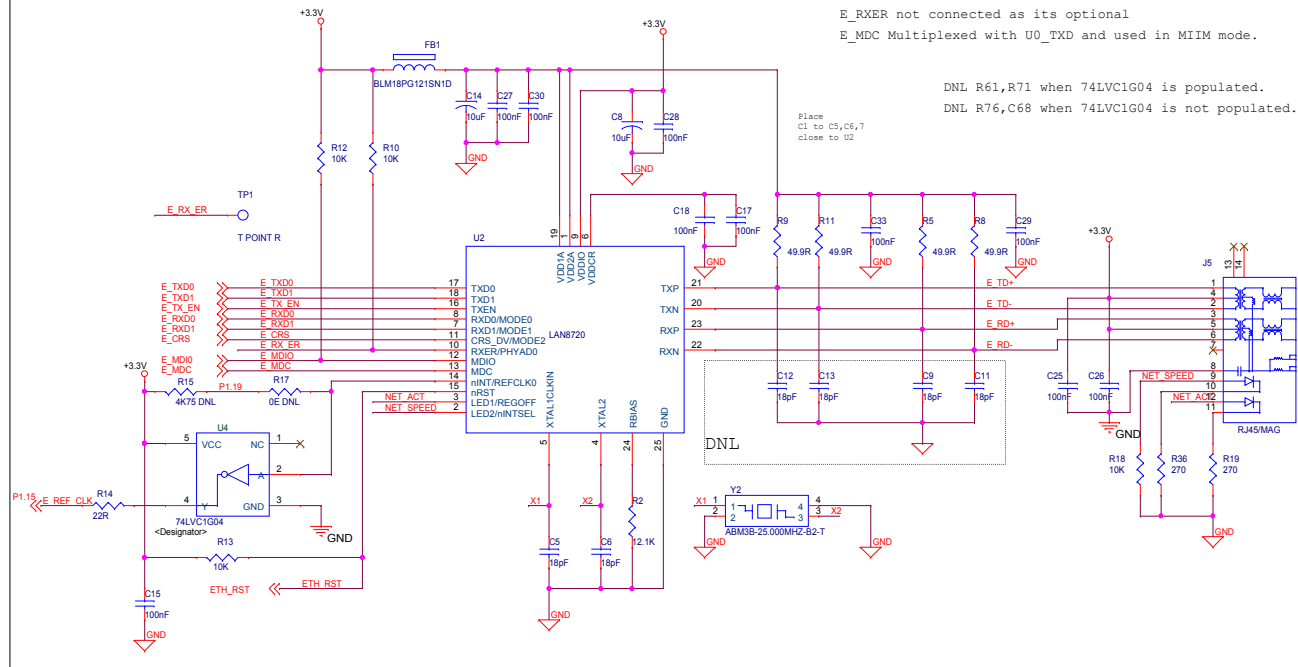
Disclaimer:

Schematic's are for reference only.
NGX Technologies Pvt. Ltd. provides no warranty for the use of
these schematics.

CONTROLLER SECTION



ETHERNET

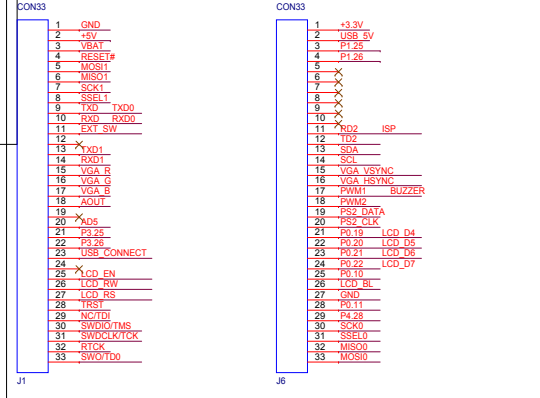


ETHERNET ROUTING GUIDELINES

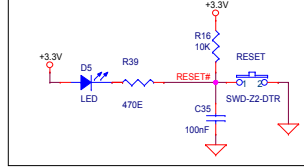
=>Keep the trace length difference between TX+ and TX- (or RX+ and RX-) in 700 mils.
 =>Keep RX+/- signal on the top layer, the RX+/- signal should avoid any vias, if possible. Avoid right angle signal trace.
 =>The crystal/oscillator clock and the switching noise from digital signals should be far away from TX+/-, RX+/- pairs.
 =>Keep TX, RX differential signals routing symmetric, equal length, and closely. The trace spacing between TX+ and TX- or between RX+ and RX- pair should be in 8 - 10 mils.
 =>The better spacing between TX+/- and RX+/- pairs should be larger than 200 mils.
 =>The trace length from LAN8720 to the transformer should not be longer than 5 inches, keep the trace as straight as possible, and keep it parallel for differential pairs.
 =>The termination resistors 49.90 and capacitors of TX+ and RX+ pairs should be placed near the transformer side and should be shorter than 400 mils.

E_RXER not connected as its optional
 E_MDC Multiplexed with U0_TXD and used in MIIM mode.
 DNL R61,R71 when 74LVC1G04 is populated.
 DNL R76,C68 when 74LVC1G04 is not populated.

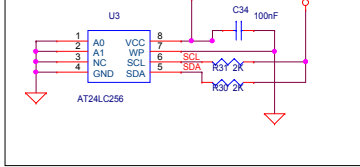
HEADERS



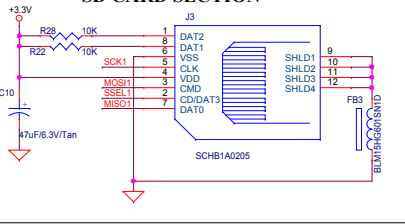
RESET SWITCH



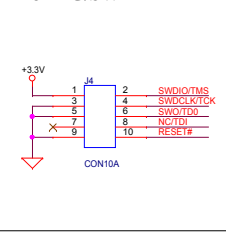
I2C



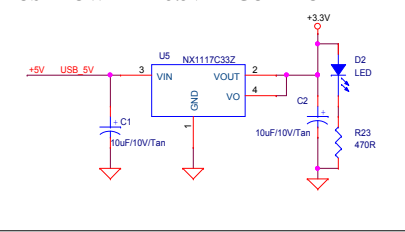
SD CARD SECTION



JTAG/SWD



USB POWERED 3.3V REGULATOR



USB SECTION

