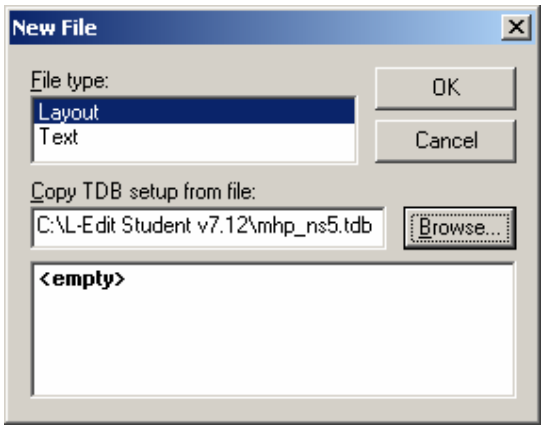
Layout Design Quick-Start Guide
(using Tanner Ledit student edition software)

Initial Setup

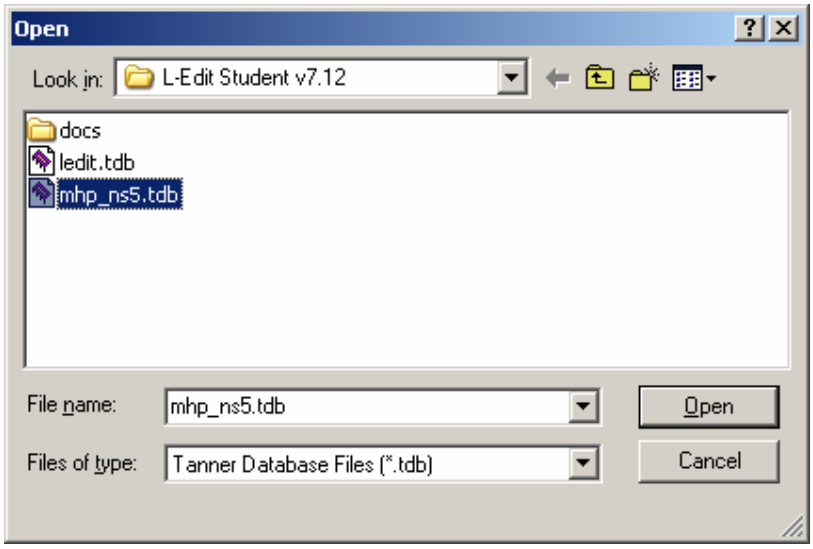
When starting a new layout design first create a new project database and than create one or more Cells.

Creating a new project database

From the menu choose: File -> New



Click on Browse to choose the appropriate technology file:

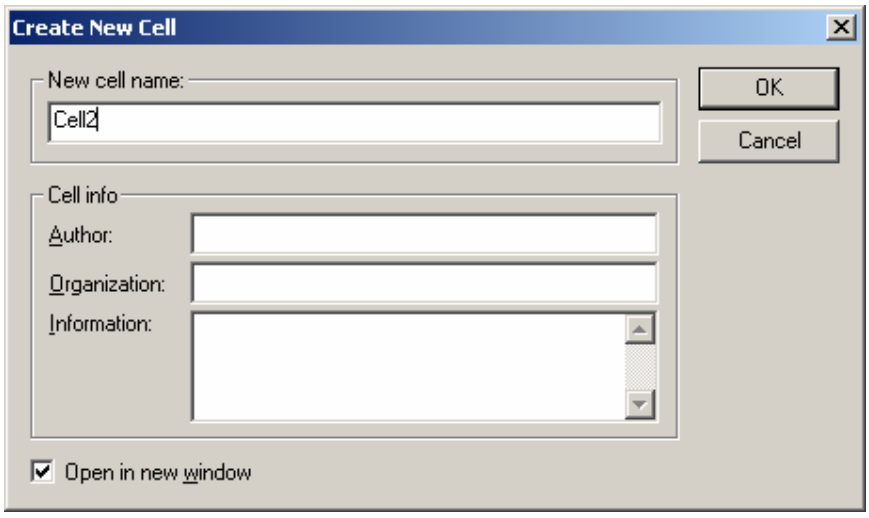


Select mhp_ns5.tdb

Click on Open than click on OK.

Creating a New Cell

From the menu choose: Cell -> New

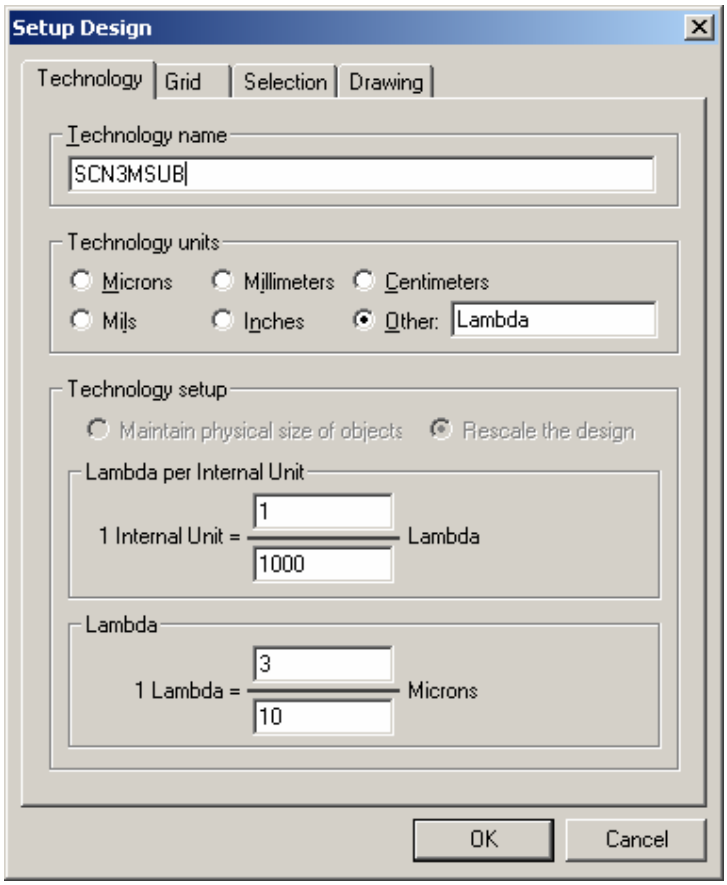


Type the new cell name and click on OK.

Setting up the Grid

The on-screen grid step should be set to 1 lambda and the mouse step to 0.5 lambda.

From the menu choose: Setup -> Design

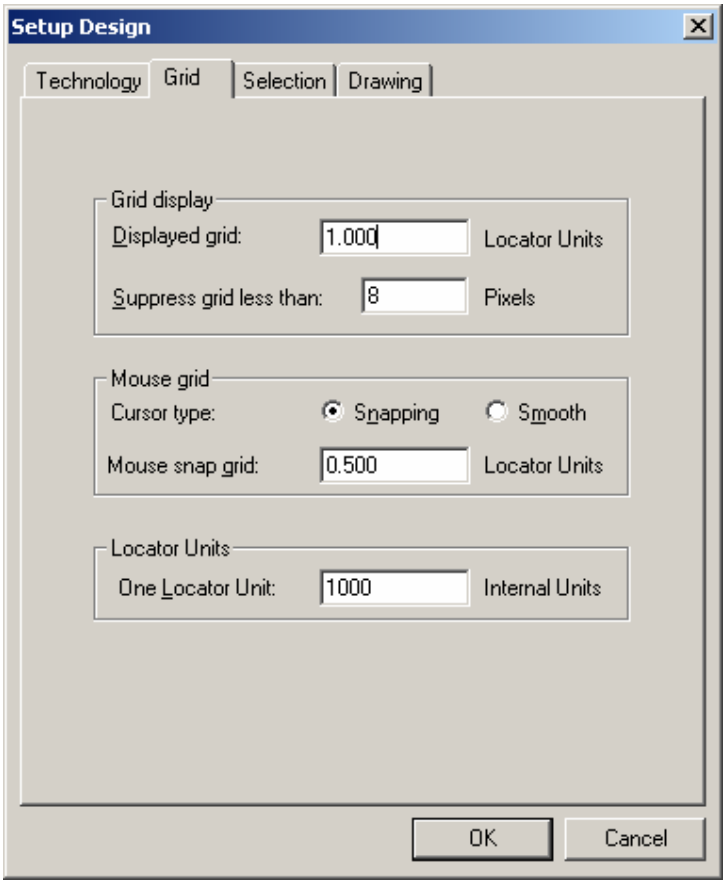


The screen shows the following important info:

- The technology name – SCN3MSUB

- The fact that technology is lambda based
- 1 lambda = 3/10 = 0.3 microns

Now click on the Grid tab.



The screen shows that:

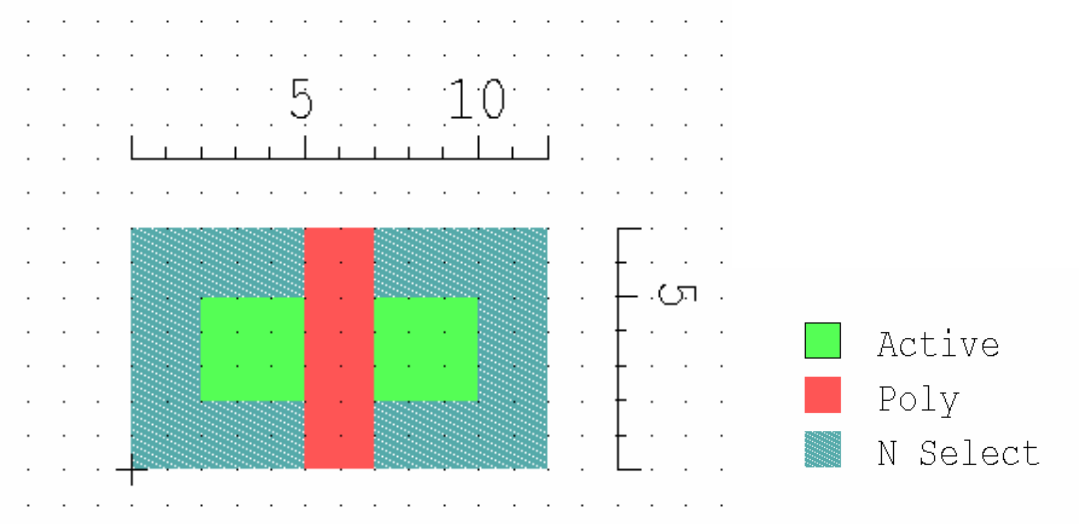
- The grid step is set to 1 lambda (in this technology setup one locator unit equals one lambda);
- The mouse will snap to 0.5 lambda

Example 1 – The Simplest MOS Transistor

In this example we will draw a minimum size (L=2 lambda, W=3 lambda) N-MOS transistor.

The Final Layout

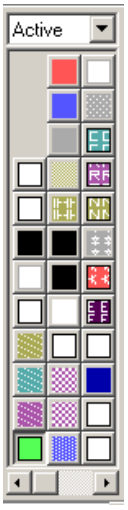
The final layout of the simplest NMOS transistor and the layers color codes are shown below:



Step-by-Step Instructions

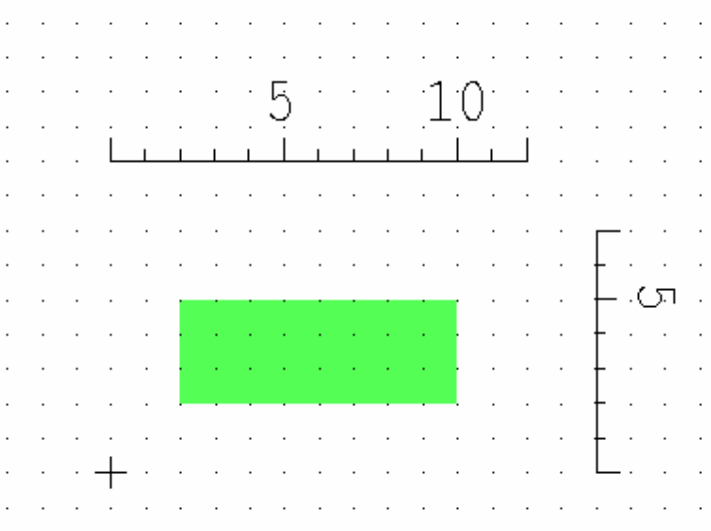
1. Active

Select the Active layer from the Layer's Palette



Choose the Box tool from the Drawing Toolbar.

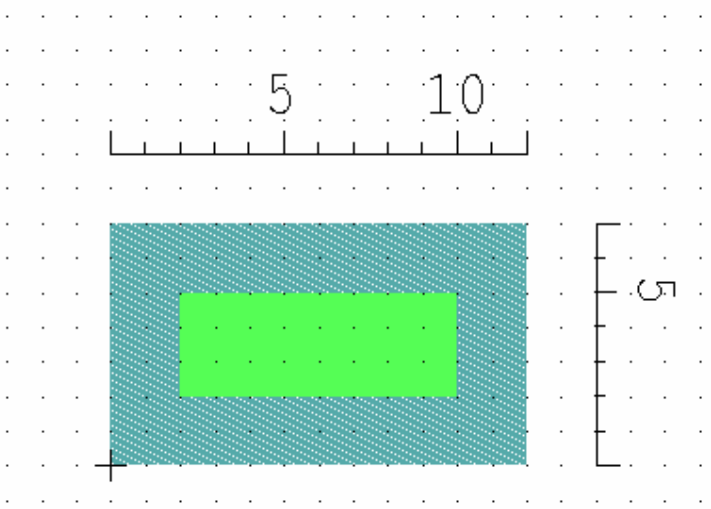
Now draw a 8lambda wide by 3 lambda high rectangle starting at coordinate 2,2 and finishing at 10,5.



2. N Select

Select the N Select layer from the Layer's Palette.

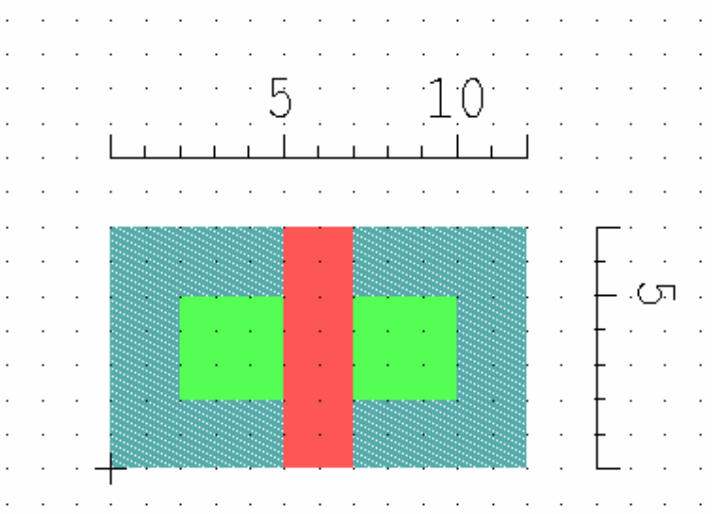
Draw a rectangle which surrounds the Active area and extends by 2lambda beyond the Active area borders.



3. Poly

Select the Poly layer from the Layer's Palette.

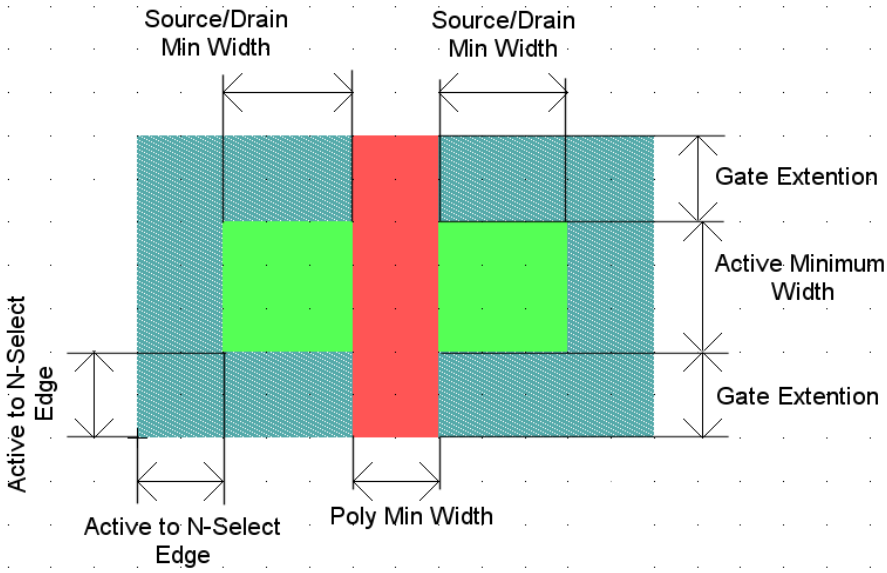
Draw a rectangle as shown on the figure:



Run a DRC check to verify that no errors were made.

This concludes the drawing of the smallest NMOS transistor.

How did we choose the layout dimensions?



The MOS transistor channel is defined by the Active and Poly overlap. The minimum channel size is L=2 lambda, W=3 lambda because of the following design rules:

- Active Minimum Width = 3 lambda
- Poly Minimum Width = 2 lambda

The size of the Drain and Source areas is restricted by:

- Source/Drain Width = 3 lambda

The Poly rectangle should extend out of active area according to:

- Gate Extension out of Active = 2 lambda

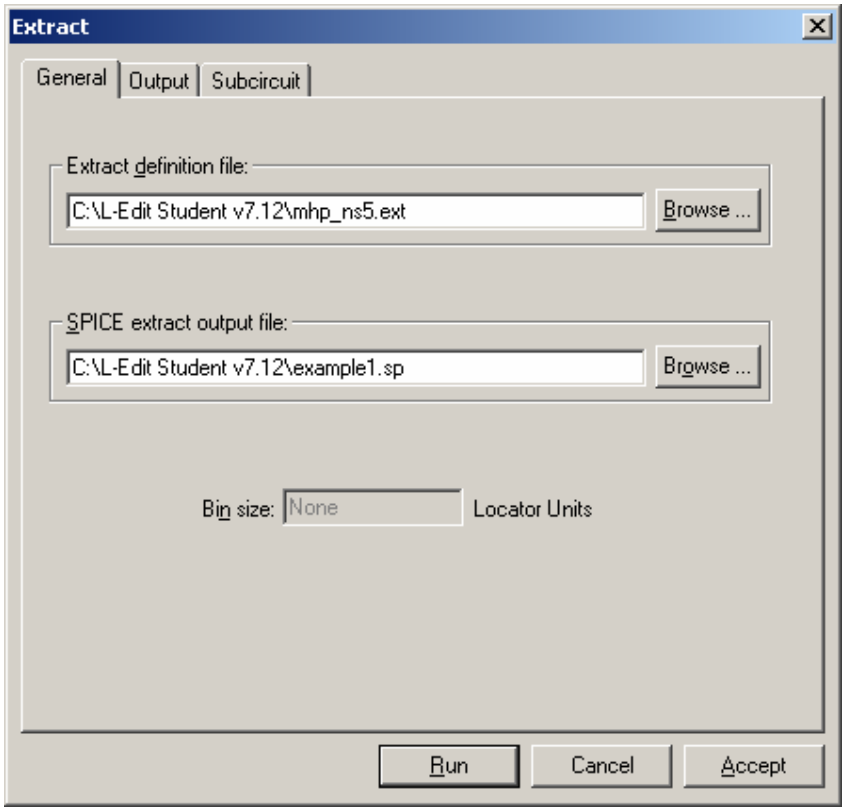
The N Select area dimensions are specified by:

- Active to N-Select Edge = 2 lambda

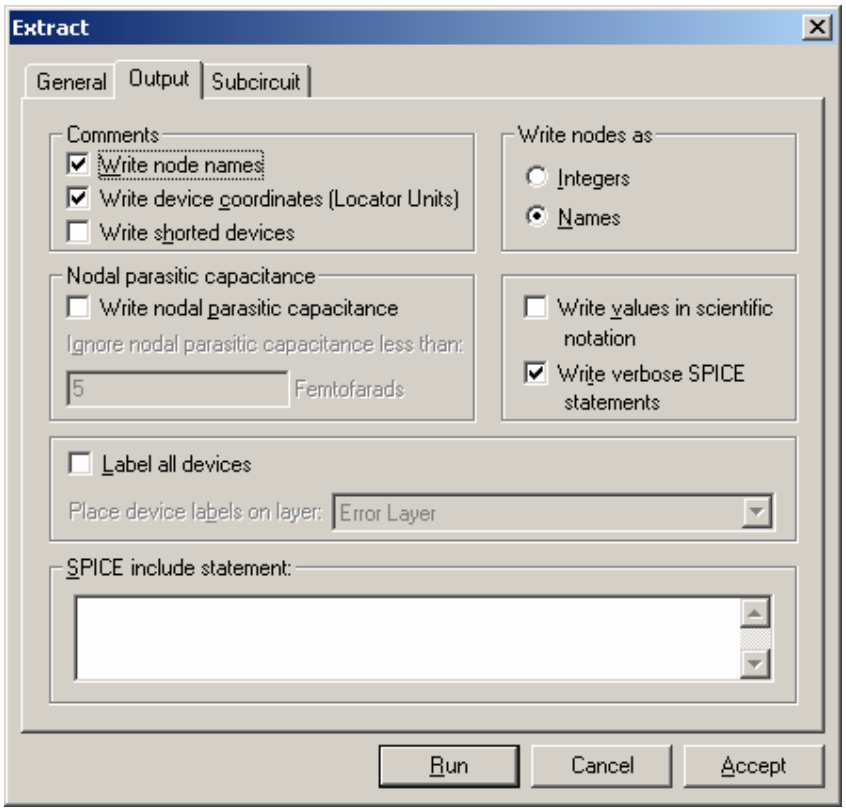
Circuit Extraction

Let's verify that our layout is actually a NMOS transistor. We will run the circuit extraction tool to create a SPICE netlist from our layout.

From the menu choose Tools -> Extract



Select mhp_ns5.ext as Extract definition file then click on the Output tab and make sure that the options are set as follows



Finally click on Run.

The resulting SPICE file is shown below:

```
* Circuit Extracted by Tanner Research's L-Edit V7.12 / Extract V4.00 ;
* TDB File:  C:\L-Edit Student v7.12\nmos, Cell:  nmosmin
* Extract Definition File:  C:\L-Edit Student v7.12\mhp_ns5.ext
* Extract Date and Time:  05/26/2004 - 19:23

* WARNING:  Layers with Unassigned AREA Capacitance.
*   <Poly Resistor>
*   <N Diff Resistor>
*   <P Diff Resistor>
*   <N Well Resistor>
* WARNING:  Layers with Unassigned FRINGE Capacitance.
*   <Pad Comment>
*   <Poly Resistor>
*   <N Diff Resistor>
*   <P Diff Resistor>
*   <N Well Resistor>
* WARNING:  Layers with Zero Resistance.
*   <Pad Comment>
*   <Cap-Well Capacitor>
*   <NMOS Capacitor>
*   <PMOS Capacitor>

* NODE NAME ALIASES


M1 2 3 4 1 NMOS L=0.6u W=0.9u AD=810f PD=3.6u AS=810f PS=3.6u
* M1 DRAIN GATE SOURCE BULK (5 2 7 5)

* Total Nodes: 4
* Total Elements: 1
* Extract Elapsed Time: 0 seconds
.END
```

The important lines are

```
M1 2 3 4 1 NMOS L=0.6u W=0.9u AD=810f PD=3.6u AS=810f PS=3.6u
* M1 DRAIN GATE SOURCE BULK (5 2 7 5)
```

This is the transistor we created! It has the expected dimensions - L=0.6u W=0.9u (the technology we are using has lambda =0.3 microns). And the gate is located at coordinates (5,2) – (7,5).

The lines that start with asterisk (*) are comments.