0.35 um CMOS C35 Design Rules

Seven Digit Document: ENG-183

Revision #: 2.0

Company Confidential

Table of Contents

1 Introduction

1.1 Revision

Change Status of Pages (including short description of change)

Rev. 1	Affected pages:	1 to44	(March 2002)
First version of design rule specification			

Rev. 2	Affected pages:	1 to 51	(February 2003)
Added thick metal module and process C35B4M3			

1.2 Process Family

This document is valid for the following 0.35um CMOS processes:

Process name	No. of masks	CMOS core module *	POLY1-POLY2 capacitor module **	5 Volt module	High resistive poly module	Metal 4 module	Thick Metal module	MET2-METC capacitor module
C35B3C0	14	x	x					
C35B3C1	17	x	x	x				
C35B4C3	20	x	x	x	x	x		
C35B4M3	21	x	x	x	x		x	x

*) **CMOS core module**
consists of p-substrate, single poly, triple metal and 3.3 Volt process.
) **POLY1-POLY2 capacitor module
consists of p-substrate, double poly (RPOLY2 resistor), triple metal and 3.3 Volt process.

1.3 Related Documents

Description	Document Number
0.35 um CMOS C35 Process Parameters	ENG-182
0.35 um CMOS C35 RF Spice Models	ENG-188
0.35 um CMOS C35 Noise Parameters	ENG-189
0.35 um CMOS C35 Matching Parameters	ENG-228
LV ESD Design Rules	ENG-41
Standard Family Cells	ENG-42
Assembly Related Design Rules	ASSY-15

Note

All data represent drawn dimensions. Graphical illustrations are not to scale.

2 General

2.1 Definitions

Process Layers

CONT (CO): contact layer (connects MET1 to DIFF, POLY1, POLY2)
DIFF (OD): diffusion layer
FIMP: p-tub / n-field implant layer
HRES (HR): high resistive layer
MET1 (M1): metal1 layer
MET2 (M2): metal2 layer
MET3 (M3): metal3 layer, top metal for 3-metal processes
MET4 (M4): standard or thick metal4 layer, top metal for 4-metal processes
METCAP (MC): metal capacitor layer
MIDOX (OD2): mid gate oxide layer (V(GATE)>3.3 Volt)
NLDD: n-LDD implant
NLDD50: 5 Volt n-LDD implant
NPLUS (NP): n+implant layer
NTUB (NW): n-tub layer
PAD (CB): pad layer
POLY1 (PO): poly1 layer
POLY2 (PO2): poly2 layer
PPLUS (PP): p+implant layer
VIA1: via1 layer (connects MET2 to MET1)
VIA2: via2 layer (connects MET3 to MET2)
VIA3: via3 layer (connects MET4 to MET3)

Definition Layers

Note: These layers are not used in chip production.
They are necessary for design tools, e.g. design rule check.

CAPDEF: sandwich capacitors
DIFCUT: excludes DIFF from device extraction
DIODE: marks protection diodes for device extraction
HOTTUB: marks HOT_NTUB
M1HOLE (M1): metal1 slot (MET1 = MET1 and not M1HOLE)
M2HOLE (M2): metal2 slot (MET2 = MET2 and not M2HOLE)
M3HOLE (M3): metal3 slot (MET3 = MET3 and not M3HOLE)
M4HOLE (M4): metal4 slot (MET4 = MET4 and not M4HOLE)
NOFILL: Avoids automatic generation of fill patterns
PO1CUT: excludes dummy POLY1 from device extraction
PO2CUT: excludes dummy POLY2 from device extraction

RESDEF: resistor definition layer
RESTRM: resistor definition cut layer (RESDEF = RESDEF and not RESTRM)
SFCDEF: excludes SFC from checks and automatic layer generation
SUBDEF: Substrate definition
TUBCUT: excludes dummy NTUB from device extraction
TUBDEF: n-tub resistor definition layer
ZENER: defines Zener diodes for checks and automatic layer generation

Structures

Note: "and" is a logical intersection. "sizing" is applied per side.

COLD_NTUB: NTUB connected to highest potential
DIFFCON: diffusion contact (CONT and DIFF and not POLY2 and not POLY1)
GATE: DIFF and POLY1
HOT_NDIFF: NDIFF outside NTUB not connected to PSUB
HOT_NTUB: NTUB not connected to highest potential
MTOP: Top Metal (MET3 or MET4)
NDIFF: n+diffusion (DIFF and NPLUS)
NDIFFCON: n+diffusion contact (DIFFCON and NPLUS)
NGATE: NDIFF and POLY1
NTAP: NDIFF and NTUB
PADVIA1: VIA1 and (PAD sizing 5 um)
PADVIA2: VIA2 and (PAD sizing 5 um)
PADVIA3: VIA3 and (PAD sizing 5 um)
PDIFF: p+diffusion (DIFF and PPLUS)
PDIFFCON: p+diffusion contact (DIFFCON and PPLUS)
PGATE: PDIFF and POLY1
POLY1CON: poly1 contact (CONT and POLY1 and not POLY2)
POLY2CON: poly2 contact (CONT and POLY2)
PSUB: p-substrate
PTAP: PDIFF and not NTUB
SCRIBE: scribe line border
SFC: standard family cells, they contain all derived process layers
WIDE_METx: METx width and length > 10 um, any METx within 1 um is included

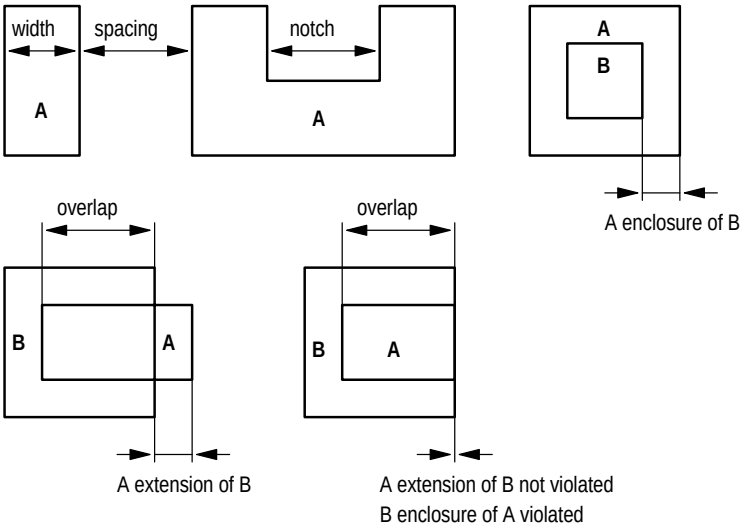
Elements

CMIM: metal2 to metalC capacitor (MET2 and METCAP)
CORNER: corner cell with slotted metal busses
CPOLY: poly1-poly2 capacitor (POLY1 and POLY2)
CVAR: Varactor - NMOS capacitor in NTUB
LAT2: lateral PNP transistor (2 um x 2 um emitter)
ND: parasitic n+p- diode (NDIFF and PSUB and DIODE)
NMOS: n-channel MOSFET (NGATE and PSUB)
NMOSM: n-channel MOSFET with mid gate oxide (NGATE and PSUB and MIDOX)
NMOSH: high voltage n-channel MOSFET
NMOSMH: high voltage n-channel MOSFET with mid-oxide

NWD: parasitic n-p- diode (NTUB and PSUB and DIODE)
PD: parasitic p+n- diode (PDIFF and NTUB and DIODE)
PMOS: p-channel MOSFET (PGATE and NTUB)
PMOSM: p-channel MOSFET with mid gate oxide (PGATE and NTUB and MIDOX)
RDIFFP3: p+diffusion resistor (PDIFF and RESDEF)
RNWELL: n-tub resistor (NTUB and RESDEF)
RPOLY2: poly2 resistor (POLY2 and RESDEF)
RPOLYH: high resistive poly2 resistor (POLY2 and HRES and not PPLUS)
VERT10: vertical PNP transistor (10 um x 10 um emitter)

Geometric Relations

A and B: logical intersection.
A sizing X um: A sized X um per side.
A width: distance inside_A - inside_A
A spacing to B: distance outside_A - outside_B (different polygons)
A notch: distance outside_A - outside_A (same polygon)
A enclosure of B: distance inside_A - outside_B (A contains B)
A extension of B: distance inside_A - outside_B (A may intersect B)
A overlap of B: distance inside_A - inside_B



2.2 Layout Requirements

Guideline	Description	Value
REC001	Grid	integral multiple of 0.025 um
REC002	Corners	90 deg,135 deg
REC003	Data extrema including SCRIBE	integral multiple of 5 um

3 Layer Overview

3.1 Core Module

Drawn Process Layers

Name	GDS2 Layer / Datatype	Width [um]	Spacing [um]
NTUB	5 / 0	1.7	1.0
DIFF	10 / 0	0.3	0.6
POLY1	20 / 0	0.35	0.45
NPLUS	23 / 0	0.6	0.6
PPLUS	24 / 0	0.6	0.6
CONT	34 / 0	0.4	0.4
MET1	35 / 0	0.5	0.45
VIA1	36 / 0	0.5	0.45
MET2	37 / 0	0.6	0.5
VIA2	38 / 0	0.5	0.45
MET3	39 / 0	0.6	0.6
PAD	40 / 0	15	15

Derived Process Layers

Name	GDS2 Layer / Datatype	Equation
FIMP	8 / 0	NTUB and not SFC
NLDD	21 / 0	NPLUS
MET1	35 / 0	MET1 and not M1HOLE
MET2	37 / 0	MET2 and not M2HOLE
MET3	39 / 0	MET3 and not M3HOLE

Definition Layers

Name	GDS2 Layer / Datatype	Comments
M1HOLE	35 / 1	MET1 slots
M2HOLE	37 / 1	MET2 slots
M3HOLE	39 / 1	MET3 slots
SFCDEF	62 / 2	standard family cells
SUBDEF	62 / 3	substrate definition
HOTTUB	62 / 4	HOT_NTUB
NOFILL	62 / 5	no fill patterns allowed
ZENER	62 / 10	zener diodes
DIODE	62 / 11	parasitic diodes in schematic
TUBDEF	62 / 12	tub resistors
RESDEF	62 / 13	diffusion and poly resistors
RESTRM	62 / 14	removes RESDEF and TUBDEF
CAPDEF	62 / 20	sandwich capacitors
DIFCUT	62 / 30	excludes DIFF for some checks
PO1CUT	62 / 31	excludes POLY1 for some checks
TUBCUT	62 / 34	excludes NTUB for some checks

3.2 POLY1-POLY2 Capacitor Module

Drawn Process Layers

Name	GDS2 Layer / Datatype	Width [um]	Spacing [um]
POLY2	30 / 0	0.65	0.5

Definition Layers

Name	GDS2 Number / Datatype	Comments
PO2CUT	62 / 32	excludes POLY2 for some checks

3.3 5 Volt Module

Drawn Process Layers

Name	GDS2 Layer / Datatype	Width [um]	Spacing [um]
MIDOX	14 / 0	0.6	0.6

Derived Process Layers

Name	GDS2 Layer / Datatype	Equation
NLDD	21 / 0	NPLUS and not MIDOX
NLDD50	53 / 0	NPLUS and MIDOX

3.4 Metal 4 Module

Drawn Process Layers

Name	GDS2 Layer / Datatype	Width [um]	Spacing [um]
VIA3	41 / 0	0.5	0.45
MET4	42 / 0	0.6	0.6

Derived Process Layers

Name	GDS2 Layer / Datatype	Equation
MET4	42 / 0	MET4 and not M4HOLE

Definition Layers

Name	GDS2 Number / Datatype	Comments
M4HOLE	42 / 1	MET4 slots

3.5 Thick Metal Module

Drawn Process Layers

Name	GDS2 Layer / Datatype	Width [um]	Spacing [um]
VIA3	41 / 0	0.5	0.45
MET4	42 / 0	2.5	2

Derived Process Layers

Name	GDS2 Layer / Datatype	Equation
MET4	42 / 0	MET4 and not M4HOLE

Definition Layers

Name	GDS2 Number / Datatype	Comments
M4HOLE	42 / 1	MET4 slots

3.6 High Resistive Poly Module

Drawn Process Layers

Name	GDS2 Layer / Datatype	Width [um]	Spacing [um]
HRES	29 / 0	0.6	0.6

3.7 MET2-METCAP Capacitor Module

Drawn Process Layers

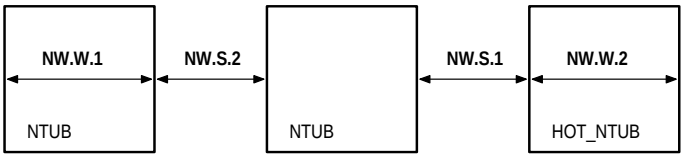
Name	GDS2 Layer / Datatype	Width [um]	Spacing [um]
METCAP	55 / 0	4	0.8

4 Layer Rules

4.1 Core Module

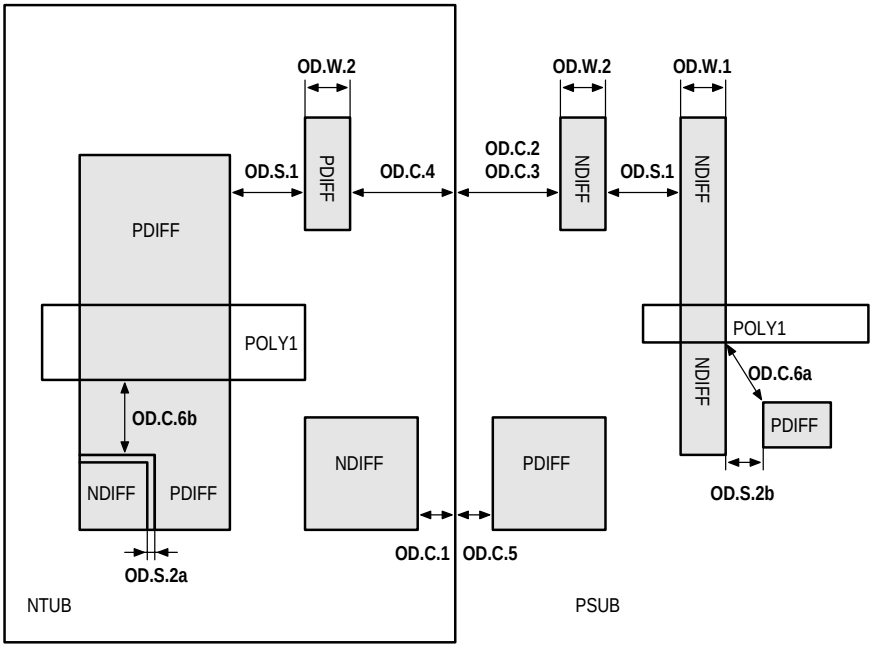
4.1.1 NTUB

Rule	Description	Value [um]
NW.W.1	Minimum NTUB width	1.7
NW.W.2	Minimum HOT_NTUB width	3
NW.S.1	Minimum spacing of NTUB with different potential	3
NW.S.2	Minimum spacing of NTUB with same potential	1



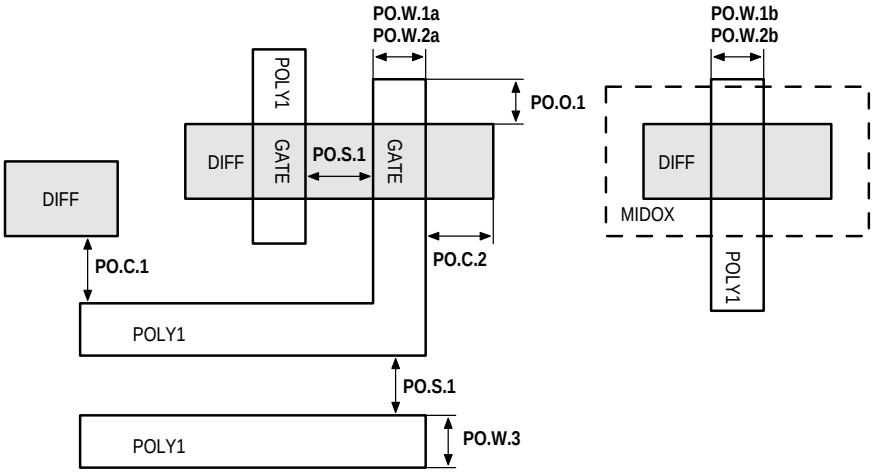
4.1.2 DIFF

Rule	Description	Value [um]
OD.W.1	Minimum DIFF width to define the width of NMOS / PMOS	0.4
OD.W.2	Minimum DIFF width for interconnection (NDIFF or PDIFF)	0.3
OD.S.1	Minimum DIFF spacing	0.6
OD.C.1	Minimum NTUB enclosure of NDIFF	0.2
OD.C.2	Minimum NDIFF to COLD_NTUB spacing	1.2
OD.C.3	Minimum NDIFF to HOT_NTUB spacing	2.6
OD.C.4	Minimum NTUB enclosure of PDIFF	1.2
OD.C.5	Minimum PDIFF to NTUB spacing	0.2
OD.C.6a	Minimum PDIFF to NGATE spacing	0.45
OD.C.6b	Minimum NDIFF to PGATE spacing	0.45
OD.S.2a	Minimum NDIFF to butting PDIFF spacing	0
OD.S.2b	Minimum NDIFF to non-butting PDIFF spacing	0.6



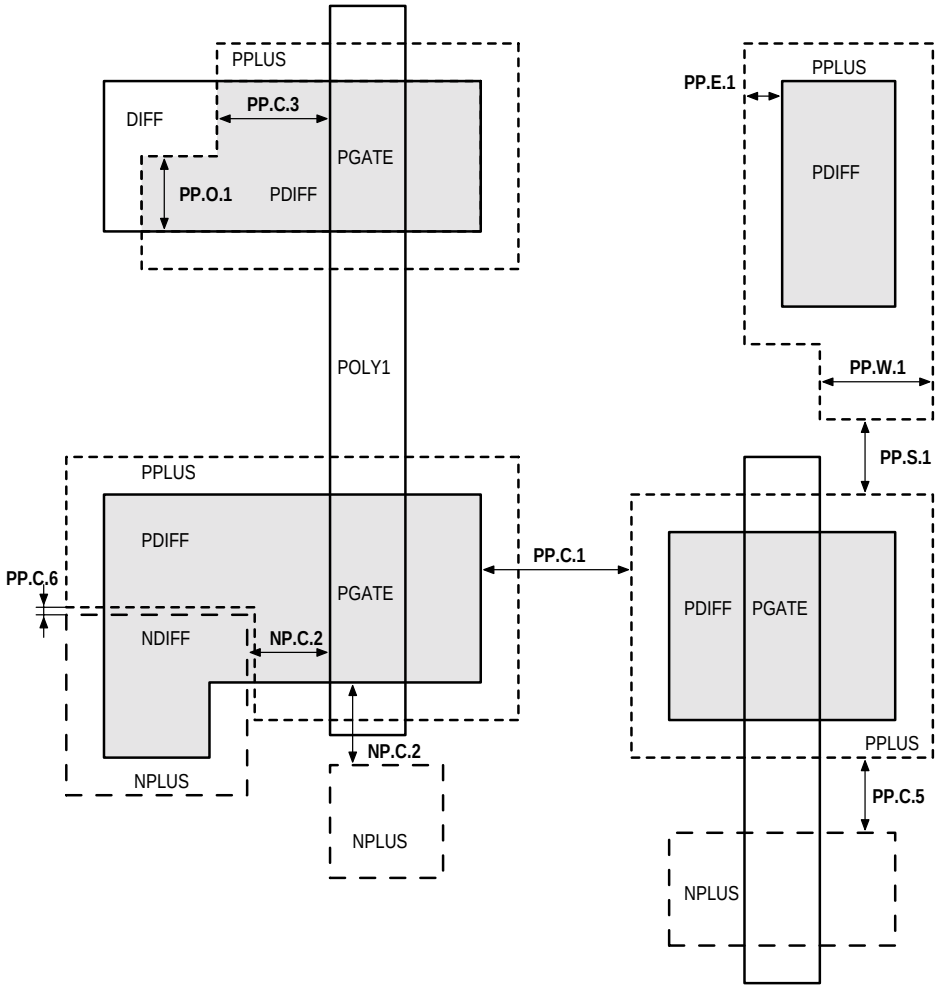
4.1.3 POLY1

Rule	Description	Value [um]
PO.W.1a	Minimum GATE length of PMOS	0.35
PO.W.1b	Minimum GATE length of PMOSM	0.5
PO.W.2a	Minimum GATE length of NMOS	0.35
PO.W.2b	Minimum GATE length of NMOSM	0.5
PO.W.3	Minimum POLY1 width for interconnect	0.35
PO.S.1	Minimum POLY1 spacing	0.45
PO.C.1	Minimum POLY1 to DIFF spacing	0.2
PO.C.2	Minimum DIFF extension of GATE	0.5
PO.O.1	Minimum POLY1 extension of GATE	0.4
PO.R.1	Minimum density of POLY1 area [%] Density = total poly layer area / chip area Recommended dummy structures are 5um * 2um rectangles with 2um spacing. They should not be placed on active devices.	14



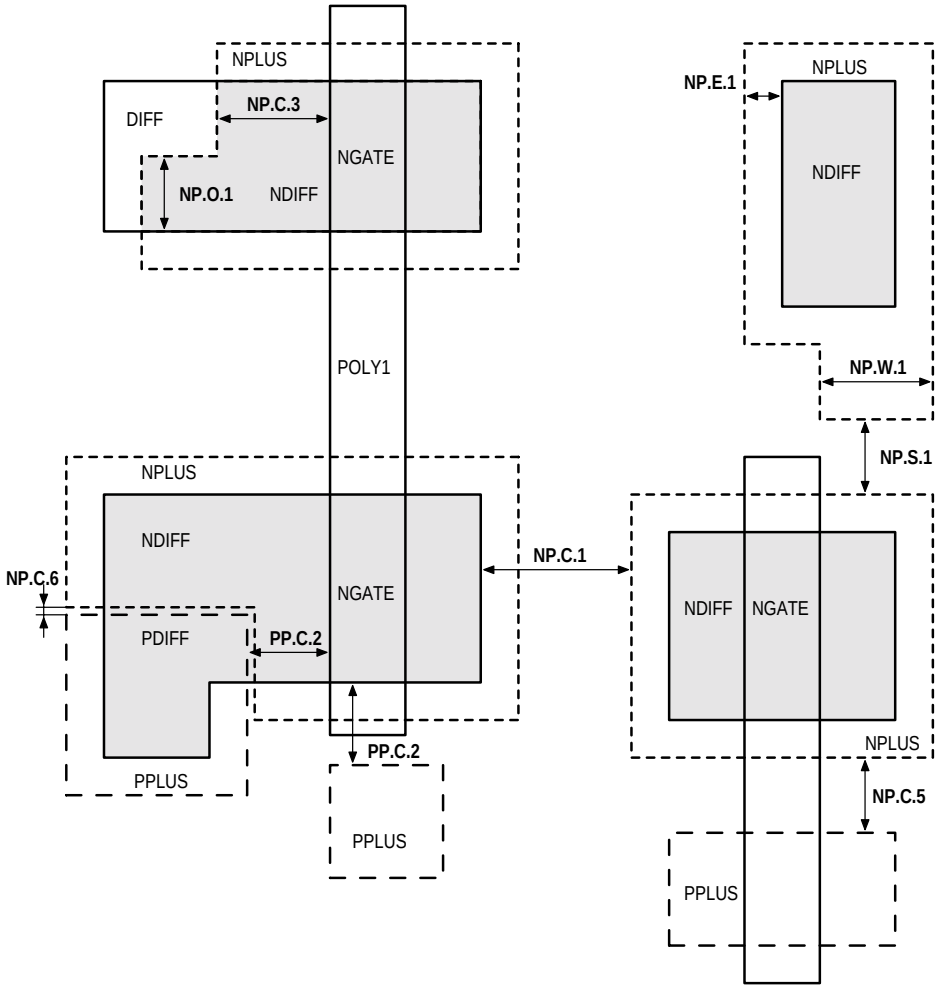
4.1.4 PPLUS

Rule	Description	Value [um]
PP.W.1	Minimum PPLUS width	0.6
PP.S.1	Minimum PPLUS spacing	0.6
PP.C.1	Minimum PPLUS to DIFF spacing	0.35
PP.C.2	Minimum PPLUS to NGATE spacing (shown in NPLUS section)	0.45
PP.C.3	Minimum PPLUS extension of PGATE	0.45
PP.O.1	Minimum overlap of PPLUS and DIFF	0.45
PP.E.1	Minimum PPLUS extension of DIFF	0.25
PP.C.5	Minimum PPLUS to NPLUS spacing on POLY1 Overlap of NPLUS and PPLUS on the same POLY1 region is not allowed	0.25
PP.C.6	Minimum PPLUS to NPLUS spacing on DIFF with same potential	0



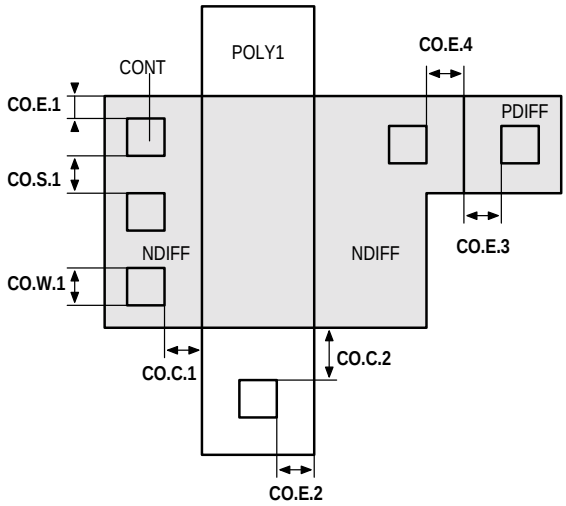
4.1.5 NPLUS

Rule	Description	Value [um]
NP.W.1	Minimum NPLUS width	0.6
NP.S.1	Minimum NPLUS spacing	0.6
NP.C.1	Minimum NPLUS to DIFF spacing	0.35
NP.C.2	Minimum NPLUS to PGATE spacing (shown in PPLUS section)	0.45
NP.C.3	Minimum NPLUS extension of NGATE	0.45
NP.O.1	Minimum overlap of NPLUS and DIFF	0.45
NP.E.1	Minimum NPLUS extension of DIFF	0.25
NP.C.5	Minimum PPLUS to NPLUS spacing on POLY1 Overlap of NPLUS and PPLUS on the same POLY1 region is not allowed	0.25
NP.C.6	Minimum NPLUS to PPLUS spacing on DIFF with same potential	0



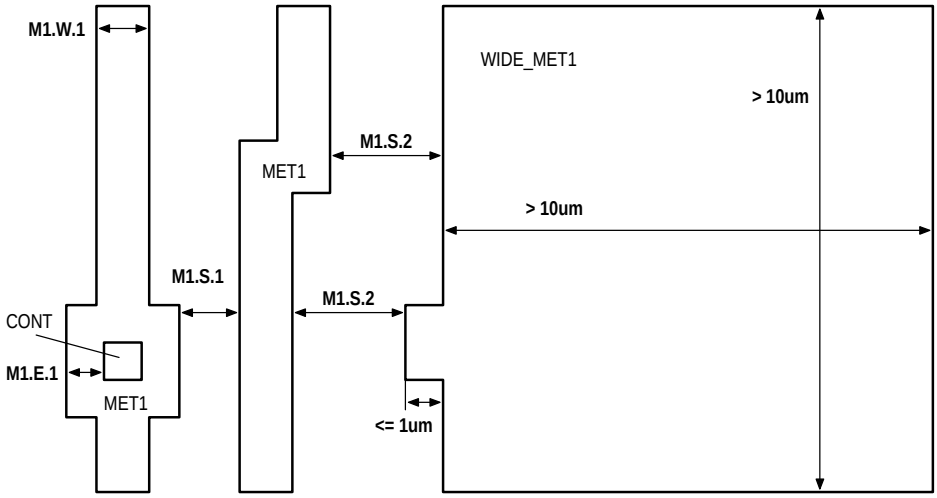
4.1.6 CONT

Rule	Description	Value [um]
CO.W.1	Fixed CONT width	0.4
CO.S.1	Minimum CONT spacing	0.4
CO.C.1	Minimum DIFFCON to GATE spacing	0.3
CO.C.2	Minimum POLY1CON to DIFF spacing	0.4
CO.E.1	Minimum DIFF enclosure of DIFFCON Use as many CONTs as possible.	0.15
CO.E.2	Minimum POLY1 enclosure of POLY1CON	0.2
CO.E.3	Minimum PPLUS enclosure of PDIFFCON	0.25
CO.E.4	Minimum NPLUS enclosure of NDIFFCON	0.25
CO.R.1	POLY1CON on DIFF is not allowed	
CO.R.2	Butted CONT is not allowed	



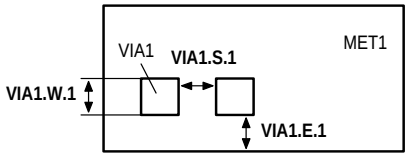
4.1.7 MET1

Rule	Description	Value [um]
M1.W.1	Minimum MET1 width	0.5
M1.S.1	Minimum MET1 spacing	0.45
M1.S.2	Minimum MET1 to WIDE_MET1 spacing	0.8
M1.E.1	Minimum MET1 enclosure of CONT	0.15
M1.R.1	Minimum density of MET1 area [%] Density = total metal layer area / chip area Recommended dummy structures are 5um * 2um rectangles with 2um spacing. They should not be placed on active devices.	30



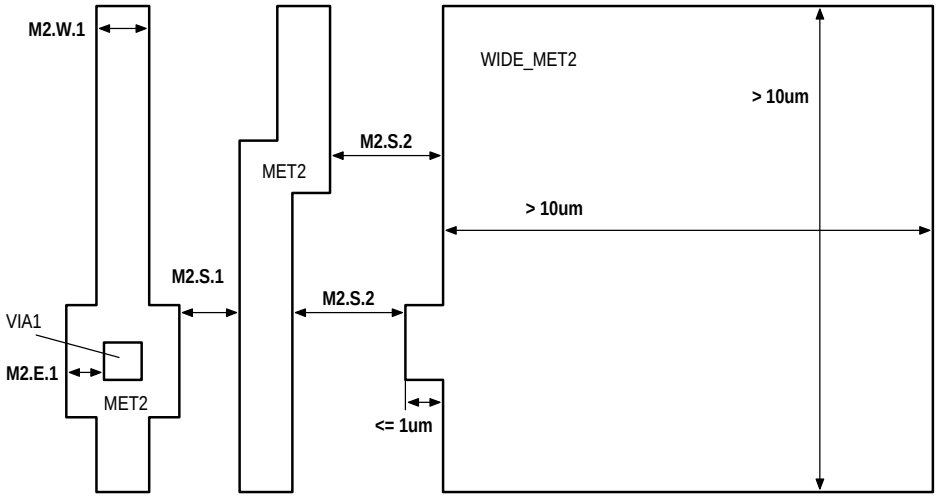
4.1.8 VIA1

Rule	Description	Value [um]
VIA1.0	VIA1 can be located at any region	
VIA1.W.1	Fixed VIA1 width	0.5
VIA1.S.1	Minimum VIA1 spacing	0.45
VIA1.E.1	Minimum MET1 enclosure of VIA1	0.2
VIA1.C.1	VIA1 can be fully or partially stacked on CONT	



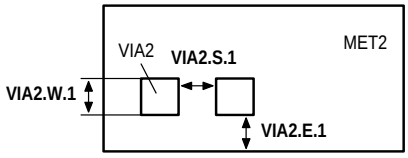
4.1.9 MET2

Rule	Description	Value [um]
M2.W.1	Minimum MET2 width	0.6
M2.S.1	Minimum MET2 spacing	0.5
M2.E.1	Minimum MET2 enclosure of VIA1	0.15
M2.S.2	Minimum MET2 to WIDE_MET2 spacing	0.8
M2.R.1	Minimum density of MET2 area [%] Density = total metal layer area / chip area Recommended dummy structures are 5um * 2um rectangles with 2um spacing. They should not be placed on active devices.	30



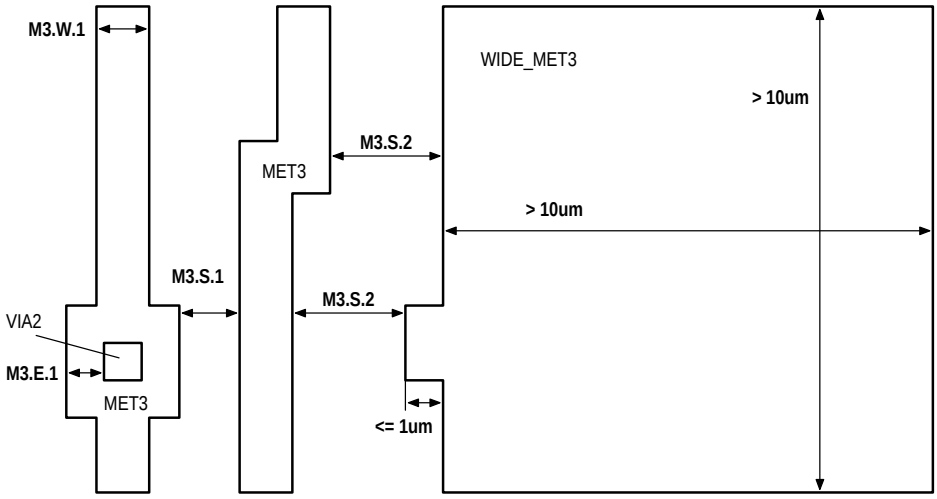
4.1.10 VIA2

Rule	Description	Value [um]
VIA2.0	VIA2 can be located at any region	
VIA2.W.1	Fixed VIA2 width	0.5
VIA2.S.1	Minimum VIA2 spacing	0.45
VIA2.E.1	Minimum MET2 enclosure of VIA2	0.2
VIA2.C.1	VIA2 can be fully or partially stacked on VIA1, CONT	



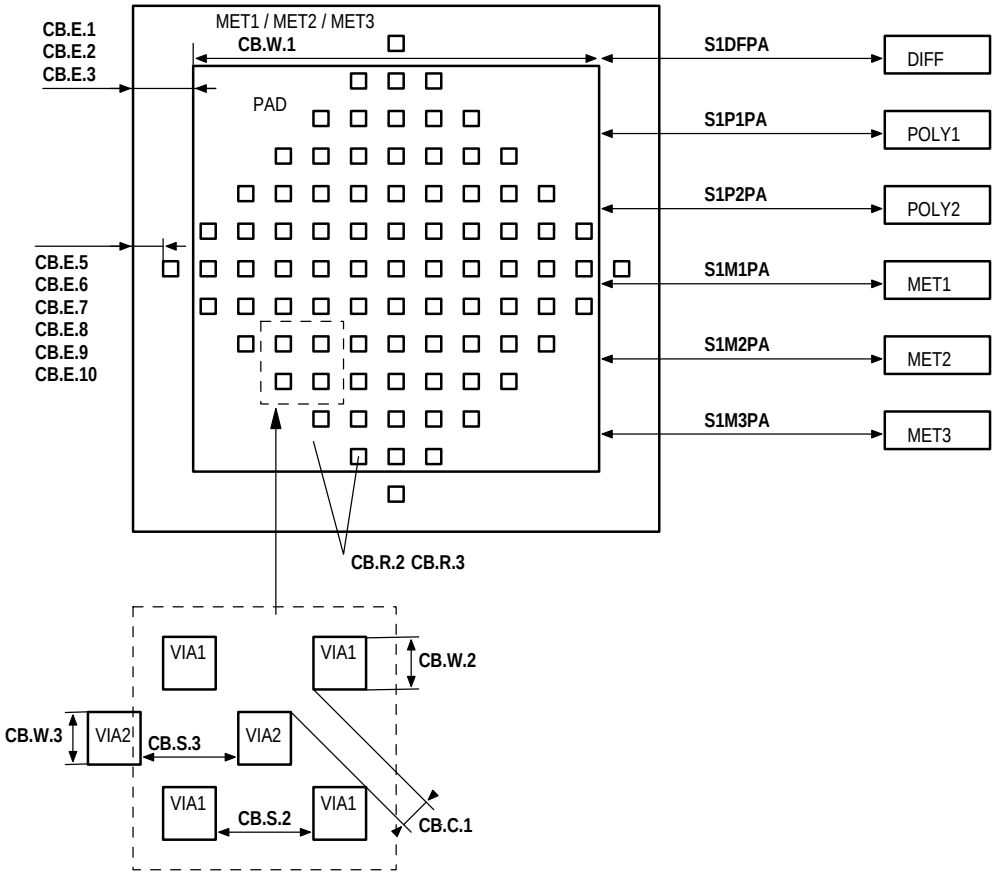
4.1.11 MET3

Rule	Description	Value [um]
M3.W.1	Minimum MET3 width	0.6
M3.S.1	Minimum MET3 spacing	0.6
M3.E.1	Minimum MET3 enclosure of VIA2	0.15
M3.S.2	Minimum MET3 to WIDE_MET3 spacing	0.8
M3.R.1	Minimum density of MET3 area [%] Density = total metal layer area / chip area Recommended dummy structures are 5um * 2um rectangles with 2um spacing.	30



4.1.12 PAD

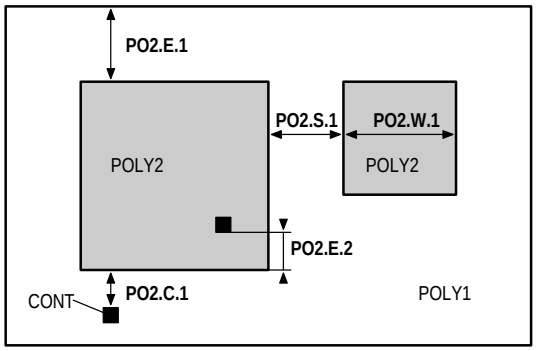
Rule	Description	Value [um]
CB.R.1	The bond stack must be MET3 / VIA2 / MET2 / VIA1 / MET1	
W1PA	Minimum PAD width	15
CB.W.1	Minimum bonding PAD width	85
CB.S.1	Minimum PAD spacing	15
CB.E.1	Fixed MET1 enclosure of PAD	5
CB.E.2	Fixed MET2 enclosure of PAD	5
CB.E.3	Fixed MET3 enclosure of PAD	5
CB.E.5	Minimum MET1 enclosure of the nearest PADVIA1 (vias on the four corners of diamond)	3
CB.E.6	Maximum MET1 enclosure of the nearest PADVIA1 (vias on the four corners of diamond)	6
CB.E.7	Minimum MET2 enclosure of the nearest PADVIA2 and PADVIA1 (vias on the four corners of diamond)	3
CB.E.8	Maximum MET2 enclosure of the nearest PADVIA2 and PADVIA1 (vias on the four corners of diamond)	6
CB.E.9	Minimum MET3 enclosure of the nearest PADVIA2 (vias on the four corners of diamond)	3
CB.E.10	Maximum MET3 enclosure of the nearest PADVIA2 (vias on the four corners of diamond)	6
CB.W.2	Fixed PADVIA1 width	0.5
CB.W.3	Fixed PADVIA2 width	0.5
CB.S.2	Minimum PADVIA1 spacing	0.8
CB.S.3	Minimum PADVIA2 spacing	0.8
CB.C.1	Minimum PADVIA2 to PADVIA1 spacing	0.3
CB.R.2	Minimum ratio of PADVIA1 area to PAD area [%]	5
CB.R.3	Minimum ratio of PADVIA2 area to PAD area [%]	5
S1DFPA	Minimum PAD to DIFF spacing	9
S1P1PA	Minimum PAD to POLY1 spacing	9
S1P2PA	Minimum PAD to POLY2 spacing	9
S1M1PA	Minimum PAD to MET1 spacing (different net)	9
S1M2PA	Minimum PAD to MET2 spacing (different net)	9
S1M3PA	Minimum PAD to MET3 spacing (different net)	9

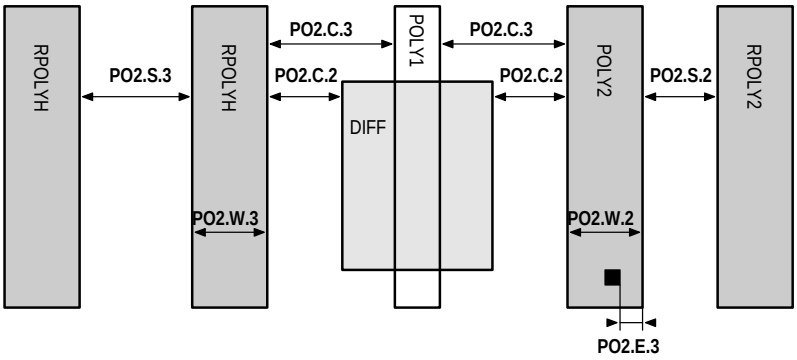

MET1 / MET2 / MET3
CB.W.1
CB.E.1
CB.E.2
CB.E.3
PAD
CB.E.5
CB.E.6
CB.E.7
CB.E.8
CB.E.9
CB.E.10
S1DFPA
DIFF
S1P1PA
POLY1
S1P2PA
POLY2
S1M1PA
MET1
S1M2PA
MET2
S1M3PA
MET3
CB.R.2 CB.R.3
VIA1
VIA1
CB.W.2
CB.W.3
VIA2
CB.S.3
VIA2
VIA1
CB.S.2
VIA1
CB.C.1

4.2 POLY1-POLY2 Capacitor Module

4.2.1 POLY2

Rule	Description	Value [um]
PO2.W.1	Minimum CPOLY width	0.8
PO2.W.2	Minimum POLY2 width	0.65
PO2.W.3	Minimum RPOLYH width	0.8
PO2.S.1	Minimum CPOLY spacing	0.65
PO2.S.2	Minimum POLY2 spacing	0.5
PO2.S.3	Minimum RPOLYH spacing	0.75
PO2.C.1	Minimum POLY1CON to CPOLY spacing	1.2
PO2.C.2	Minimum DIFF to POLY2 spacing	0.2
PO2.C.3	Minimum POLY1 to POLY2 spacing	0.65
PO2.E.1	Minimum POLY1 enclosure of CPOLY	1
PO2.E.2	Minimum CPOLY enclosure of POLY2CON	0.6
PO2.E.3	Minimum POLY2 enclosure of POLY2CON	0.25
PO2.R.1	POLY2 on DIFF is not allowed	

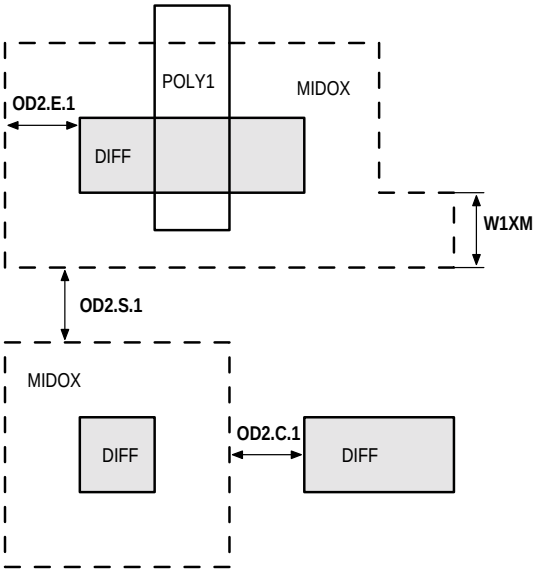




4.3 5 Volt Module

4.3.1 MIDOX

Rule	Description	Value [um]
W1XM	Minimum MIDOX width	0.6
OD2.E.1	Minimum MIDOX enclosure of DIFF	0.6
OD2.S.1	Minimum MIDOX spacing	0.6
OD2.C.1	Minimum MIDOX to DIFF spacing	0.6
BAD1XM	MIDOX outside GATE is not allowed	



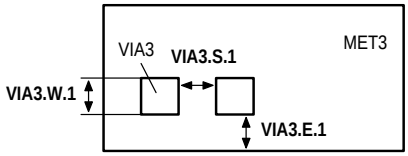
4.4 Metal 4 Module

4.4.1 MET3

Rule	Description	Value [um]
M3.S.1	Minimum MET3 spacing	0.5

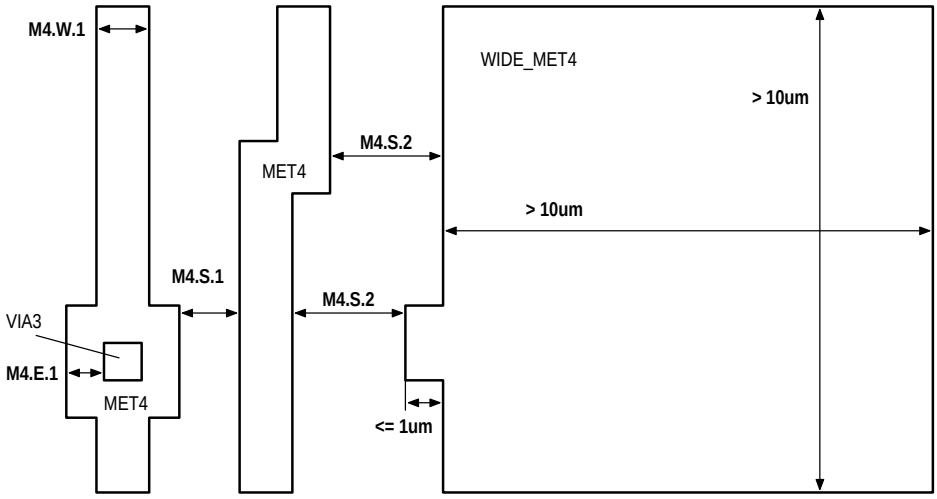
4.4.2 VIA3

Rule	Description	Value [um]
VIA3.0	VIA3 can be located at any region	
VIA3.W.1	Fixed VIA3 width	0.5
VIA3.S.1	Minimum VIA3 spacing	0.45
VIA3.E.1	Minimum MET3 enclosure of VIA3	0.2
VIA3.C.1	VIA3 can be fully or partially stacked on VIA2, VIA1, CONT	



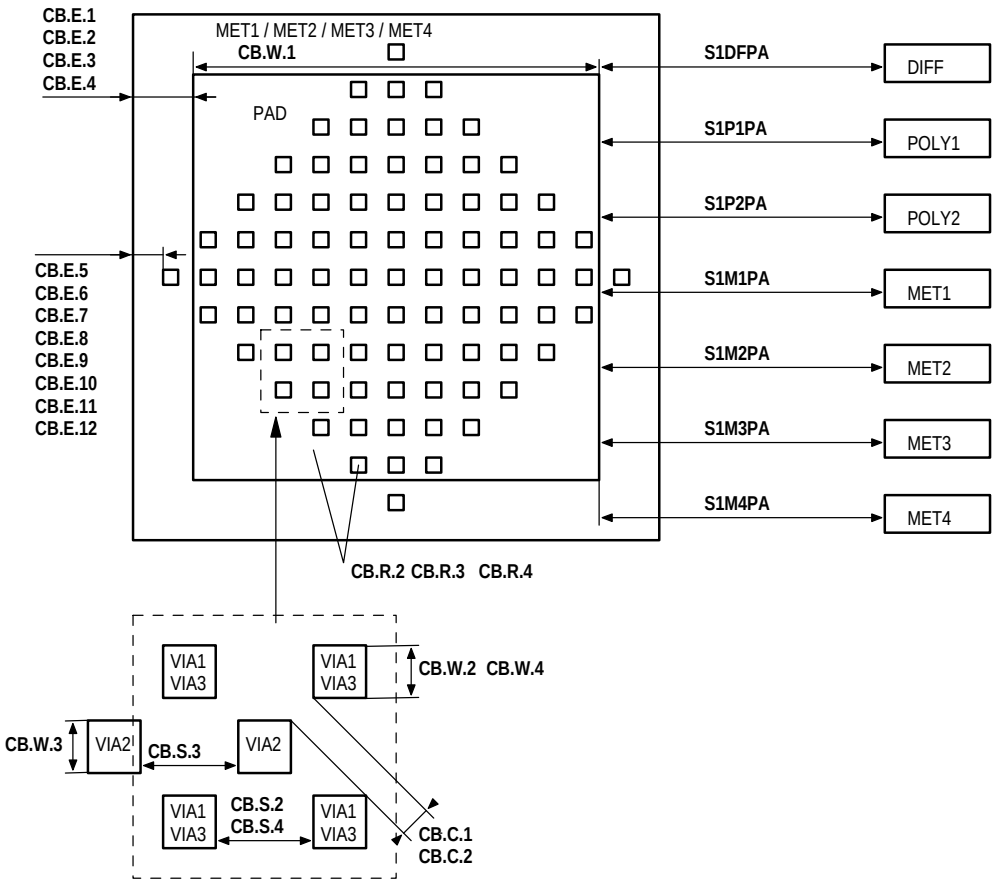
4.4.3 MET4

Rule	Description	Value [um]
M4.W.1	Minimum MET4 width	0.6
M4.S.1	Minimum MET4 spacing	0.6
M4.E.1	Minimum MET4 enclosure of VIA3	0.15
M4.S.2	Minimum MET4 to WIDE_MET4 spacing	0.8
M4.R.1	Minimum density of MET4 area [%] Density = total metal layer area / chip area Recommended dummy structures are 5um * 2um rectangles with 2um spacing.	30



4.4.4 PAD

Rule	Description	Value [um]
CB.R.1	The bond stack must be MET4 / VIA3 / MET3 / VIA2 / MET2 / VIA1 / MET1	
CB.E.4	Fixed MET4 enclosure of PAD	5
CB.E.9	Minimum MET3 enclosure of the nearest PADVIA3 and PADVIA2 (vias on the four corners of diamond)	3
CB.E.10	Maximum MET3 enclosure of the nearest PADVIA3 and PADVIA2 (vias on the four corners of diamond)	6
CB.E.11	Minimum MET4 enclosure of the nearest PADVIA3 (vias on the four corners of diamond)	3
CB.E.12	Maximum MET4 enclosure of the nearest PADVIA3 (vias on the four corners of diamond)	6
CB.W.4	Fixed PADVIA3 width	0.5
CB.S.4	Minimum PADVIA3 spacing	0.8
CB.C.2	Minimum PADVIA3 to PADVIA2 spacing	0.3
CB.R.4	Minimum ratio of PADVIA3 area to PAD area [%]	5
S1M4PA	Minimum PAD to MET4 spacing (different net)	9



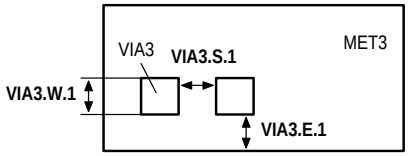
4.5 Thick Metal Module

4.5.1 MET3

Rule	Description	Value [um]
M3.S.1	Minimum MET3 spacing	0.5

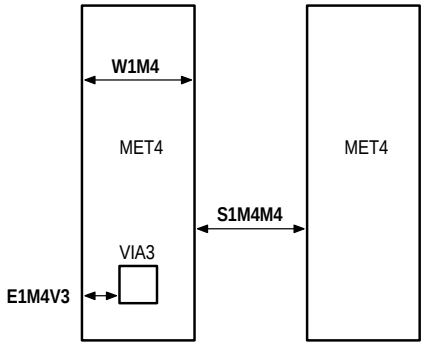
4.5.2 VIA3

Rule	Description	Value [um]
VIA3.0	VIA3 can be located at any region	
VIA3.W.1	Fixed VIA3 width	0.5
VIA3.S.1	Minimum VIA3 spacing	0.45
VIA3.E.1	Minimum MET3 enclosure of VIA3	0.2
VIA3.C.1	VIA3 can be fully or partially stacked on VIA2, VIA1, CONT	



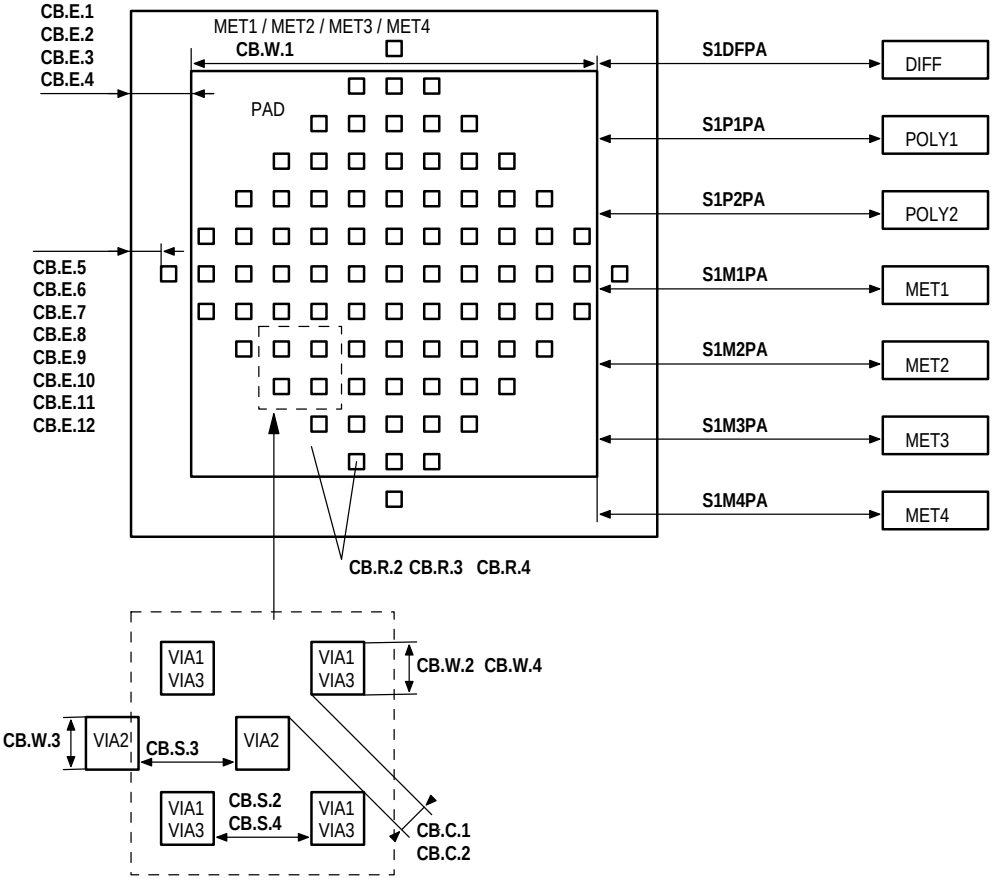
4.5.3 MET4

Rule	Description	Value [um]
W1M4	Minimum MET4 width	2.5
S1M4M4	Minimum MET4 spacing	2
E1M4V3	Minimum MET4 enclosure of VIA3	0.5



4.5.4 PAD

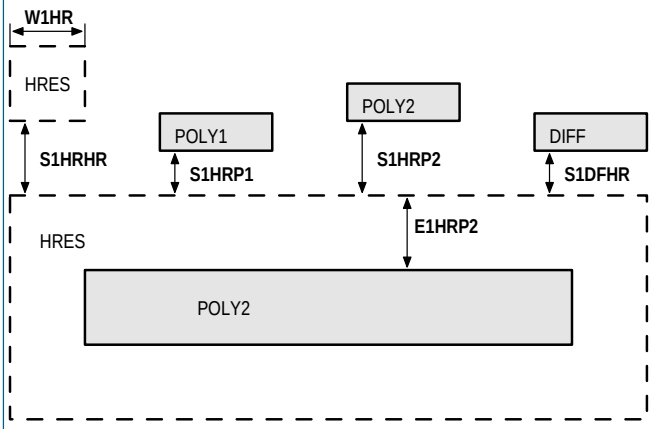
Rule	Description	Value [um]
CB.R.1	Recommended bond stack: MET4 / VIA3 / MET3 / VIA2 / MET2 / VIA1 / MET1 Note: All METx layers must be connected together	
CB.E.4	Fixed MET4 enclosure of PAD	5
CB.E.9	Minimum MET3 enclosure of the nearest PADVIA3 and PADVIA2 (via on the four corners of diamond)	3
CB.E.10	Maximum MET3 enclosure of the nearest PADVIA3 and PADVIA2 (via on the four corners of diamond)	6
CB.E.11	Minimum MET4 enclosure of the nearest PADVIA3 (via on the four corners of diamond)	3
CB.E.12	Maximum MET4 enclosure of the nearest PADVIA3 (via on the four corners of diamond)	6
CB.W.4	Fixed PADVIA3 width	0.5
CB.S.4	Minimum PADVIA3 spacing	0.8
CB.C.2	Minimum PADVIA3 to PADVIA2 spacing	0.3
CB.R.4	Minimum ratio of PADVIA3 area to PAD area [%]	5
S1M4PA	Minimum PAD to MET4 spacing (different net)	9



4.6 High Resistive Poly Module

4.6.1 HRES

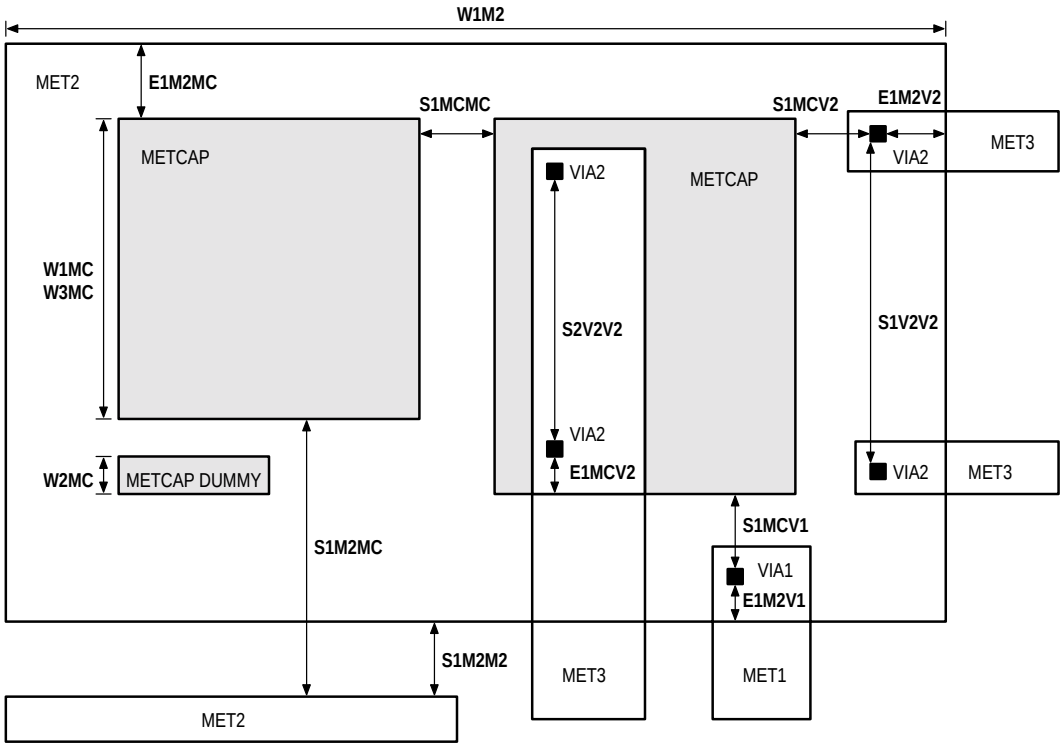
Rule	Description	Value [um]
W1HR	Minimum HRES width	0.6
S1HRHR	Minimum HRES spacing	0.6
BAD1HR	HRES is not allowed over DIFF	
BAD2HR	HRES is not allowed over NPLUS	
BAD3HR	HRES is not allowed over POLY1	
E1HRP2	Minimum HRES enclosure of POLY2	3
S1HRP1	Minimum HRES to POLY1 spacing	0.35
S1HRP2	Minimum HRES to POLY2 spacing	3
S1DFHR	Minimum HRES to DIFF spacing	0.35



4.7 MET2-METCAP Capacitor Module

4.7.1 METCAP

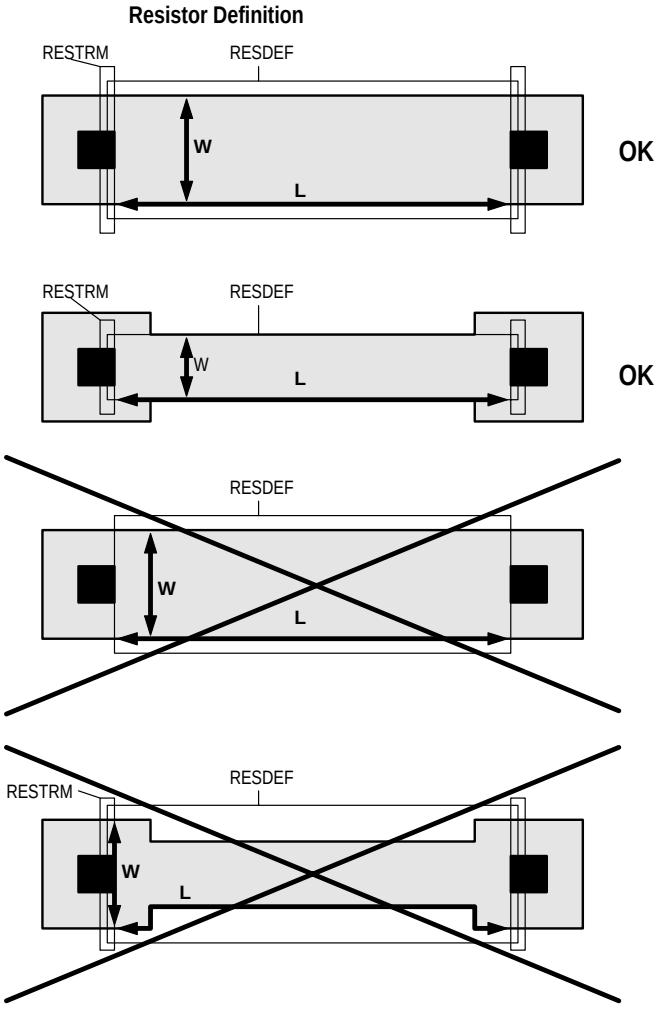
Rule	Description	Value [um]
W1MC	Minimum METCAP width	4
W2MC	Minimum dummy METCAP width	0.5
W3MC	Maximum METCAP width	30
W1M2	Maximum MET2 width (capacitor bottom plate)	35
S1MCMC	Minimum METCAP spacing	0.8
S1M2M2	Minimum MET2 spacing (capacitor bottom plate)	0.8
S1MCV1	Minimum spacing between VIA1 and METCAP	0.5
S1MCV2	Minimum spacing between VIA2 and METCAP	0.5
S1V2V2	Minimum VIA2 spacing on MET2 bottom plate outside METCAP	4
S2V2V2	Minimum VIA2 spacing on METCAP	3.5
S1M2MC	Minimum spacing between METCAP and unrelated MET2	5
E1M2MC	Minimum MET2 enclosure of METCAP	1
E1M2V1	Minimum MET2 enclosure of VIA1 (capacitor bottom plate)	0.2
E1M2V2	Minimum MET2 enclosure of VIA2 (capacitor bottom plate)	0.2
E1MCV2	Minimum METCAP enclosure of VIA2	0.5
R1MC	Minimum METCAP density [%]	3
R1V2	Minimum VIA2 density inside METCAP [%]	1
BAD1M1	MET1 under METCAP region is not allowed	



5 Element Rules

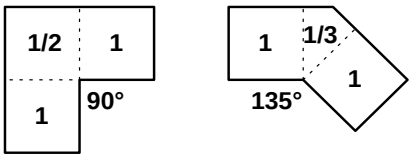
5.1 Layout Conventions

5.1.1 Resistor Definition



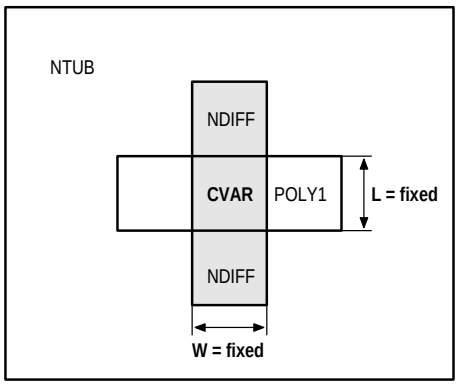
5.1.2 Resistor Corner Correction

Use the following effective number of squares to calculate the resistance of corners:



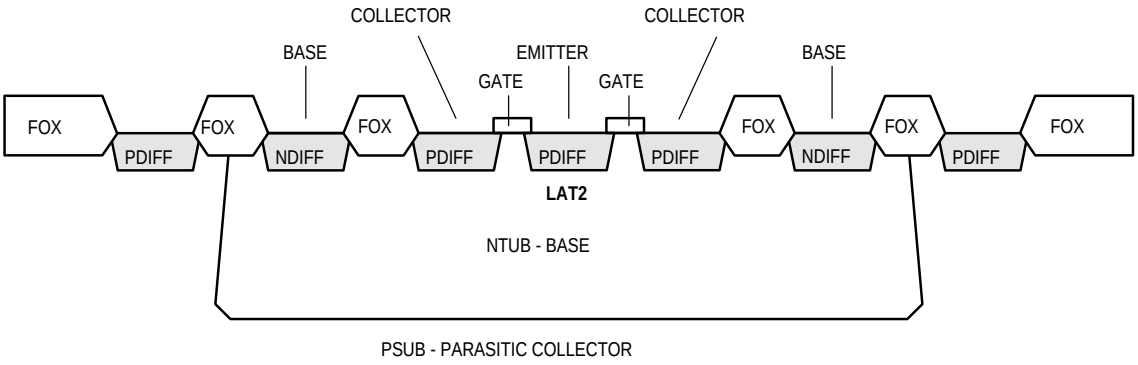
5.2 Core Module

5.2.1 CVAR



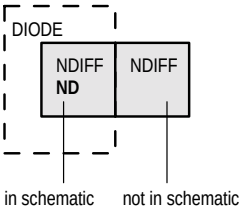
Note: The layout of CVAR units are predefined and available on request.

5.2.2 LAT2



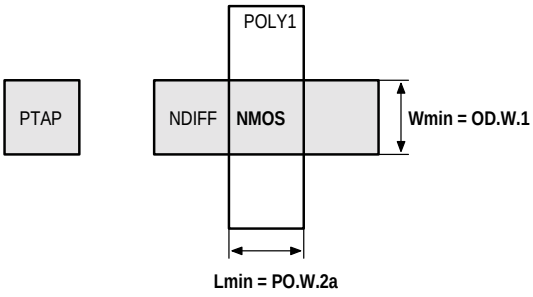
Note: The layout of LAT2 is predefined and available on request. It must not be changed.

5.2.3 ND



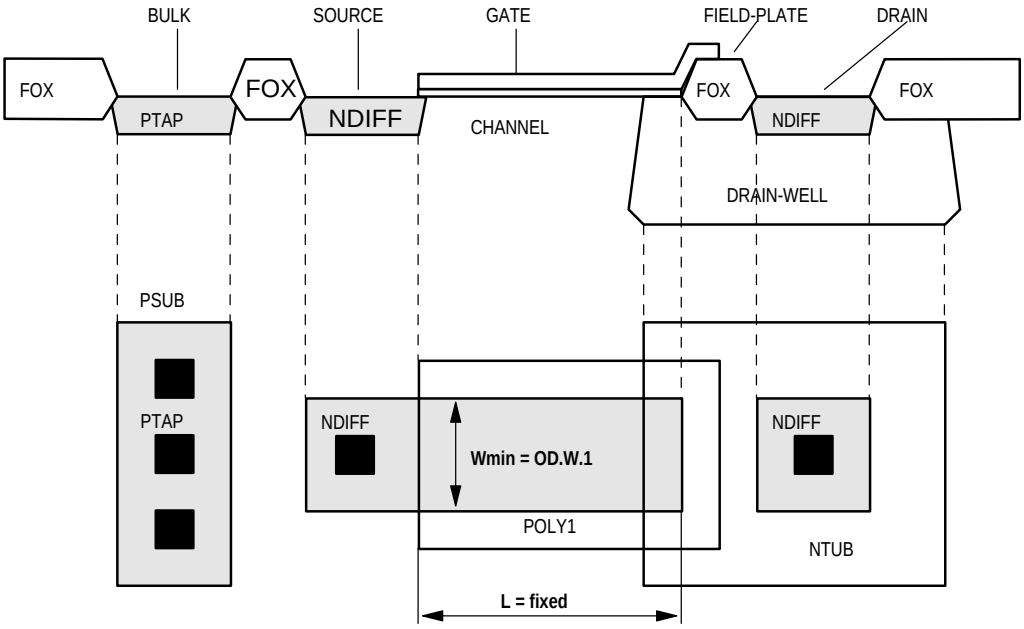
Note: ND is only intended for simulation of reverse leakage currents and junction capacitances. It is not recommended to use this diode as an active circuit element.

5.2.4 NMOS



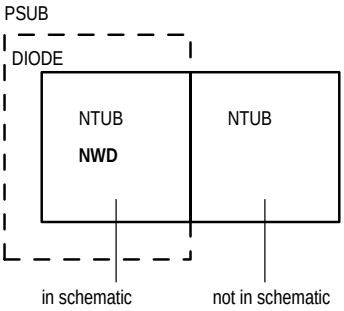
Guideline	Description	Value [um]
REC006	Precision analog NMOS should not be covered with MET1 / 2. If this is not possible MET1 / 2 covering of matching transistors should be identical.	
REC007	Minimum channel length for critical analog NMOS transistors Critical analog NMOS transistors are: 1. Transistors biased at (Vth < VGS < VDS / 2; VDS = VDSmax). Low temperature applications are especially critical. 2. Transistors used in circuits sensitive to Vth shift.	0.6

5.2.5 NMOSH



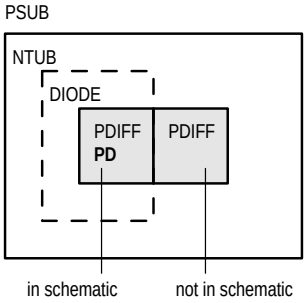
Note: The layout of NMOSH is predefined and available on request. Only W may be changed.

5.2.6 NWD



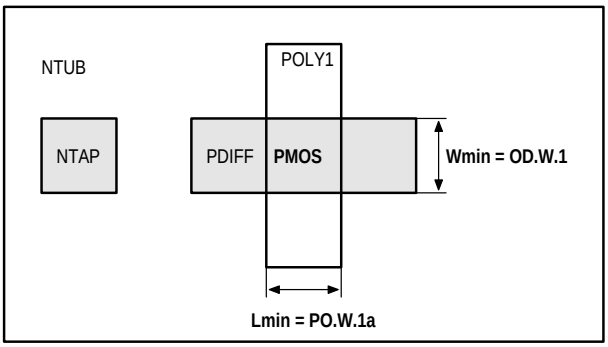
Note: NWD is only intended for simulation of reverse leakage currents and junction capacitances. It is not recommended to use this diode as an active circuit element.

5.2.7 PD



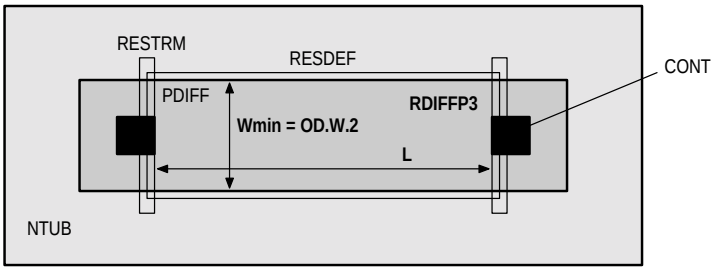
Note: PD is only intended for simulation of reverse leakage currents and junction capacitances. It is not recommended to use this diode as an active circuit element.

5.2.8 PMOS

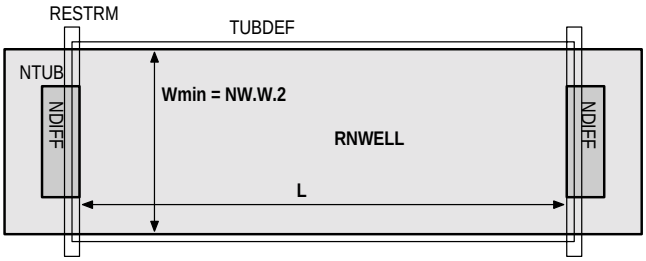


Guideline	Description
REC010	Precision analog PMOS should not be covered with MET1 / 2. If this is not possible MET1 / 2 covering of matching transistors should be identical.

5.2.9 RDIFFP3

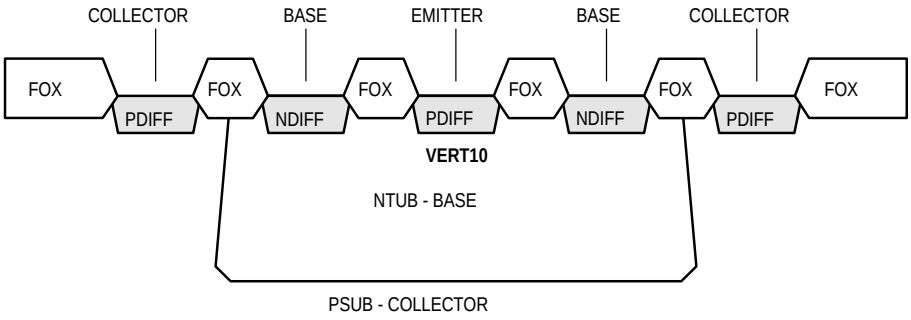


5.2.10 RNWELL



Guideline	Description	Value
REC017	Minimum number of RNWELL squares	5

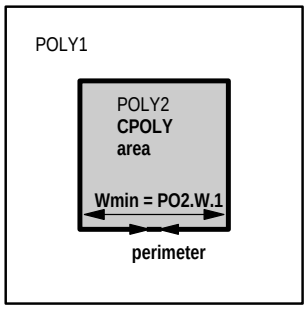
5.2.11 VERT10



Note: The layout of VERT10 is predefined and available on request. It must not be changed.

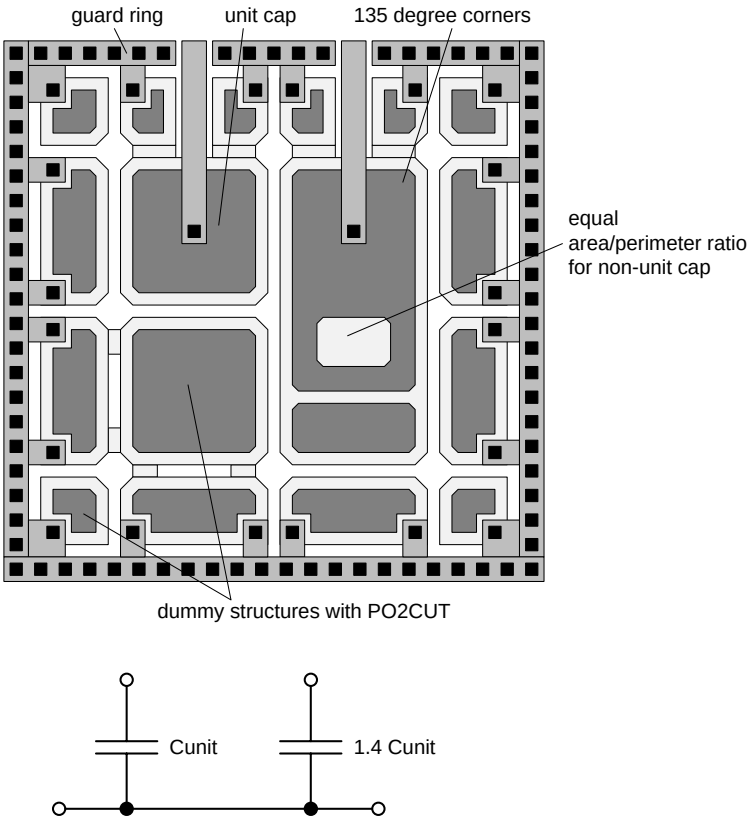
5.3 POLY1-POLY2 Capacitor Module

5.3.1 CPOLY

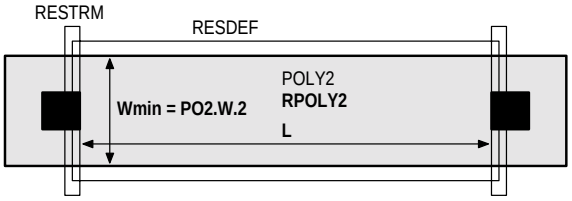


Guideline	Description
REC004	PPLUS on CPOLY is not allowed
REC005	NPLUS on CPOLY is not allowed

CPOLY Example

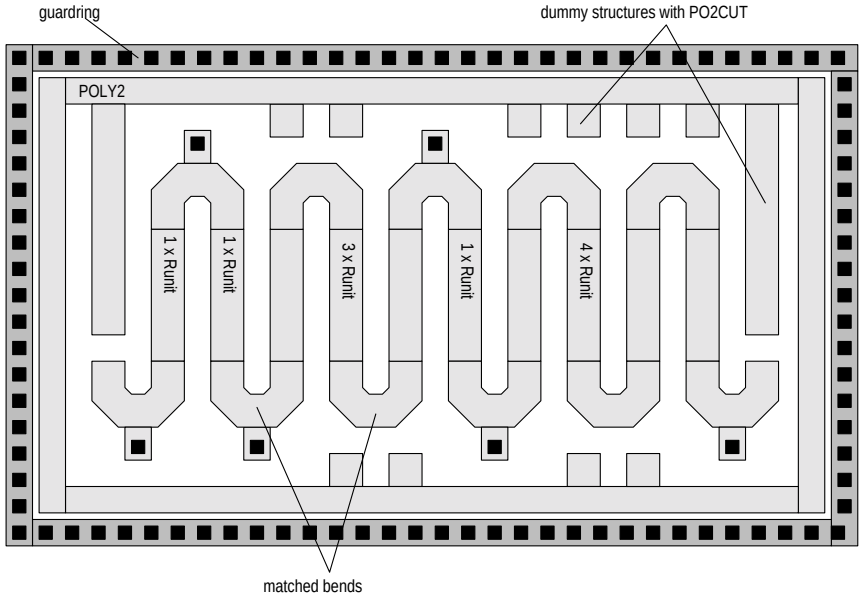


5.3.2 RPOLY2



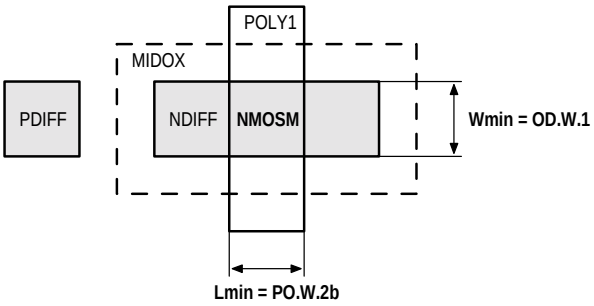
Rule	Description	Value
REC012	PPLUS on RPOLY2 is not allowed	
REC013	NPLUS on RPOLY2 is not allowed	
REC014	Minimum number of RPOLY2 squares	5

RPOLY2 Example



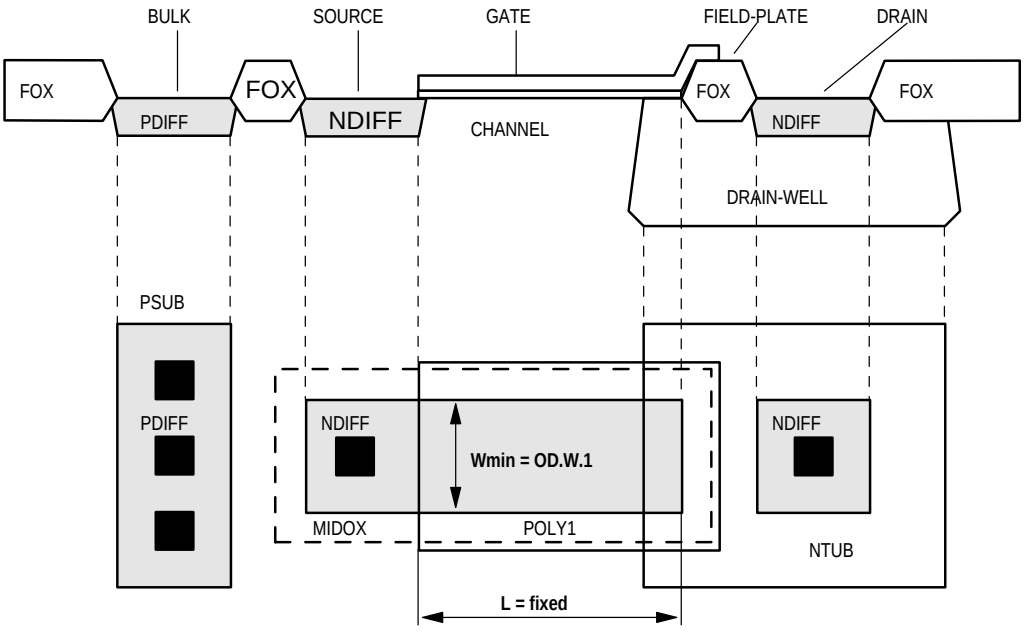
5.4 5-Volt Module

5.4.1 NMOSM



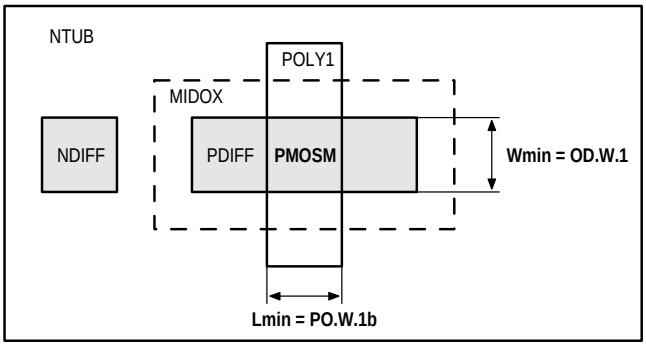
Guideline	Description	Value [um]
REC008	Precision analog NMOSM should not be covered with MET1 / 2. If this is not possible MET1 / 2 covering of matching transistors should be identical.	
REC009	Minimum channel length for critical analog NMOSM transistors Critical analog NMOSM transistors are: 1. Transistors biased at (Vth < VGS < VDS / 2; VDS = VDSmax). Low temperature applications are especially critical. 2. Transistors used in circuits sensitive to Vth shift.	1

5.4.2 NMOSMH



Note: The layout of NMOSMH is predefined and available on request. Only W may be changed.

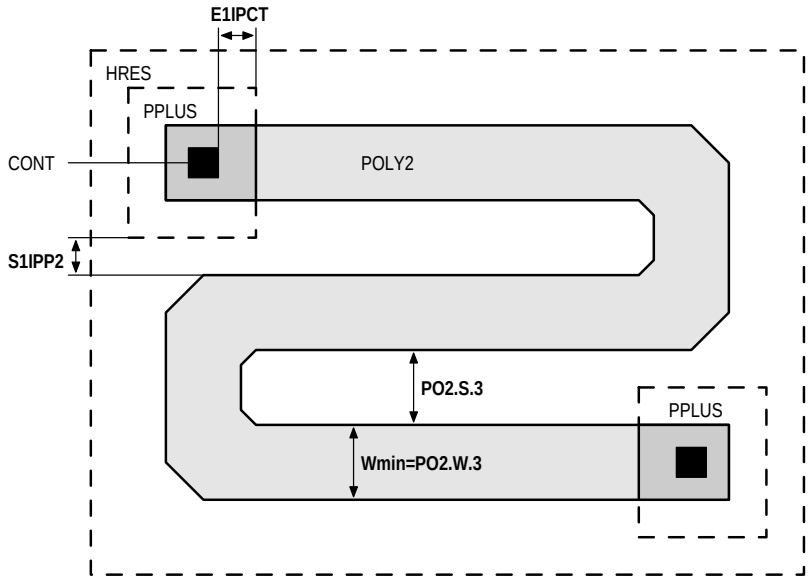
5.4.3 PMOSM



Guideline	Description
REC011	Precision analog PMOSM should not be covered with MET1 / 2. If this is not possible MET1 / 2 covering of matching transistors should be identical.

5.5 High Resistive Poly Module

5.5.1 RPOLYH

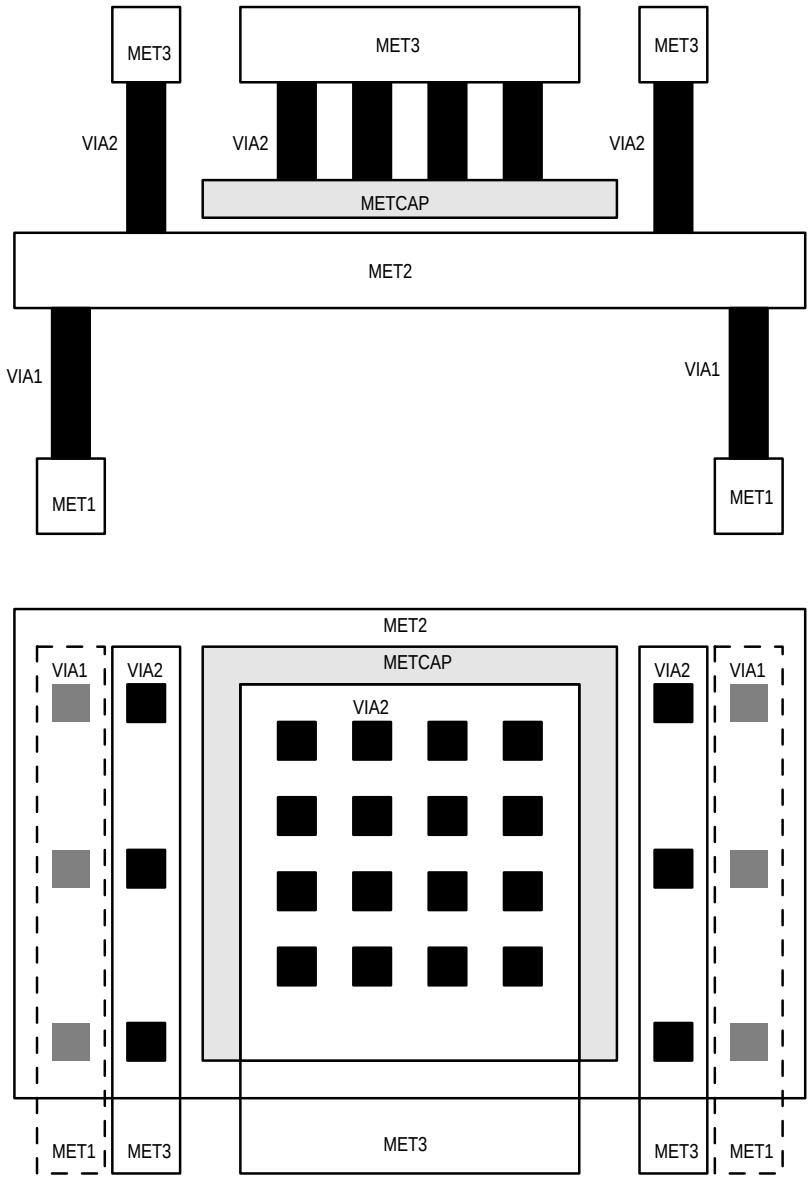


Rule	Description	Value [um]
E1IPCT	Minimum PPLUS enclosure of POLY2CON	0.6
S1IPP2	Minimum PPLUS to RPOLYH spacing	0.35

Guideline	Description	Value [um]
REC015	Minimum number of RPOLYH squares	5
REC016	Minimum high precision RPOLYH width	2

5.6 MET2-METCAP Capacitor Module

5.6.1 CMIM



Note: Acitve and passive circuit elements under METCAP are not allowed to avoid noise coupling or deviated MIM capacitance. Put as many VIA2 on METCAP to achieve a high Q factor.

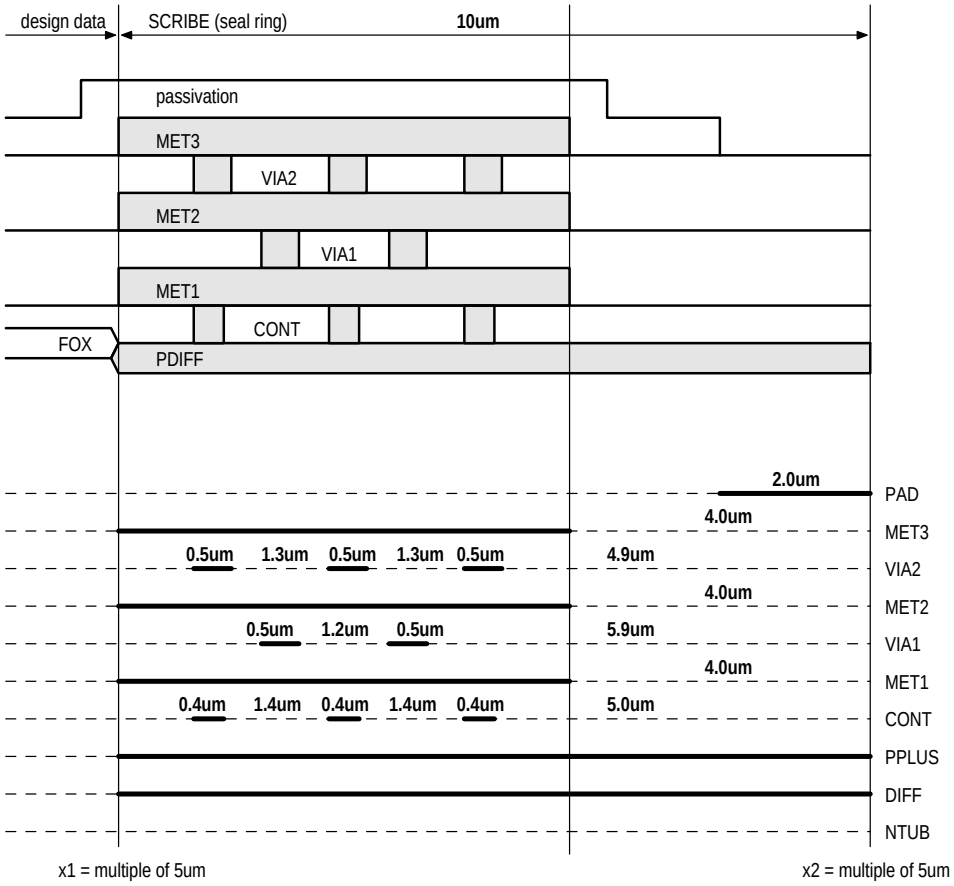
6 Scribe Border

A scribe border seals the chip against humidity and other external influences. This guard ring is connected to substrate.

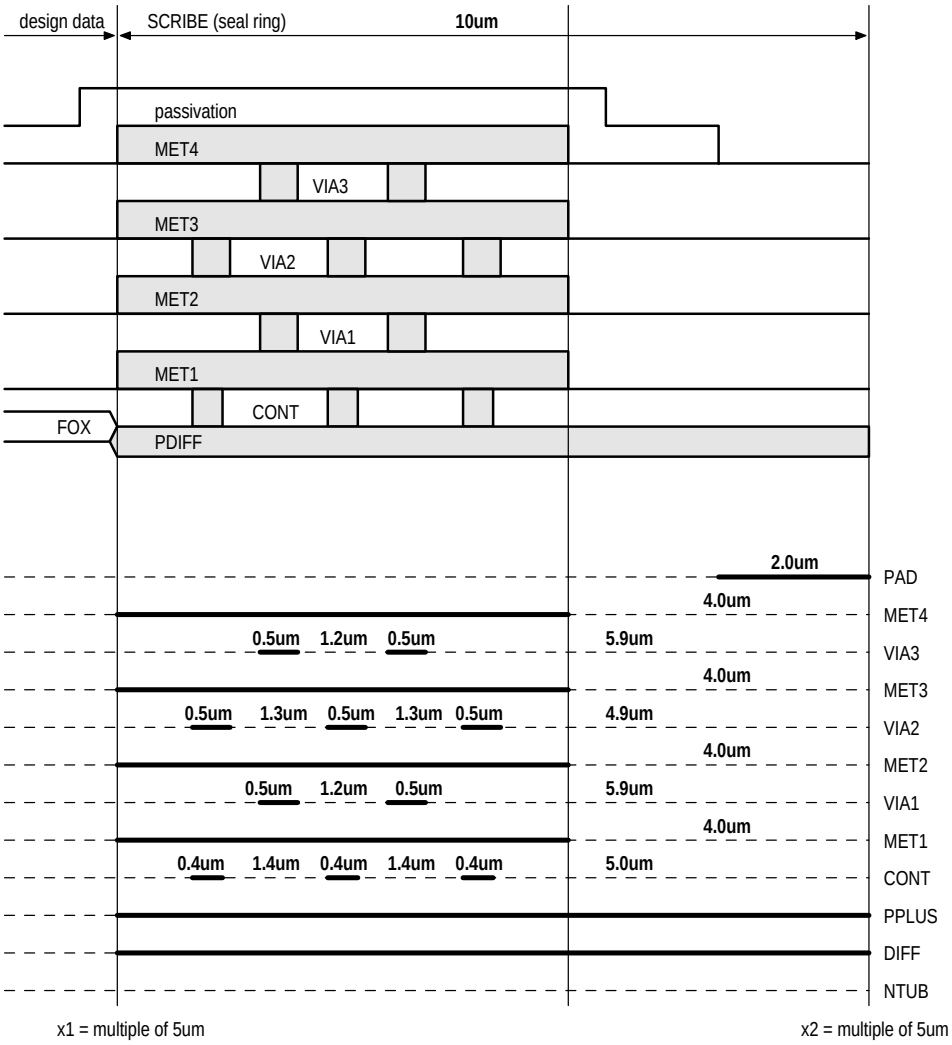
SCRIBE is a predefined layout and must completely enclose the design data. The inner edge of SCRIBE is butted to the data extrema of the design.

Only minimum sized vias according to the standard design rules are allowed.

6.1 Core Module



6.2 Metal 4 Module



6.3 Thick Metal Module

Identical to Metal 4 Module.

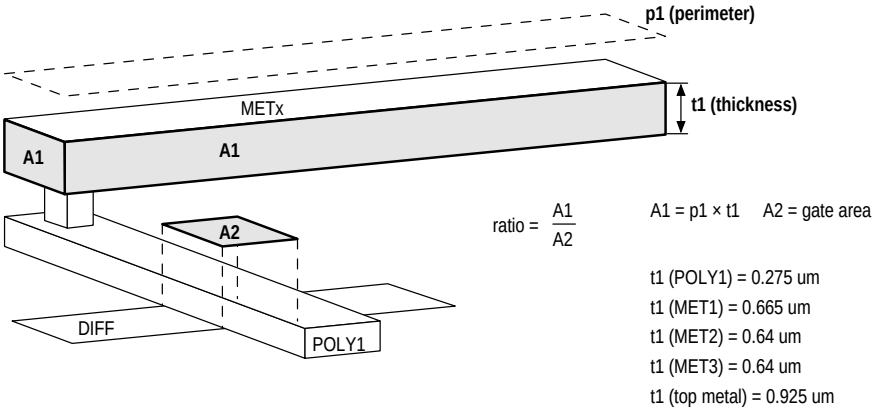
7 Ion Etch Antennas

7.1 Core Module

Structures collect electric charge during ion-etching which can be a hazard for associated GATE oxide.

Rule	Description	Value [um]
A.R.1	Maximum ratio of floating POLY1 edge area to connected GATE area	200
A.R.2	Maximum ratio of floating MET1 edge area to connected GATE area	400
A.R.3	Maximum ratio of floating MET2 edge area to connected GATE area	400
A.R.4	Maximum ratio of floating MET3 edge area to connected GATE area	400

Note: “floating” are shapes connected to active GATE area but not to DIFF.
Only layers which have been formed before etching have to be considered



7.2 Metal 4 Module

Rule	Description	Value [um]
A.R.5	Maximum ratio of floating MET4 edge area to connected GATE area	400

7.3 Thick Metal Module

Identical to Metal 4 Module.

8 Stress Release and CMP Rules

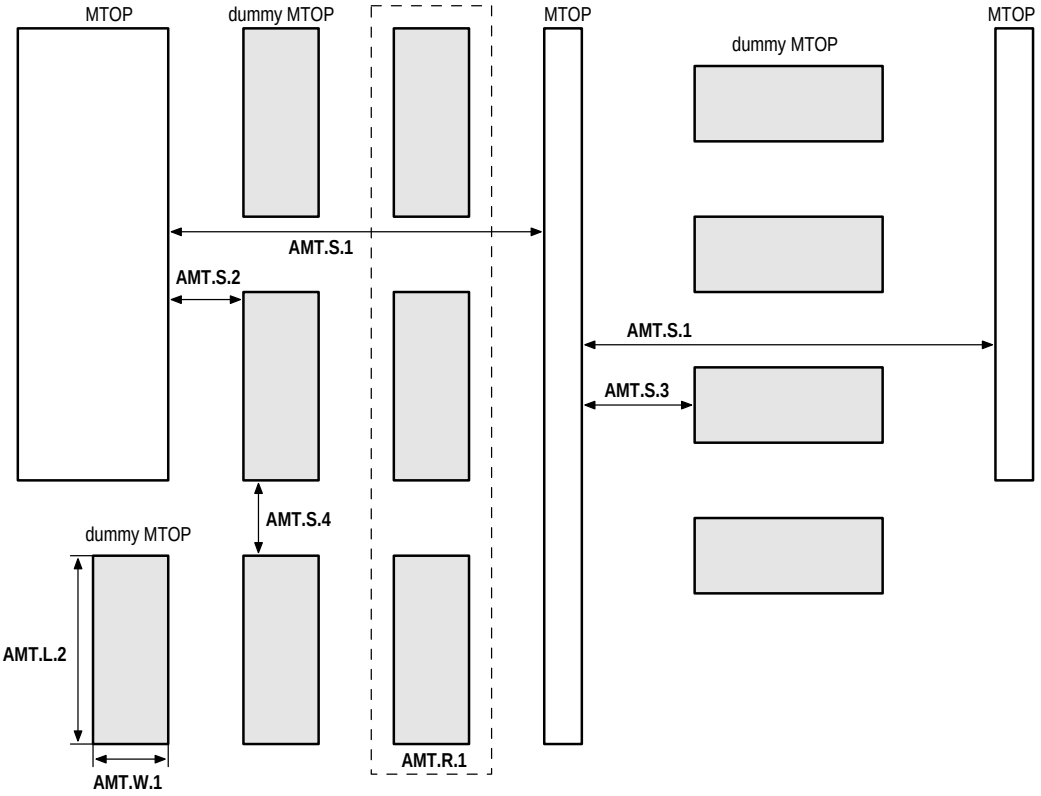
8.1 Top Metal Dummy Structures

Rule	Description	Value [um]
AMT.S.1	Maximum MTOP spacing when the width of one or both MTOP shapes is less than 10um.	10

To meet AMT.S.1 the following dummy structures must be added in the top metal layer as an assembly stress buffer:

Guideline	Description	Value [um]
AMT.W.1	Fixed width of dummy MTOP block	2
AMT.L.1	Fixed length of dummy MTOP block	5
AMT.S.2	Minimum MTOP feature to dummy MTOP block spacing	2
AMT.S.3	Maximum MTOP feature to dummy MTOP block spacing	6
AMT.S.4	Fixed dummy MTOP block spacing	2
AMT.R.1	Minimum number of dummy MTOP blocks in a region	3

Note: Automatic filling with dummy MTOP blocks can be suppressed with layer NOFILL.

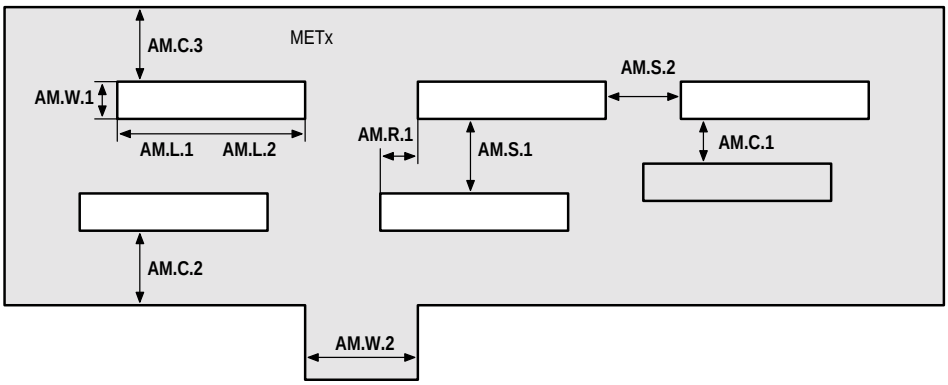


8.2 Metal Slots

Slots must be inserted to release stress in wide metal (> 35um):

Rule	Description	Value [um]
AM.W.0	Maximum METx width	35
AM.W.1	Fixed slot width	3
AM.L.1	Minimum slot length	30
AM.L.2	Maximum slot length	300
AM.S.1	Minimum spacing between two parallel slots	10
AM.S.2	Minimum spacing between two slots in a sequence	10

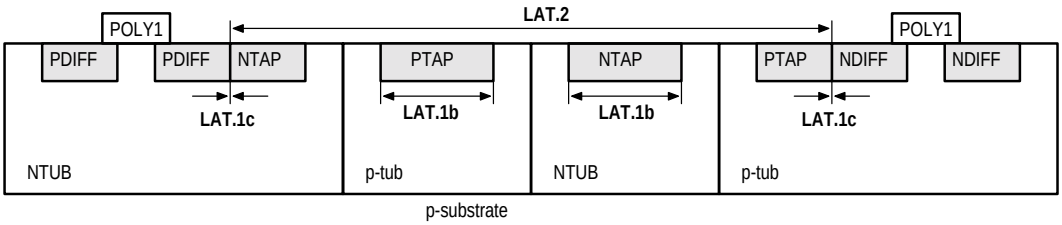
Guideline	Description	Value [um]
AM.C.1	Minimum slots spacing between neighbor layers (i.e.: MET1 / MET2, MET2 / MET3, MET3 / MET4)	2
AM.C.2	Minimum slot to inner metal edge spacing	10
AM.C.3	Minimum slot to outer metal edge spacing	10
AM.W.2	Minimum width of METx connected to wide METx with slots No slot is allowed opposite this metal	10
AM.R.1	Starting position of parallel slots should be staggered.	
AM.R.2	Slot must be parallel to the current direction.	

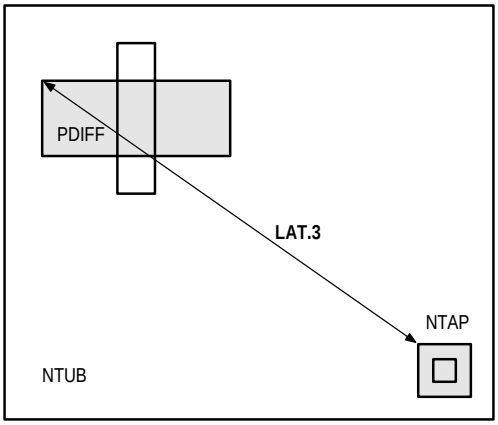


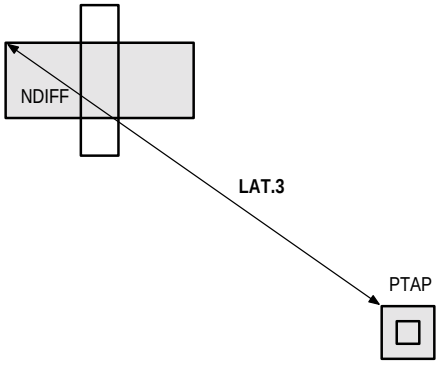
Note: The cell CORNER is available to insert slots in buses at die corners.

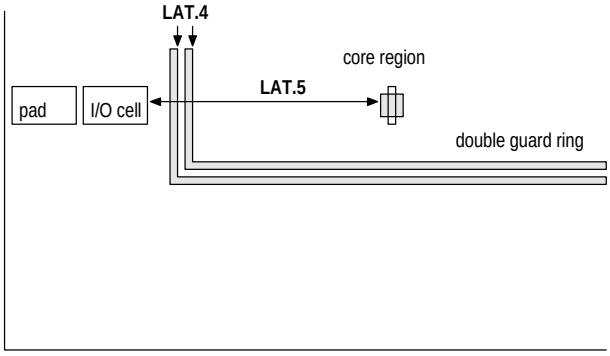
9 Latch-up Prevention

Guideline	Description	Value [um]
LAT.1a	A double guard ring structure should be inserted in between NMOS and PMOS of I / O buffers	
LAT.1b	Minimum PTAP and NTAP guard ring width for I / O buffers	3
LAT.1c	Maximum distance from PTAP or NTAP guard ring to source DIFF for I / O buffers	2
LAT.2	Minimum NMOS to PMOS spacing for I / O buffers and ESD devices Active DIFF area in this spacing is not allowed.	40
LAT.3	Maximum distance from any point inside source / drain DIFF to the nearest TAP DIFF of the same NTUB or PSUB.	20
LAT.4	A guard ring structure with NTUB pseudo-collector and PTAP should be inserted between I / O buffers and internal circuit area	
LAT.5	Minimum I / O buffer to internal circuit spacing	50
LAT.6	Any HOT_NDIFF area connecting to I / O pads should be surrounded by double guard ring.	
LAT.7	Any NTUB without direct connection to VDD and with HOT_NDIFF inside it should be surrounded by double guard ring.	
LAT.8	For special devices such as bipolar transistor, diode, resistor, or special circuits such as charge pump, power regulator, high noise or high power circuitry, a double guard ring should be inserted surrounding and between them.	
LAT.9	All the guard rings and pickups should be connected to VDD / VSS with very low series resistance. That is, NTUB should be tied together with NTAP, and DIFF should be tied together with contacts and metal to VDD / VSS. As many as possible CONT should be used.	


LAT.2
POLY1
POLY1
PDIFF
PDIFF
NTAP
PTAP
NTAP
PTAP
NDIFF
NDIFF
LAT.1c
LAT.1b
LAT.1b
LAT.1c
NTUB
p-tub
NTUB
p-tub
p-substrate


PDIFF
LAT.3
NTAP
NTUB


NDIFF
LAT.3
PTAP


LAT.4
core region
LAT.5
pad
I/O cell
double guard ring

10 Support

For questions on process parameters please refer to:

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