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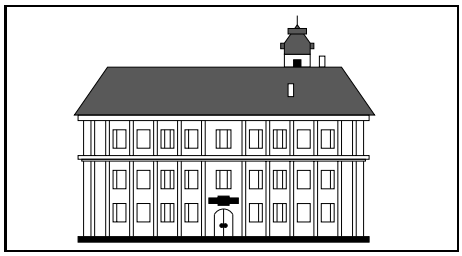

0.35 µm CMOS Design Rules

7 Digit Document #: **9931032**

Revision #: **2.0**

Document control

Controlled Copy # ____

Strictly Controlled

Version History

Version	Description
1.0 = Rev. N/C	
2.0	1. Change version control (A -> 2.0) 2. Guideline: Ratio of POLY1 area to die area 3. Changed Minimum pad pitch

Process Family

This document is valid for the following twin-tub 0.35 µm processes:

process name	no. of mask layers	CMOS core module*	poly capacitor module	5 Volt option
CSA	13	x		
CSD	14	x	x	
CSF	14	x		x
CSI	15	x	x	x

*) p-substrate, triple metal, single poly, 3.3 Volt

Related Documents

0.35 µm CMOS Process Parameters: Doc. 9933016
ESD Design Rules: Doc. 9931020
Standard Family Cells: Doc. 9931021
Assembly Related Design Rules: Doc. 9981005

Note

All data represent drawn dimensions. Graphical illustrations are not to scale.

Support

Technical questions on design rules should be directed to the following department:

Process Characterization: e-mail: rules@amsint.com
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Table of Contents

1. Definitions

Mask Layers

NTUB	WN	:=	n-tub layer
DIFF	DF	:=	diffusion layer
FIMP	IF	:=	n-field implant layer
MIDOX	XM	:=	mid gate oxide layer ($V_{GATE} > 3.3Volt$)
POLY1	P1	:=	poly1 layer
POLY2	P2	:=	poly2 layer
NPLUS	IN	:=	n+implant layer
PPLUS	IP	:=	p+implant layer
CONT	CT	:=	contact layer (connects MET1 to DIFF, POLY1, POLY2)
MET1	M1	:=	metal1 layer
M1HOLE	M1	:=	metal1 slot (metal1 = MET1 and not M1HOLE)
VIA	VI	:=	via1 layer (connects MET2 to MET1)
MET2	M2	:=	metal2 layer
M2HOLE	M2	:=	metal2 slot (metal2 = MET2 and not M2HOLE)
VIA2	V2	:=	via2 layer (connects MET3 to MET2)
MET3	M3	:=	metal3 layer
M3HOLE	M3	:=	metal3 slot (metal3 = MET3 and not M3HOLE)
PAD	PA	:=	pad layer

Note: The 2-character symbols are used for short rule names.

Definition Layers

These layers are not used in chip production.
They are necessary for design tools, e.g. design rule check.

CAPDEF	:=	defines sandwich capacitors
DIFCUT	:=	excludes DIFF from device extraction
DIODE	:=	marks protection diodes for device extraction
PO1CUT	:=	excludes dummy POLY1 from device extraction
PO2CUT	:=	excludes dummy POLY2 from device extraction
RESDEF	:=	resistor definition layer
RESTRM	:=	resistor terminal layer
SFCDEF	:=	excludes SFC from checks and automatic layer generation
ZENER	:=	excludes Zener diodes from checks and automatic layer generation

Structures

DIFFCON := diffusion contact (CONT & DIFF)
DIFFM := diffusion for 5 volt operation (DIFF & MIDOX)
NDIFF (DN) := n+diffusion (DIFF & NPLUS)
NDIFFCON := n+diffusion contact (CONT & NDIFF)
PADVIA1 := VIA underneath PAD (VIA & PAD)
PADVIA2 := VIA2 underneath PAD (VIA2 & PAD)
PDIFF (DP) := p+diffusion (DIFF & PPLUS)
PDIFFCON := p+diffusion contact (CONT & PDIFF)
POLY1CON := poly1 contact (CONT & POLY1)
POLY2CON := poly2 contact (CONT & POLY2)
PSUB := p-substrate
SCRIBE := scribe line border (Peripheral bus + scribe edge, example in SFC)
SCRIBECUT := scribe line border cut (example in SFC)
SFC := standard family cells
WIDE_MET1 := MET1 width and length $>$ 10 µm
WIDE_MET2 := MET2 width and length $>$ 10 µm
WIDE_MET3 := MET3 width and length $>$ 10 µm

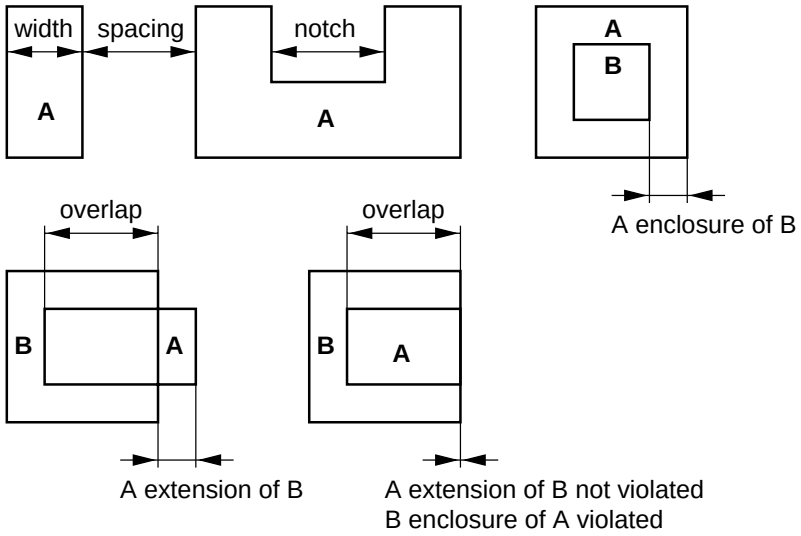
Elements

CORNER := corner cell with slotted metal busses
CPOLY := poly1-poly2 capacitor (POLY1 & POLY2)
LAT2 := lateral PNP transistor (2 µm x 2 µm emitter)
SUBDIODE := parasitic n+p- diode (NDIFF & PSUB & DIODE)
NMOS := n-channel MOSFET
NMOSM := n-channel MOSFET with mid gate oxide
NMOSH := high voltage n-channel MOSFET
NWD := parasitic n-p- diode (NTUB & PSUB & DIODE)
WELLDIODE := parasitic p+n- diode (PDIFF & NTUB & DIODE)
PMOS := p-channel MOSFET
PMOSM := p-channel MOSFET with mid gate oxide
RDIFFP3 := p+diffusion resistor in periphery cells (PDIFF & RESDEF)
RNWELL := n-tub resistor (NTUB & RESDEF)
RPOLY2 := poly2 resistor (POLY2 & RESDEF)
VERT10 := vertical PNP transistor (10 µm x 10 µm emitter)

Geometric Relations

A width	WnA	:=	distance inside_A - inside_A
A spacing to B	SnAB	:=	distance outside_A - outside_B (different polygons)
A notch	SnAA	:=	distance outside_A - outside_A (same polygon)
A enclosure of B	EnAB	:=	distance inside_A - outside_B (A contains B)
A extension of B	EnAB	:=	distance inside_A - outside_B (A may intersect B)
A overlap of B	OnAB	:=	distance inside_A - inside_B

Note: The abbreviations are intended for short design rule names.



2. General Requirements

RUL001	Grid	0.05 µm
RUL002	Corners	90 °, 135 °
RUL003	Data extrema including SCRIBE	integral multiple of 5 µm

3. Process Layer Overview

Note: Width and spacing are minimum values in µm.

	layer	GDS#	width	spacing / notch	generation
rule#		N1y	W1y	S1yy	
Mask Layers					
yWN	NTUB	5	2.0	3.0	drawn
yIF	FIMP	8			=NTUB (except SFC)
yDF	DIFF	10	0.5	0.6	drawn
yXM	MIDOX	14	0.6	0.6	drawn
yP1	POLY1	20	0.3	0.6	drawn
yIN	NPLUS	23	0.6	0.6	drawn
yIP	PPLUS	24	0.6	0.6	drawn
yP2	POLY2	30	0.7	0.5	drawn
yCT	CONT	34	0.4	0.5	drawn
yM1	MET1	35	0.4	0.6	drawn
yVI	VIA	36	0.5	0.5	drawn
yM2	MET2	37	0.5	0.6	drawn
yV2	VIA2	38	0.5	0.5	drawn
yM3	MET3	39	0.5	0.7	drawn
yPA	PAD	40	15.0	15.0	drawn
	M1HOLE	57			MET1 slots
	M2HOLE	58			MET2 slots
	M3HOLE	61			MET3 slots
Definition Layers					
	SFCDEF	42			SFC
	ZENER	43			Zener diodes
	DIFCUT	44			non-standard DIFF
	PO1CUT	45			non-standard POLY1
	PO2CUT	46			non-standard POLY2
	DIODE	47			parasitic diodes
	RESDEF	49			resistors
	RESTRM	50			resistor terminals
	CAPDEF	55			sandwich capacitors

e.g.: MET1 width = W1M1, MET1 spacing = S1M1M1.

4. Structure Rules

4.1. NDIFF

S1INIP Overlap of NPLUS and PPLUS is not allowed (except ZENER)

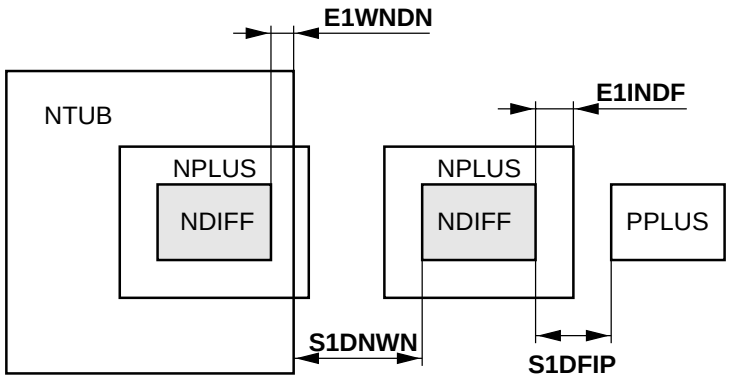
BAD1DF DIFF without NPLUS or PPLUS is not allowed (except ZENER)

E1INDF Minimum NPLUS extension of DIFF ..... 0.3 µm

S1DFIP Minimum DIFF spacing to PPLUS ..... 0.3 µm

S1DNWN Minimum NDIFF spacing to NTUB ..... 1.2 µm

E1WNDN Minimum NTUB enclosure of NDIFF ..... 0.2 µm



4.2. PDIFF

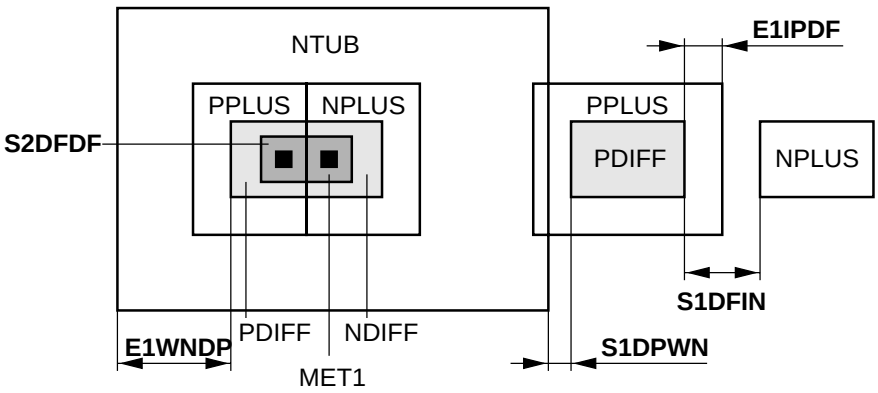
E1IPDF Minimum PPLUS extension of DIFF ..... 0.3 µm

S1DFIN Minimum DIFF spacing to NPLUS ..... 0.3 µm

S1DPWN Minimum PDIFF spacing to NTUB ..... 0.4 µm

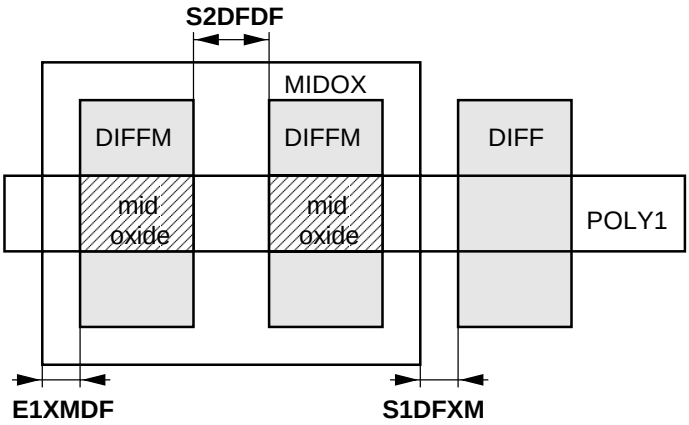
E1WNDP Minimum NTUB enclosure of PDIFF ..... 1.2 µm

BAD2DF NDIFF and butting PDIFF must be connected with MET1



4.3. MIDOX

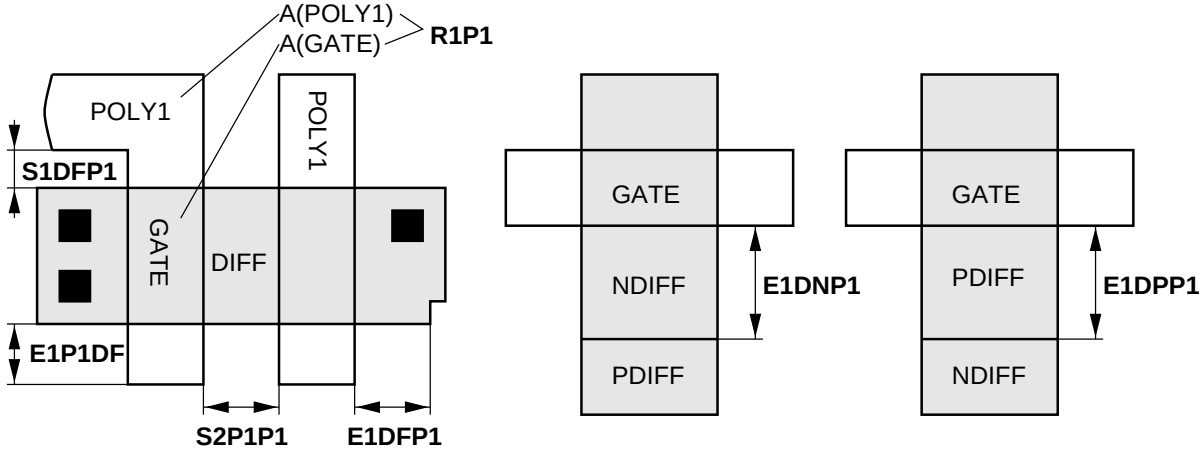
E1XMDF Minimum MIDOX enclosure of DIFFM . . . . . 0.6 µm
S1DFXM Minimum MIDOX spacing to DIFF . . . . . 0.6 µm
S2DFDF Minimum DIFFM spacing . . . . . 1.0 µm



4.4. POLY1, GATE

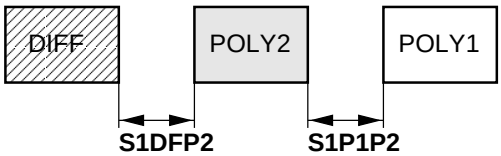
S2P1P1	Minimum GATE spacing	0.7 µm
S1DFP1	Minimum POLY1 spacing to DIFF	0.3 µm
E1P1DF	Minimum POLY1 extension of GATE	0.4 µm
E1DFP1	Minimum DIFF extension of GATE	0.7 µm
E1DNP1	Minimum NDIFF extension of GATE when butted to PDIFF	0.6 µm
E1DPP1	Minimum PDIFF extension of GATE when butted to NDIFF	0.6 µm
R1P1	Maximum ratio of POLY1 area to touched GATE area	100

Note: POLY1 structures collect electric charge during ion-etching which can be a hazard for associated GATE oxide.



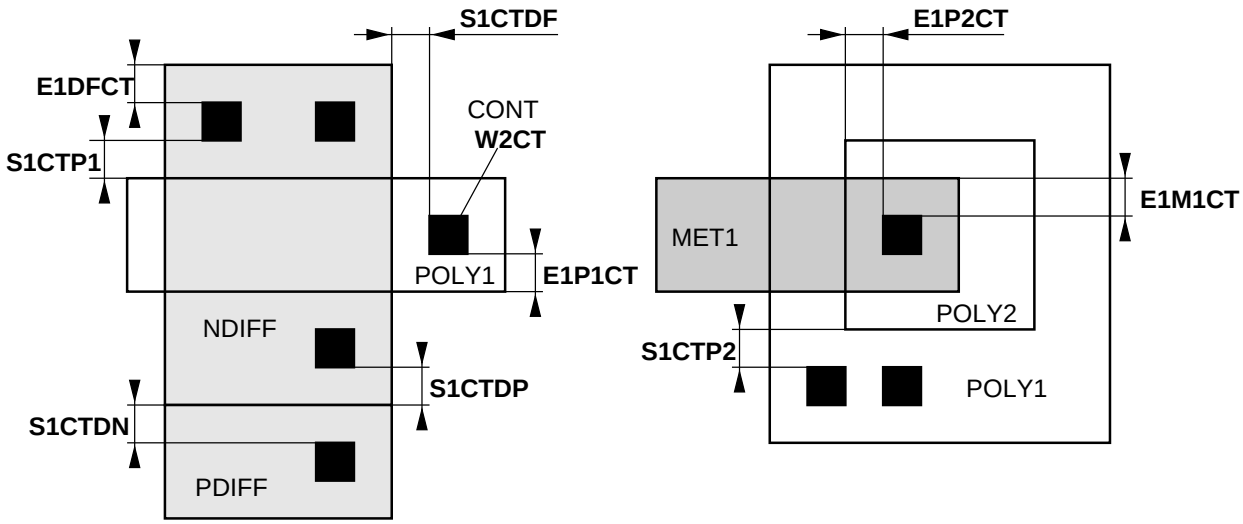
4.5. POLY2

BAD1P2	POLY2 is not allowed over DIFF	
S1DFP2	Minimum POLY2 spacing to DIFF	0.3 µm
S1P1P2	Minimum POLY1 spacing to POLY2	0.7 µm



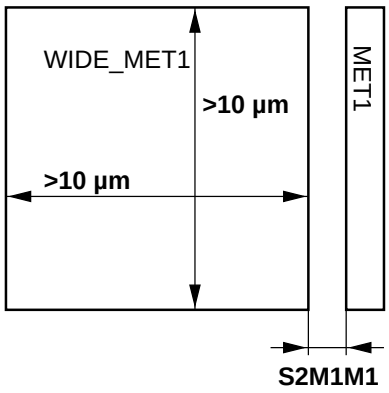
4.6. CONT

BAD1CT	CONT without MET1 is not allowed	
BAD2CT	CONT without DIFF or POLY1 or POLY2 is not allowed	
BAD3CT	POLY1CON is not allowed over DIFF	
W2CT	Fixed CONT size	0.4 µm x 0.4 µm
E1M1CT	Minimum MET1 enclosure of CONT	0.1 µm
E1DFCT	Minimum DIFF enclosure of CONT	0.3 µm
E1P1CT	Minimum POLY1 enclosure of CONT	0.2 µm
E1P2CT	Minimum POLY2 enclosure of CONT	0.6 µm
S1CTP1	Minimum DIFFCON spacing to GATE	0.4 µm
S1CTDP	Minimum NDIFFCON spacing to PDIFF	0.4 µm
S1CTDN	Minimum PDIFFCON spacing to NDIFF	0.4 µm
	Note: Butting CONTs are not allowed.	
S1CTDF	Minimum POLY1CON spacing to DIFF	0.4 µm
S1CTP2	Minimum POLY1CON spacing to POLY2	1.4 µm



4.7. MET1

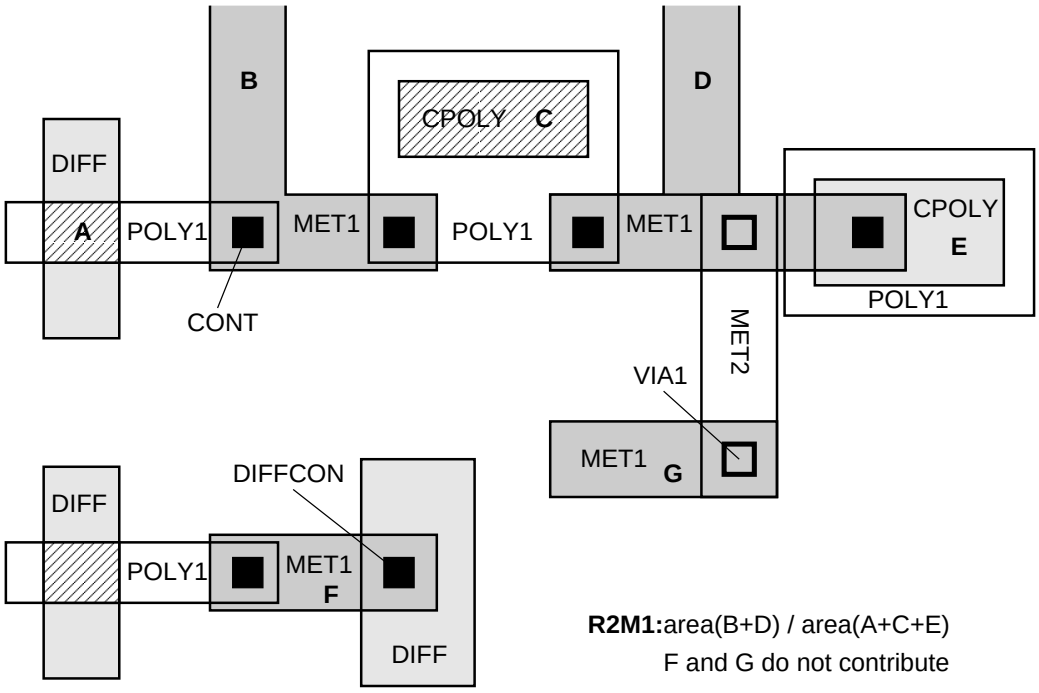
S2M1M1 Minimum MET1 spacing to WIDE_MET1 ..... 1.0 µm



R1M1 Minimum ratio of MET1 area to die area ..... 30 %

R2M1 Maximum ratio of MET1 area to connected GATE and CPOLY area 100

Note: MET1 structures collect electric charge during ion-etching which can be a hazard for associated GATE and CPOLY oxide. Only MET1 without DIFFCONs must be considered. MET1 connected to GATE or CPOLY via MET2 and shorted CPOLY does not contribute.



R2M1:area(B+D) / area(A+C+E)
F and G do not contribute

BAD1M1 Insert slots in MET1 $>$ 20 µm $\times$ 300 µm

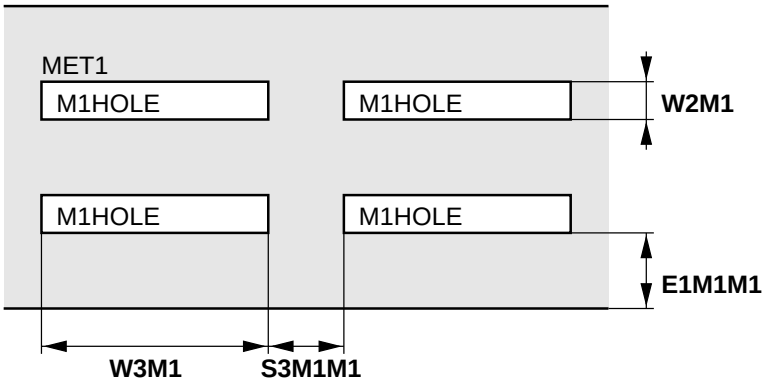
Note: Insert M1HOLEs in direction of current flow. Standard cells do not contain M1HOLEs.

W2M1 Minimum M1HOLE width . . . . . 1.0 µm

W3M1 Minimum M1HOLE length . . . . . 10.0 µm

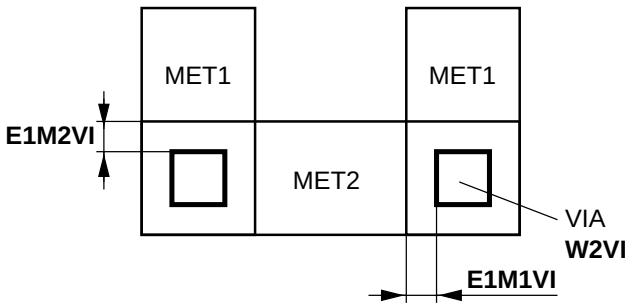
S3M1M1 Minimum M1HOLE spacing on MET1 . . . . . 10.0 µm

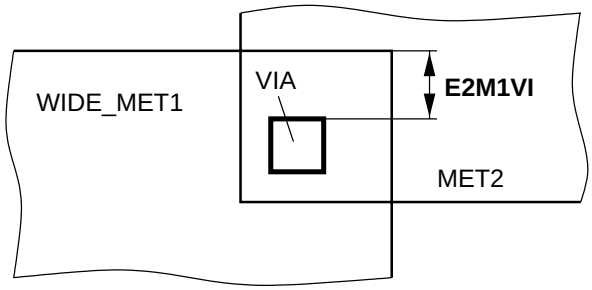
E1M1M1 Minimum MET1 enclosure of M1HOLE . . . . . 9.0 µm



4.8. VIA

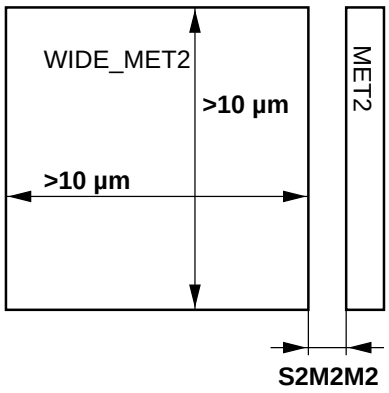
BAD1VI	VIA without MET1 is not allowed	
BAD2VI	VIA without MET2 is not allowed	
BAD3VI	VIA over GATE is not allowed	
W2VI	Fixed VIA size	0.5 µm x 0.5 µm
E1M1VI	Minimum MET1 enclosure of VIA	0.2 µm
E1M2VI	Minimum MET2 enclosure of VIA	0.1 µm
E2M1VI	Minimum WIDE_MET1 enclosure of VIA	0.6 µm





4.9. MET2

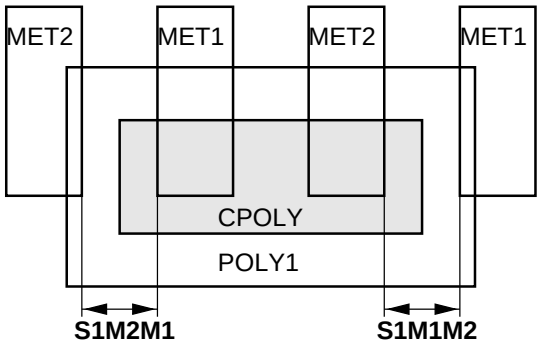
S2M2M2 Minimum MET2 spacing to WIDE_MET2 ..... 1.1 µm



BAD1M2 Stacking MET2, MET1, POLY2, POLY1 is not allowed

S1M2M1 Minimum MET2 spacing to MET1 over CPOLY ..... 1.4 µm

S1M1M2 Minimum MET1 spacing to MET2 over CPOLY ..... 1.4 µm



R1M2 Minimum ratio of MET2 area to die area ..... 30 %

R2M2 Maximum ratio of MET2 area to connected GATE and CPOLY area 100

Note: MET2 structures collect electric charge during ion-etching which can be a hazard for associated GATE and CPOLY oxide. Only MET2 without DIFFCONs must be considered. MET2 connected to GATE or CPOLY via MET3 and shorted CPOLY does not contribute.

BAD2M2 Insert slots in MET2 $>$ 20 µm $\times$ 300 µm

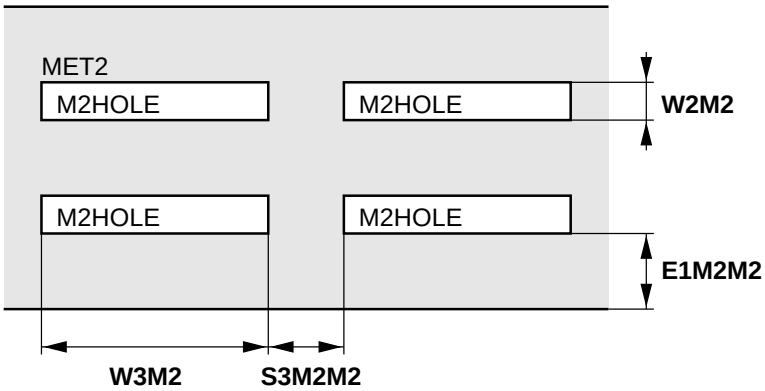
Note: Insert M2HOLEs in direction of current flow. Standard cells do not contain M2HOLEs.

W2M2 Minimum M2HOLE width . . . . . 1.1 µm

W3M2 Minimum M2HOLE length . . . . . 10.0 µm

S3M2M2 Minimum M2HOLE spacing on MET2 . . . . . 10.0 µm

E1M2M2 Minimum MET2 enclosure of M2HOLE . . . . . 9.0 µm



4.10. VIA2

BAD1V2 VIA2 without MET2 is not allowed

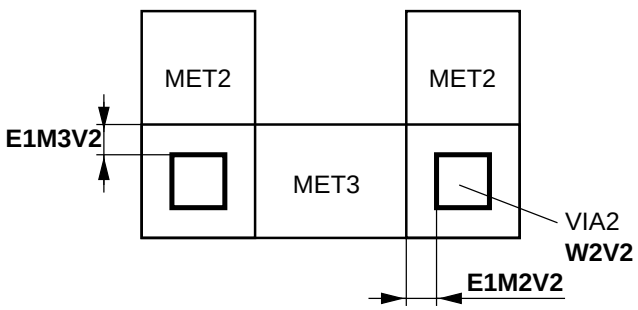
BAD2V2 VIA2 without MET3 is not allowed

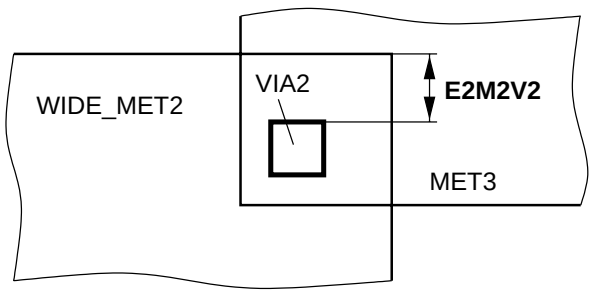
W2V2 Fixed VIA2 size . . . . . 0.5 µm x 0.5 µm

E1M2V2 Minimum MET2 enclosure of VIA2 . . . . . 0.2 µm

E1M3V2 Minimum MET3 enclosure of VIA2 . . . . . 0.1 µm

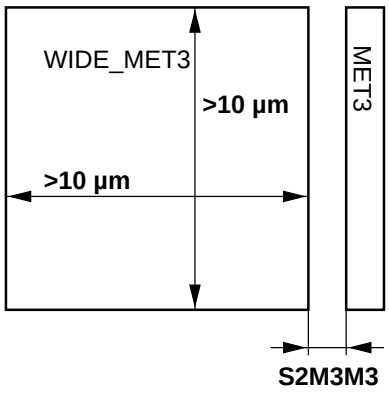
E2M2V2 Minimum WIDE_MET2 enclosure of VIA2 . . . . . 0.6 µm





4.11. MET3

S2M3M3 Minimum MET3 spacing to WIDE_MET3 ..... 1.2 µm



R1M3 Minimum ratio of MET3 area to die area ..... 30 %

R2M3 Maximum ratio of MET3 area to connected GATE and CPOLY area 100

Note: MET3 structures collect electric charge during ion-etching which can be a hazard for associated GATE and CPOLY oxide. Only MET3 without DIFFCONs must be considered. MET3 connected to shorted GATE or CPOLY does not contribute.

BAD1M3 Insert slots in MET3 $>$ 20 µm $\times$ 300 µm

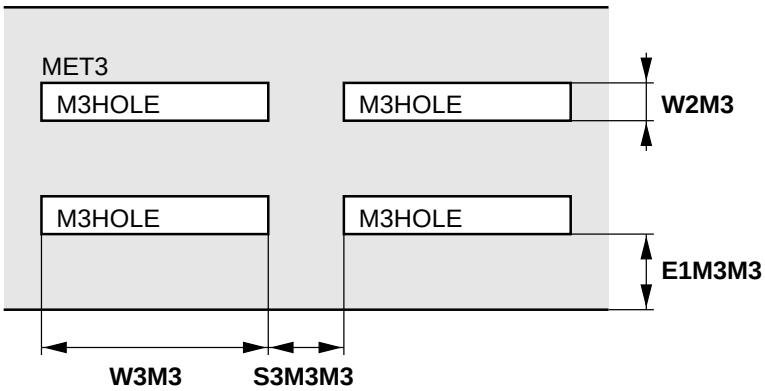
Note: Insert M3HOLEs in direction of current flow. Standard cells do not contain M3HOLEs.

W2M3 Minimum M3HOLE width ..... 1.2 µm

W3M3 Minimum M3HOLE length ..... 10.0 µm

S3M3M3 Minimum M3HOLE spacing on MET3 ..... 10.0 µm

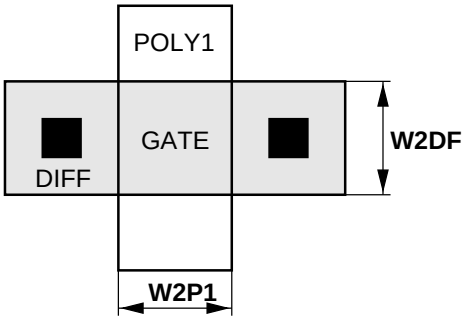
E1M3M3 Minimum MET3 enclosure of M3HOLE ..... 9.0 µm



5. Element Rules

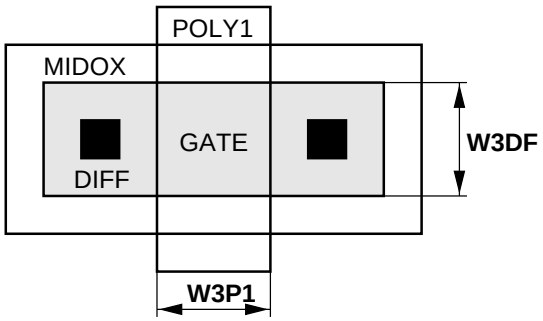
5.1. NMOS, PMOS

W2P1 Minimum GATE length . . . . . 0.3 µm
W2DF Minimum GATE width . . . . . 0.6 µm



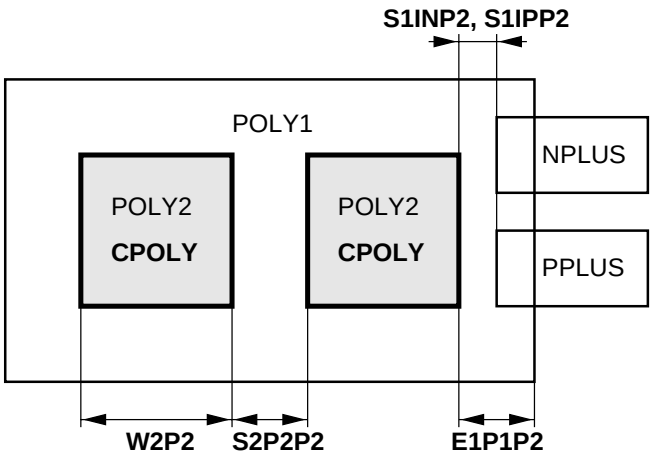
5.2. NMOSM, PMOSM

W3P1 Minimum GATE length . . . . . 0.5 µm
W3DF Minimum GATE width . . . . . 0.6 µm



5.3. CPOLY

BAD1IN	CPOLY is not allowed over NPLUS	
BAD1IP	CPOLY is not allowed over PPLUS	
W2P2	Minimum CPOLY width	0.8 µm
S2P2P2	Minimum CPOLY spacing	0.8 µm
E1P1P2	Minimum POLY1 enclosure of POLY2	1.0 µm
S1INP2	Minimum NPLUS spacing to CPOLY	1.0 µm
S1IPP2	Minimum PPLUS spacing to CPOLY	1.0 µm



Note: See chapter 8. for recommended layout structure of CPOLY.
Precision capacitor matching is improved with non-minimum POLY2 width and spacing.

5.4. RPOLY2, RNWELL

BAD2IN RPOLY2 is not allowed over NPLUS

BAD2IP RPOLY2 is not allowed over PPLUS

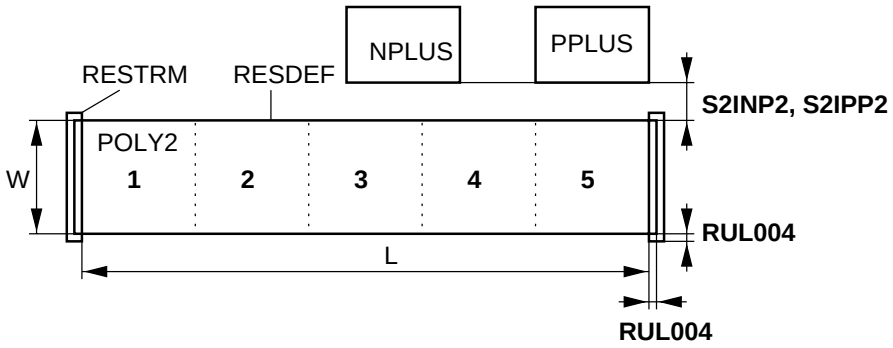
S2INP2 Minimum NPLUS spacing to RPOLY2 ..... 0.5 µm

S2IPP2 Minimum PPLUS spacing to RPOLY2 ..... 0.5 µm

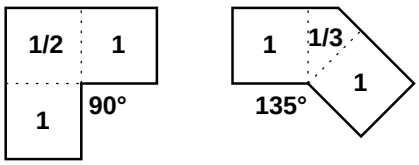
RUL004 Fixed RESTRM enclosure of RESDEF edge ..... 0.1 µm

Note: RESDEF and RESTRM are necessary for all resistors.

Note: Recommended minimum number of squares ..... L/W $\geq$ 5

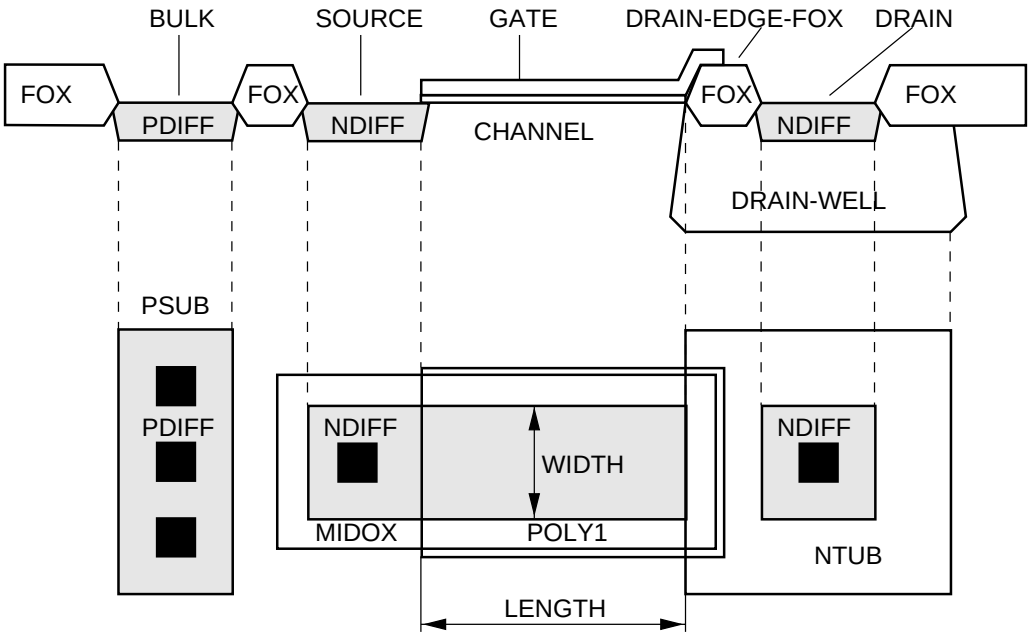


Note: Use the following effective number of squares for resistance calculation of corners:



Note: See chapter 8. for recommended layout structure of poly resistors.

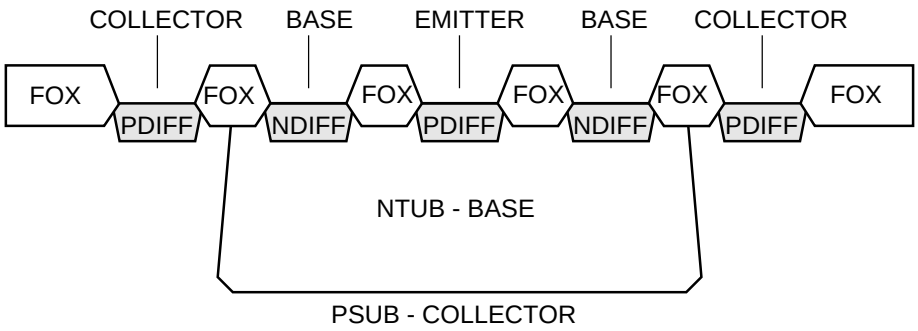
5.5. NMOSH



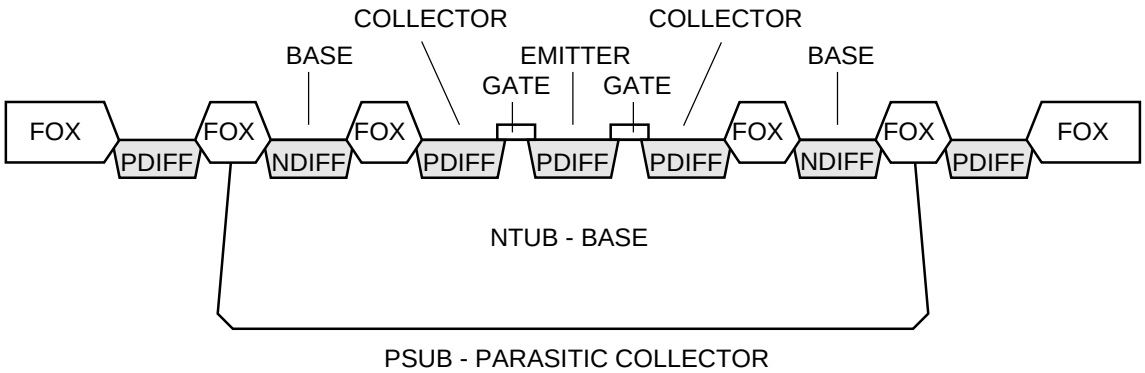
Note: The layout of NMOSH is predefined and available on request.
Only WIDTH may be changed.

5.6. VERT10, LAT2

VERT10

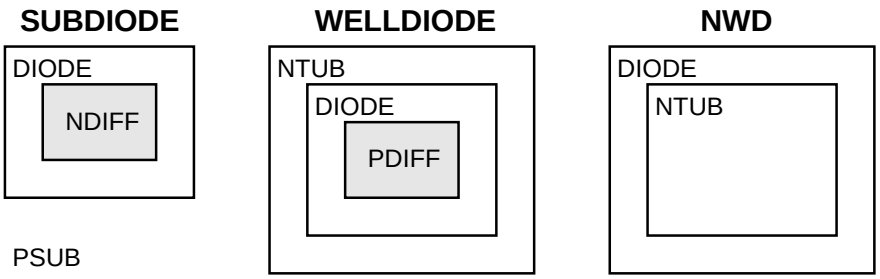


LAT2



Note: The layouts of VERT10 and LAT2 are predefined and available on request. They must not be changed.

5.7. SUBDIODE, WELLDIODE, NWD



Note: SUBDIODE, WELLDIODE, NWD are only intended for the simulation of reverse leakage currents and junction capacitances in periphery cells. It is not recommended to use these diodes as active circuit elements.

6. Periphery Rules

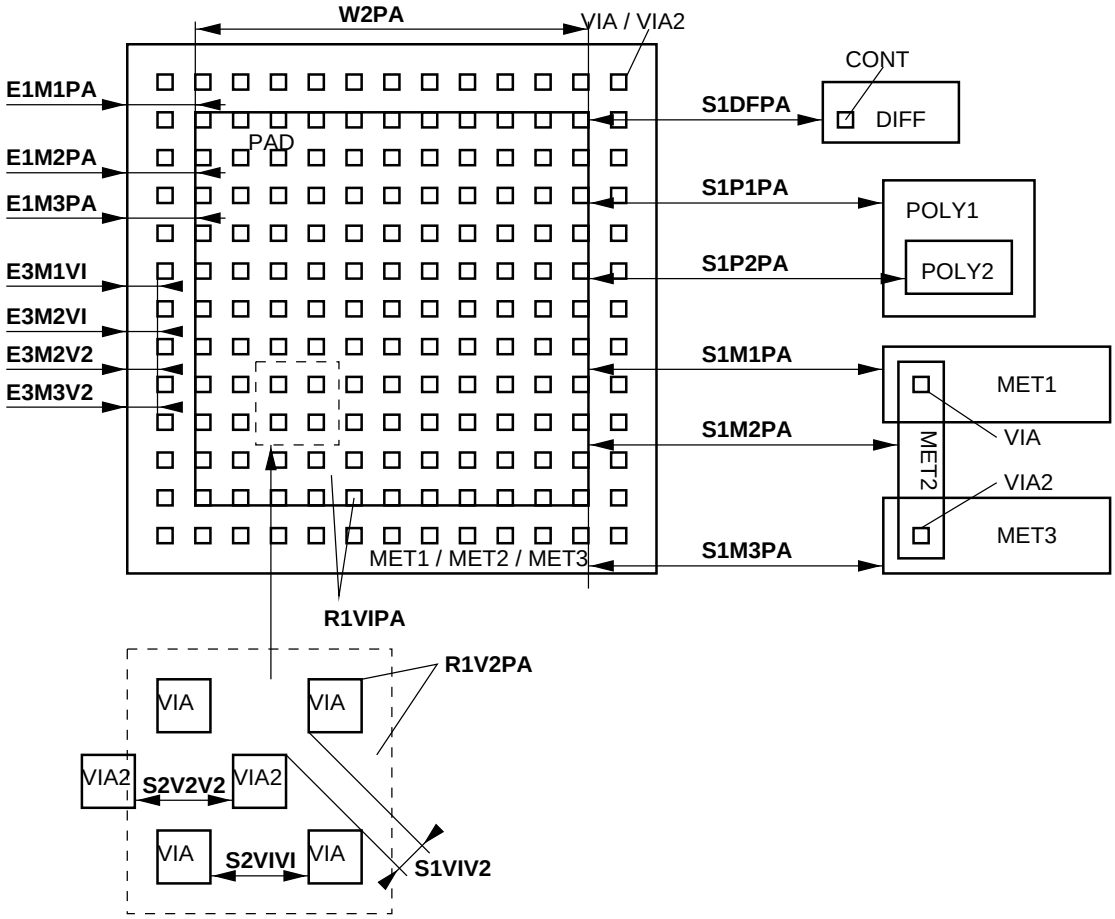
ESD Related Rules: See Doc. 9931020.

6.1. PAD Rules

BAD1PA	PAD is not allowed over DIFF	
BAD2PA	PAD is not allowed over POLY1	
BAD3PA	PAD is not allowed over POLY2	
BAD3V2	PADVIA2 over PADVIA1 is not allowed	
W2PA	Bond PAD size	85.0 µm x 85.0 µm

Note: Test PAD size 60 µm x 60 µm. Probe PAD size 15 µm x 15 µm.
Bond pads and test pads must have a minimum pitch of 100 µm.
The following rules are only valid for bond pads.

E1M1PA	Minimum MET1 enclosure of PAD	5.0 µm
E1M2PA	Minimum MET2 enclosure of PAD	5.0 µm
E1M3PA	Minimum MET3 enclosure of PAD	5.0 µm
E3M1VI	Minimum MET1 enclosure of PADVIA1	3.0 µm
E3M2VI	Minimum MET2 enclosure of PADVIA1	3.0 µm
E3M2V2	Minimum MET2 enclosure of PADVIA2	3.0 µm
E3M3V2	Minimum MET3 enclosure of PADVIA2	3.0 µm
S2VIVI	Minimum PADVIA1 spacing	0.8 µm
S2V2V2	Minimum PADVIA2 spacing	0.8 µm
S1VIV2	Minimum PADVIA2 spacing to PADVIA1	0.3 µm
S1DFPA	Minimum PAD spacing to DIFF	10.0 µm
S1P1PA	Minimum PAD spacing to POLY1	10.0 µm
S1P2PA	Minimum PAD spacing to POLY2	10.0 µm
S1M1PA	Minimum PAD spacing to MET1 (different net)	10.0 µm
S1M2PA	Minimum PAD spacing to MET2 (different net)	10.0 µm
S1M3PA	Minimum PAD spacing to MET3 (different net)	10.0 µm
R1VIPA	Minimum ratio of PADVIA1 area to PAD area	5 %
R1V2PA	Minimum ratio of PADVIA2 area to PAD area	5 %


W2PA
VIA / VIA2
CONT
E1M1PA
S1DFPA
DIFF
PAD
E1M2PA
E1M3PA
S1P1PA
POLY1
E3M1VI
S1P2PA
POLY2
E3M2VI
E3M2V2
S1M1PA
MET1
E3M3V2
S1M2PA
VIA
MET2
VIA2
MET3
S1M3PA
MET1 / MET2 / MET3
R1VIPA
R1V2PA
VIA
VIA
VIA2
S2V2V2
VIA2
VIA
S2VIVI
VIA
S1VIV2

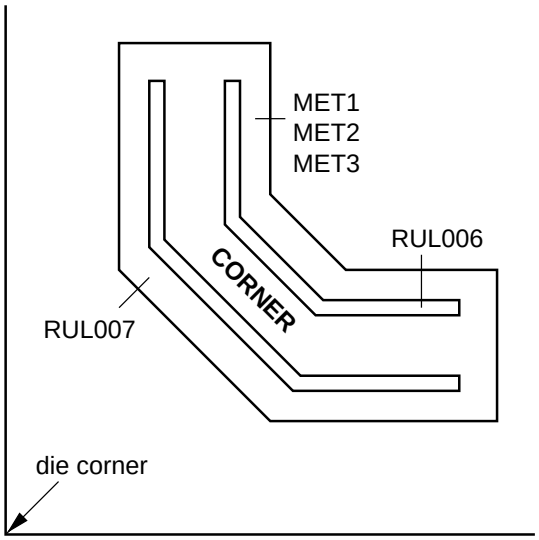
6.2. CORNER Rules

RUL005 CORNER must be used for die sizes $\geq$ 4mm $\times$ 4mm.

Note: This prevents cracks in corners of the die during thermal stress.

RUL006 Insert a continous 2 µm wide slot in $\geq$ 20 µm wide MET.

RUL007 Draw MET and slots at 45°.



Note: The layout of CORNER is predefined and available on request.

6.3. SCRIBE Rules

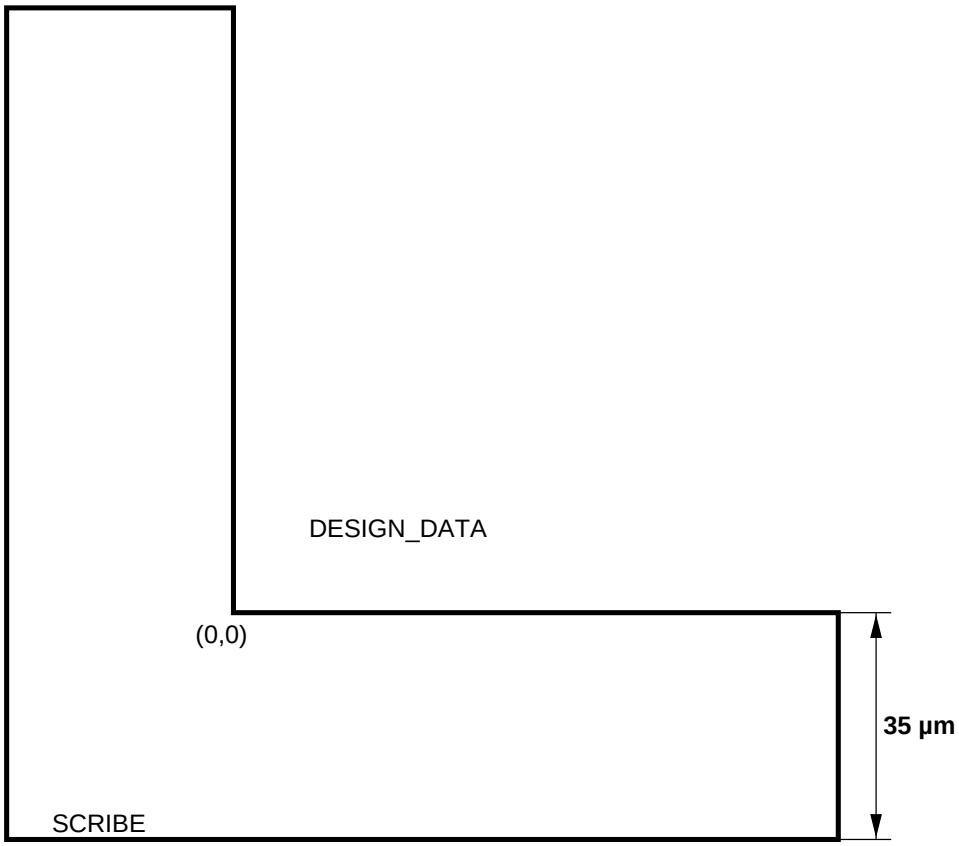
SCRIBE is a Standard Family Cell enclosing the design data. The inner edge of SCRIBE is butted to the data extrema of the design.

The SFC SCRIBE must be included in all designs without modification.

The SFC SCRIBECUT shows how to cut SCRIBE in mixed signal designs with separated supplies.

RUL008 Data extrema excluding SCRIBE ..... integral multiple of 5 µm

Note: Follows from rule RUL003 and SCRIBE width of 35.0 µm.



7. Guidelines

7.1 Connect NTUB with as much DIFFCON area as possible.
Maximum DIFFCON spacing ..... 50 µm

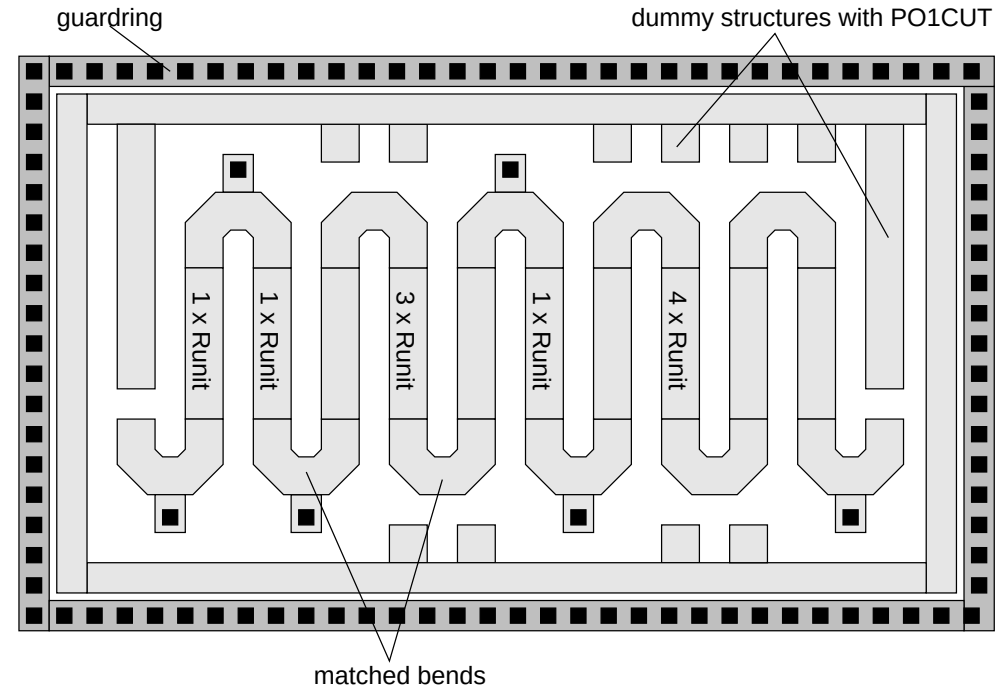
7.2 Where area permits non-minimum geometries should be used.

Note: This is particularly applicable to structures where the layout allows modifications without degrading circuit performance or increasing the overall size.

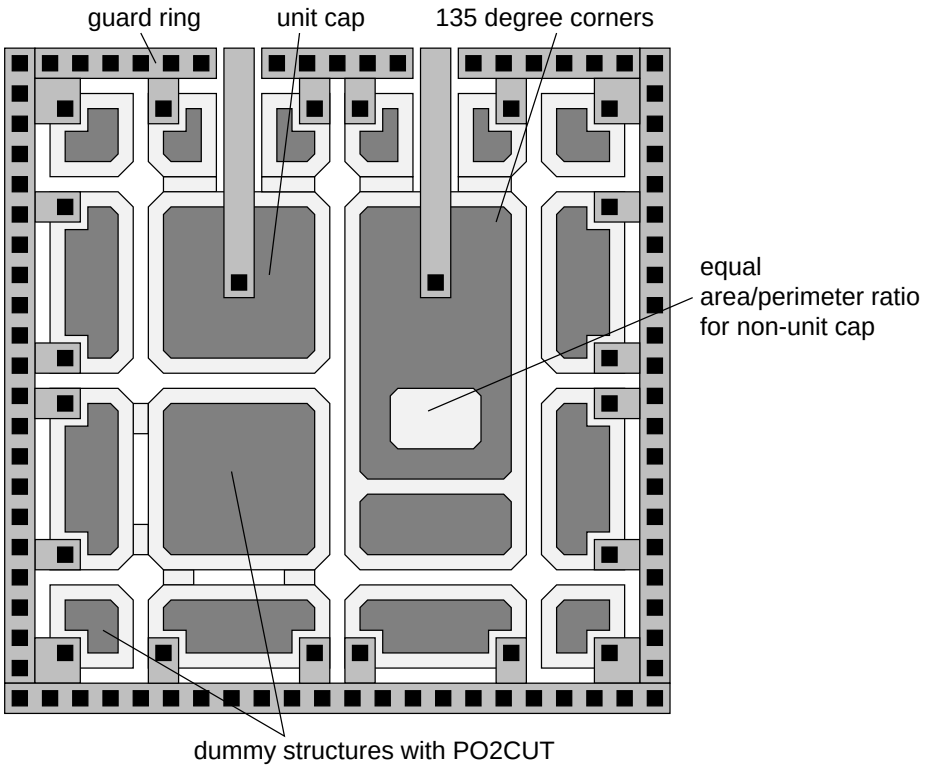
7.3 Minimum ratio of POLY1 area to die area ..... 14 %

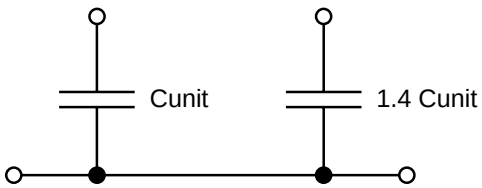
8. Recommended Layout Structures

Precision Resistors

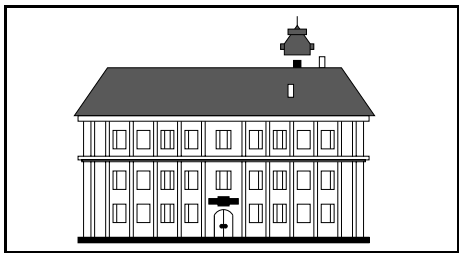


Precision Capacitors





Austria Mikro Systeme International AG



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0.35 µm CMOS Design Rules Attachment

7 Digit Document #: **9931032**

Revision #: **2.0**

Attachment to 7. Guidelines

7.4 Precision analog NMOS, PMOS, NMOSM, PMOSM should not be covered with MET1 or MET2. If this is not possible MET1 and MET2 covering of matching transistors should be identical.

7.5 Minimum channel length for critical analog NMOS transistors . . . . . 0.6 µm
Minimum channel length for critical analog NMOSM transistors . . . . . 1.0 µm

Note: Critical analog NMOS and NMOSM transistors are:

1. Transistors biased at ($Vth < V_{GS} < V_{DS}/2, V_{DS} = V_{DSmax}$).
   Low temperature applications are especially critical.
2. Transistors used in circuits sensitive to Vth shift.