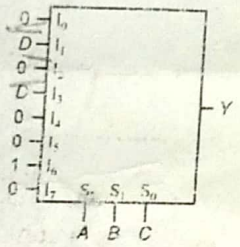
National Institute of Technology, Warangal

Department of Computer Science & Engineering
MCA, I-Semester
Computer Organization (CS5302)
Minor-I, Sept-2019

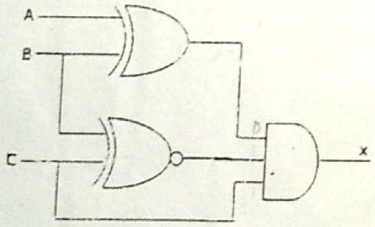
All Questions are compulsory. All the questions are having equal marks.

Time – 1 Hrs **Marks – 10**

1. Write the correct Minimization form of the given Boolean expression. **[1.5]**
$$(\bar{A}\bar{B}\bar{C} + \bar{A}B\bar{C} + \bar{A}BC + AB\bar{C})$$
2. 2's complement representation of a 16-bit number (one sign bit and 15 magnitude bit) is FFFF. Represent its magnitude in decimal form. **[2]**
3. The four variable function f is given in terms of min-terms as f(A, B, C, D) = $\sum m(2,3,8,10,11,12,14,15)$. Using the K-Map minimize the function in the sum of products form. Also give the realization using only two input NAND gates. **[2]**
4. An 8-to-1 multiplexer is used to implement a logical function Y as shown in the figure. Solve it for the correct output Y. **[1.5]**



5. How many minimum number of NAND gates are required to implement the Boolean Function $A + A\bar{B} + A\bar{B}C$? **[1.5]**
6. For the logic circuit shown in the figure, what is the required input combination (A, B, C) to make the output X = 1? **[1.5]**



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Department of Computer Science & Engineering
MCA, I-Semester
Computer Organization (CS5302)
Mid-Exam, Sept-2019

All Questions are compulsory.

Time – 2 Hrs **Marks – 30**

1. Consider a simple design of CPU having one Program Counter, Two General Purpose Registers, One Accumulator, One Data Register. Memory Address Register and Single Data Bus is connected with CPU along with Decoder and timing & control signals. Assume that CPU can execute 12 different instructions. Give proper justifications for the following questions:
   i) If every instruction has a size of 4 bytes, then what will be the value of PC for each instruction? [1]
   ii) Write the instructions and control signals generated by CPU when you will switch on the CPU first time. [1]
   iii) Control signals generated at machine states T0, T1 and T2. Give proper justification with the help of Assembly language code. [1]
   iv) CPU can perform only 12 different instructions, design a proper circuit which can decode all these instructions correctly. [2]
   v) As per your assumption (in case-iv), generate the timing and control signals for given instructions
      a) ADD R1
      b) MOV ACC, M
      c) MOV M, ACC [3]
   vi) Design a Micro-programmed control unit for timing and control signals as per your assumptions followed by above instruction format. [1]
   vii) Generate the timing and control signals according to the micro-programmed unit for given instructions (Software Solution for the given instructions):
      a) CMP
      b) AND R1 [1]
2. Explain why each of the following micro-operations cannot be executed during a single clock pulse in the system Specify a sequence of micro-operations that will perform the operation.
   a. IR ←M[PC]
   b. AC ←AC + R1
   c. DR ← DR + AC [3]

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National Institute of Technology, Warangal

Department of Computer Science & Engineering
MCA, I-Semester
Computer Organization (CS5302)
Minor-II, NOV-2019

All Questions are compulsory. All the questions are having equal marks.

Time – 1 Hrs **Marks – 10**

1. Based on Multiprogramming with Varibale Number of Tasks and Multiprogramming with Fixed Number of Tasks give a brief overview for given techniques:

   1) First Fit Algorithm
   2) Best Fit Algorithm
   3) Internal Fragmentation
   4) External Fragmentation
   5) Compaction [3]

2. Given page reference string: 1,2,3,4,2,1,5,6,2,1,2,3,7,6,3,2,1,2,3,6
   Compare the number of page faults for LRU, FIFO and Optimal page replacement algorithm with Hit Ratio. Consider 4 memory blocks are available. [3]

3. Consider a direct mapped cache of size 16 KB with block size 256 bytes. The size of main memory is 128 KB. Find-

   1) Number of bits in tag
   2) Tag directory size [2]

4. Consider a fully associative mapped cache of size 16 KB with block size 256 bytes. The size of main memory is 128 KB. Find-
   1) Number of bits in tag
   2) Tag directory size [2]

National Institute of Technology, Warangal

Department of Computer Science & Engineering
MCA, I-Semester
Computer Organization (CS5302)
Major Exam, 28-NOV-2019

All Questions are compulsory.

Time – 3 Hrs. **Marks – 50**

1. (a) Explain how a CPU supporting virtual memory would translate a virtual memory address into the actual memory address, assuming that the requested page is in memory. **[4]**

   (b) Explain what the CPU does when the requested page is not in memory? **[3]**

2. Consider the following C statement.

   if (!(a < b && b < c)) between = 0;

   (a) Rewrite the **if** condition to an equivalent condition without using the NOT operator **!**.**[3]**

   (b) What is the name of the Boolean algebra law that this illustrates? **[2]**

3. (a) Design a circuit with three inputs, and which outputs 1 precisely when at least two of the inputs are 1. **[4]**

   (b) The following truth table computes the 2's bit of the product of two 2-bit inputs. Draw a Karnaugh map and indicate a minimized sum-of-products expression corresponding to the Karnaugh map. (You do not need to draw the circuit.) **[5]**

x_1	x_0	y_1	y_0	p_1	x_1	x_0	y_1	y_0	p_1
0	0	0	0	0	1	0	0	0	0
0	0	0	1	0	1	0	0	1	1
0	0	1	0	0	1	0	1	0	0
0	0	1	1	0	1	0	1	1	1
0	1	0	0	0	1	1	0	0	0
0	1	0	1	0	1	1	0	1	1
0	1	1	0	1	1	1	1	0	1
0	1	1	1	1	1	1	1	1	0

4. A Computer System has a main memory consisting of 16M words. It also has a 32K-word cache organized in the block-set-associative manner, with 4 blocks per set and 128 words per block.

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a) Calculate the number of bits in each of the TAG, SET and WORD fields of the main memory address format. [4]

b) How will the main memory address look like for a fully associative mapped cache? [4]

5. A virtual memory system has an address space of 8K words, a memory space of 4K words and pages of 4K words having page and block size of 1K words. The following page references changes occur during a given time interval. 4, 2, 0, 1, 2, 6, 1, 4, 0, 1, 0, 2, 3, 5, 7.
Determine the four pages that resident in main memory after each page reference change if the replacement algorithm used is
i) LRU ii) Optimal iii) FIFO [6]

6. Consider a 4 stage pipeline processor. Calculate the number of cycles needed by the four instructions I1, I2, I3 and I4 in stages S1, S2, S3 and S4 is shown below-

	S1	S2	S3	S4
I1	2	1	1	1
I2	1	3	2	2
I3	2	1	1	3
I4	1	2	2	2

What is the number of cycles needed to execute the following loop?

for (i = 1 to 2) {I1; I2; I3; I4; } [6]

7. Consider a processor with 64-registers and an instruction set of size twelve. Each instruction has five distinct fields, namely, opcode, two source register identifiers, one destination register identifier, and a twelve-bit immediate value. Each instruction must be stored in memory in a byte-aligned fashion. If a program has 100 instructions, calculate the amount of memory (in bytes) consumed by the program text. [5]

8. Write a program to evaluate the arithmetic statement $Y = (A + B) * (C + D)$ using three-address, two-address, one-address and zero-address instructions. [4]

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