Lab X Topic
CSE 521 FPGA Design
Name: Coyote ID:

I Goals (give the objectives and purposes of this lab, the following are three examples)

1) Design RTL combinational circuit

2) Practice Verilog programming through circuit design

3) Get familiar with FPGA design

II Design Process (give the details of each steps in your design, should include some necessary components such as circuit analysis, circuit diagram, truth table, flowchart, module hierarchy, etc..)

III Program (provide detailed codes for each module and other source files)

IV Results (provide detailed results such as timing diagram, pictures of circuit implementation)

V Problem (what kind of problem have you met during the experiment, what is the reason for it and how did you solve it?)

VI What you learned