Lab 3 UART with Parity Bit

Demo is due on 7th, Mar., report is due on 9th, Mar.

Design a UART with a parity bit. It can be done by adding a parity state into the ASMD of the basic UART. In this new UART, a parity bit is included during transmission. The UART also has an error signal to indicate the parity error. Verify the new UART with hardware board.

1. Read the example codes for receiver and transmitter in a UART and learn how they work. Refer to the textbook listing 8.1 and 8.3.

2. Refer to the verification circuit for basic UART in textbook 8.4.2. Add a signal to indicate parity error using segment display.

3. Use a FIFO buffer to provide buffer space.

4. For the example codes of FIFO, refer to chapter 4.

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