EE/CE 2310 Introduction to Digital Systems

Lab #1: Exploring Combinational Logic

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Section 1: Statement of the Learning Goal

The EE/CE 2310 lab exercise will reinforce retaining information from the classroom lectures on combinational logic and provide experience with common 7400 digital circuits. Additionally, we will be more familiarized with laboratory equipment, operation of fundamental logic gates, and design and construction of combinational logic circuits based on derived Boolean algebra expressions.

Section 2: Changes to the Procedure

There were no changes to the written lab procedure.

Section 3: Designing and Constructing Combinational Circuits Questions

1. **In the fourth EE 2310 class, you were given a circuit specification and told to develop a truth table, a corresponding Boolean expression, and the resulting circuit. Build that circuit design in this lab and verify that the output of the circuit matches the truth table.**

Truth table:

X	Y	Z	f
0	0	0	1
0	0	1	1
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	0

Karnaugh Map:

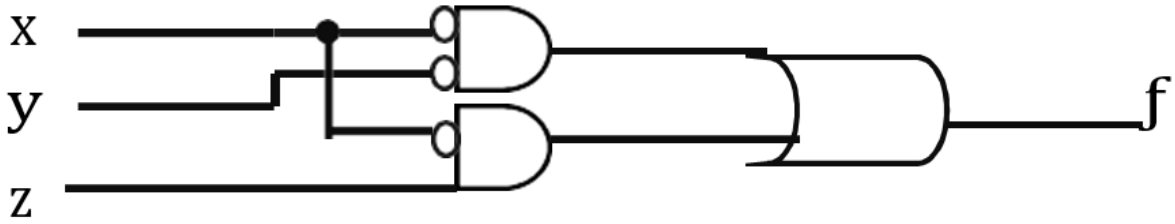
		YZ			
		00	01	11	10
X	0	**1**	**1**	**1**	
	1				

Boolean Expression:

$$f = \bar{x}\bar{y}\bar{z} + \bar{x}\bar{y}z + \bar{x}yz$$

$$f = \bar{x}\bar{y} + \bar{x}z$$

Diagram of Logic Circuit:



2. **The Boolean expression for a logic function is: $f = \bar{w}\bar{x}yz + \bar{w}\bar{x}y\bar{z} + \bar{w}xyz + \bar{w}xy\bar{z}$. Simplify this function and construct a digital circuit that corresponds to the simplified expression. Verify that the circuit obeys the Karnaugh map for the full expression.**

Truth Table:

W	X	Y	Z	f
0	0	0	0	
0	0	0	1	
0	0	1	0	1
0	0	1	1	1
0	1	0	0	
0	1	0	1	
0	1	1	0	1
0	1	1	1	1
1	0	0	0	
1	0	0	1	
1	0	1	0	
1	0	1	1	
1	1	0	0	
1	1	0	1	
1	1	1	0	
1	1	1	1	

Karnaugh Map:

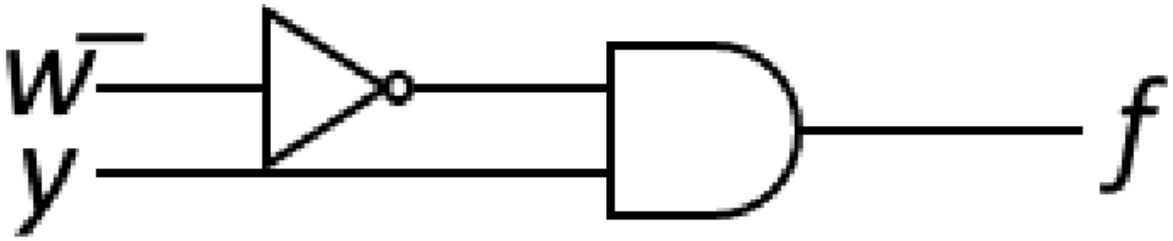
	YZ				
WX		00	01	11	10
	00			1	1
	01			1	1
	11				
	10				

Boolean Expression:

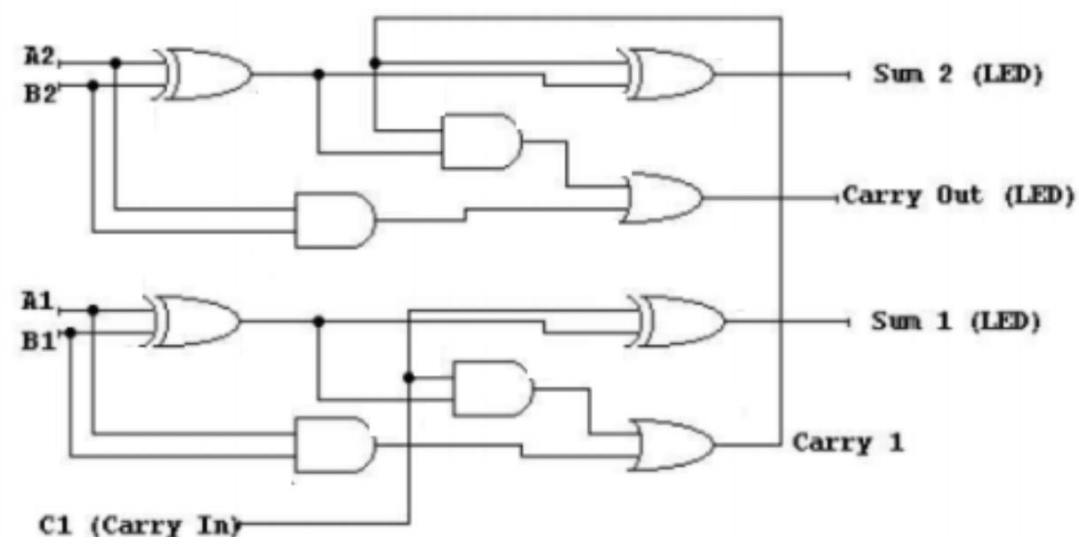
$$f = \bar{w}\bar{x}yz + \bar{w}\bar{x}y\bar{z} + \bar{w}xyz + \bar{w}xy\bar{z}$$

$$f = \bar{w}y$$

Diagram of Logic Circuit:



3. **Simple adder. Lecture 6 shows pictures of 1-bit half- and full adders. Consulting those diagrams, build a 2-bit positive number (no 2's compliment) adder, using only AND's, OR's, and XOR's. Prove that it works by adding: 1 + 0, 1 + 1, 1 + 10, 1 + 11, 10 + 10, 10 + 11, and 11 + 11. You will need the MSB carry-out connected to an LED to interpret the last three additions.**

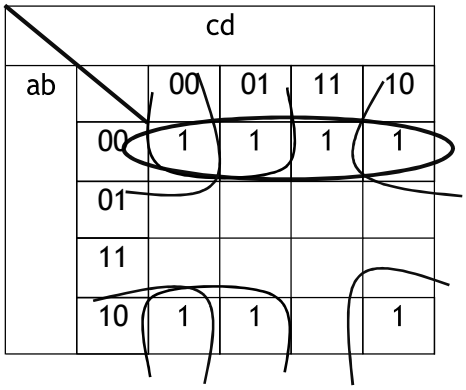


4. **A control system monitors four temperature sensors in a chemical process. Call them a, b, c, and d. When the temperature is too high, a sensor returns a logic 1. If the temperature is acceptable, it returns a 0. A function *f* is designed so that when it is a logic 1, heat is applied to the process. *f* should be logic 1 when variables a and b are simultaneously 0, when b and d are simultaneously 0, or when b and c are 0 at the same time. Derive a function for *f* for the conditions stated, simplify it, and build the circuit. Verify that the circuit satisfies the original conditions.**

Truth Table:

a	b	c	d	f
0	0	0	0	1
0	0	0	1	1
0	0	1	0	1
0	0	1	1	1
0	1	0	0	
0	1	0	1	
0	1	1	0	
0	1	1	1	
1	0	0	0	1
1	0	0	1	1
1	0	1	0	1
1	0	1	1	
1	1	0	0	
1	1	0	1	
1	1	1	0	
1	1	1	1	

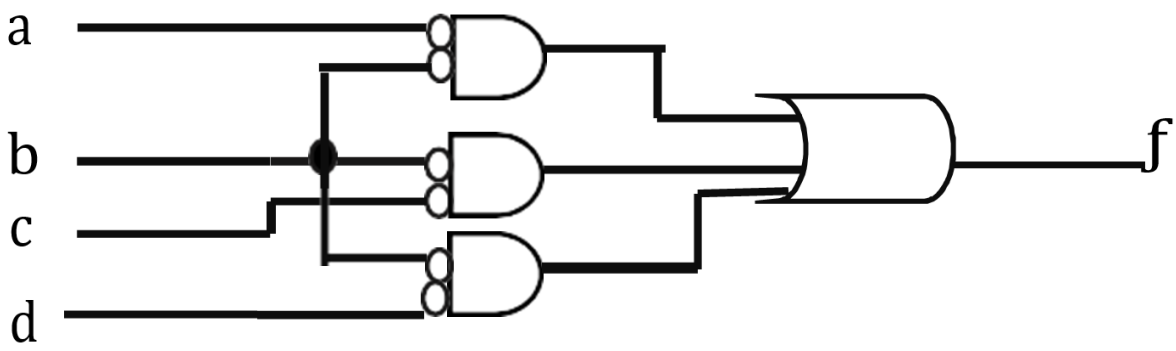
Karnaugh Map:



Boolean Expression:

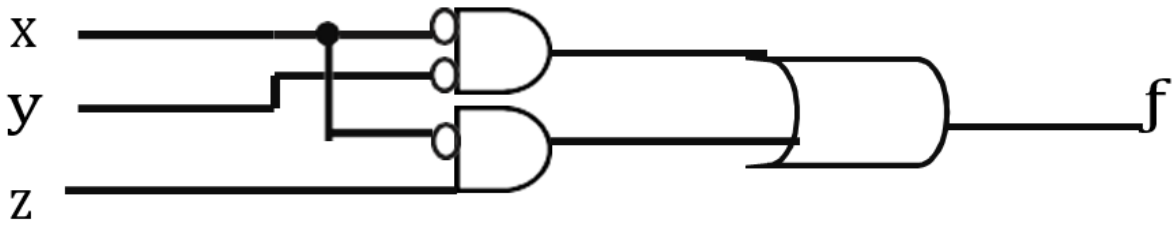
$$f = \bar{a}\bar{b} + \bar{b}\bar{c} + \bar{b}\bar{d}$$

Diagram of Logic Circuit:

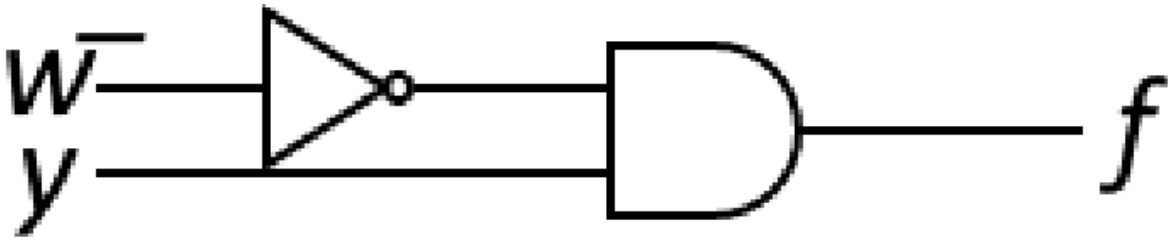


Section 4: Diagrams of Logic Circuits Assembled

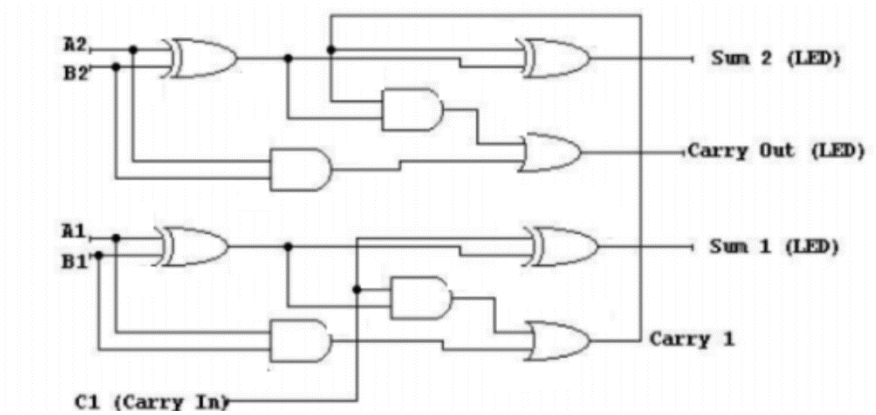
1.


x
y
z
f

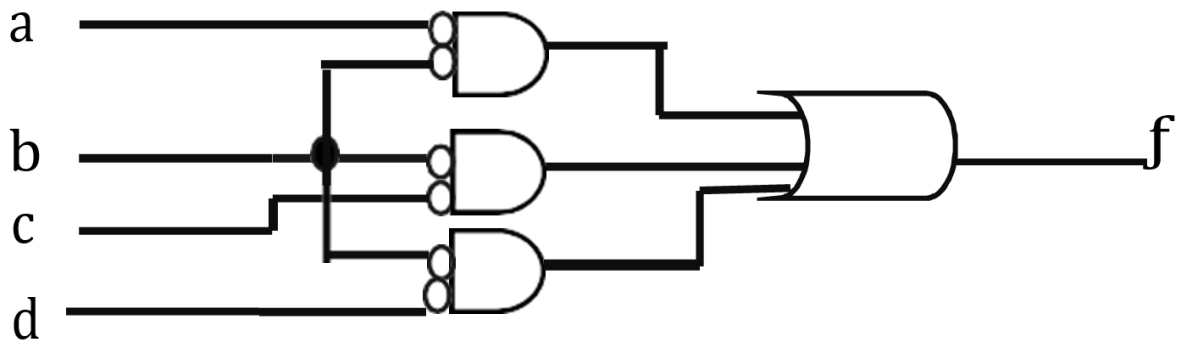
2.


w
y
f

3.


A2
B2
Sum 2 (LED)
Carry Out (LED)
A1
B1
Sum 1 (LED)
Carry 1
C1 (Carry In)

4.


a
b
c
d
f

Section 5: Statements of Results

1. For the first circuit design of the lab we had no issues with making the truth table, Karnaugh map, or simplifying the Boolean expression to create the logical circuit. After designing the circuit on paper, we constructed it on the protoboard by placing the chips vertically from each other and having matching wire colors for each input. The expected results matched the truth table and the circuit worked as the lab TA checked it.

X	Y	Z	f
0	0	0	1
0	0	1	1
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	0

2. The process of the first circuit design was incorporated into the second circuit design. We made the truth table, Karnaugh map, simplified the Boolean expression, and drew the circuit diagram first on paper before constructing the circuit on the protoboard. The expected results matched the work we did on paper and the lab TA checked us off for it. However, there was one issue through the entire process. One of the wires was connected to the wrong pin, which made the circuit not work according to our work in previous tests.

W	X	Y	Z	f
0	0	0	0	
0	0	0	1	
0	0	1	0	1
0	0	1	1	1
0	1	0	0	
0	1	0	1	
0	1	1	0	1
0	1	1	1	1
1	0	0	0	
1	0	0	1	
1	0	1	0	
1	0	1	1	
1	1	0	0	
1	1	0	1	
1	1	1	0	
1	1	1	1	

3. For the third circuit design, we encountered issues with drawing the adder to answer the problem on the lab questions first on paper. The TA helped us finish the diagram and fix our mistakes with connecting the wires when we made the adder on the protoboard. The adder worked according to our expected outcomes, but we encountered many issues in making it work.

4. For the last circuit design, we completed the design for the circuit on paper and went on to construct the real circuit on the protoboard. This circuit took a while since there were many wires involved; however, we color coded the wires to the complementary inputs to trace them back. There were a couple of mistakes in connecting the wires to the correct pins; but, the result met the expected condition, which was checked through our lab TA.

a	b	c	d	f
0	0	0	0	1
0	0	0	1	1
0	0	1	0	1
0	0	1	1	1
0	1	0	0	
0	1	0	1	
0	1	1	0	
0	1	1	1	
1	0	0	0	1
1	0	0	1	1
1	0	1	0	1
1	0	1	1	
1	1	0	0	
1	1	0	1	
1	1	1	0	
1	1	1	1	

Section 6: Discussion of Results

The circuit designs we were instructed to create in lab followed the same process of design. We had to first create a truth table, Karnaugh map, simplify the Boolean expression, and draw the logical circuit diagram on paper, and then create the circuit on the protoboard. If we did not follow this process, the outcome of the circuit will not match the correct results wanted. Through creating the circuit on the protoboard, we encountered a problem that occurred in 2 out of the 4 circuit problems. There was a lot of wiring necessary to connect the chips together; thus, the wires sometimes were not connected to the correct pins, allowing for error in our

design. Other than connecting some of the wires to the wrong pins, we had no other discrepancies and the results matched the expected outcomes. Both my partner and I learned that having one flaw in your design could corrupt your project's function.

Section 7: Summary and Conclusions

The lab exercise allowed us to apply conceptual knowledge learned in class to building a real circuit and seeing it light up the LEDs to check that they are correct. Not only did we apply conceptual knowledge, but we understood the necessity to have a process before creating the circuit. It is essential to make the truth tables, Karnaugh maps, simplify the Boolean expressions, and draw the circuit diagram on paper first before creating it on the protoboard. Moreover, through the lab process, we learned that there are various potential mistakes we can make it if we do not perform the lab carefully. For example, since we were not careful enough on 2 of the lab circuit problems, we connected a wire to a wrong pin, which led to the entire circuit not functioning correctly. Through this mistake we experienced the phenomena of combinational logic circuits, logic gates have an order to work, and without order logic gates would not work. Therefore, the lab exercise allowed us to familiarize ourselves with the lab equipment, apply our conceptual knowledge of circuits, and learn about common mistakes in creating circuits.