EE/CE 2310 Introduction to Digital Systems

Lab #2: Building a Sequential Logic Circuit

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Section 1: Statement of the Learning Goal

The EE/CE 2310 lab exercise will reinforce our knowledge in sequential logic circuits and components: flip-flops (FF's), binary counter, and storage register. After building the sequential logic circuit, we will be able to observe simple FF's in operation and be able to design a sequential circuit using multiple devices.

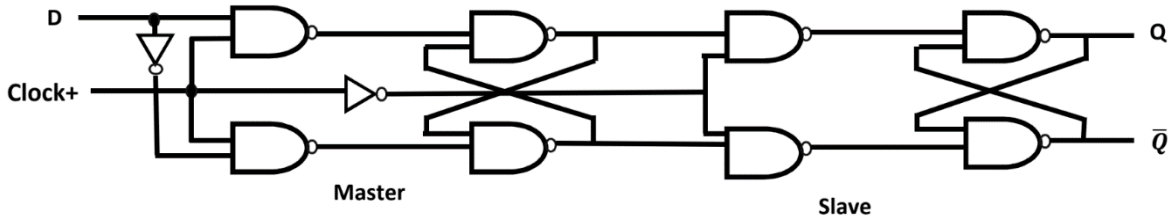
Section 2: Changes to the Procedure

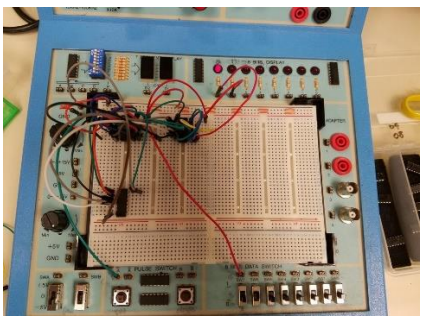
There were no changes to the written lab procedure.

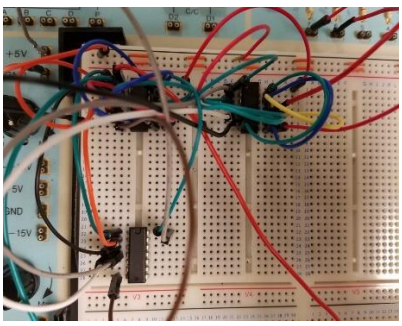
Section 3: Building a Sequential Logic Circuit Questions

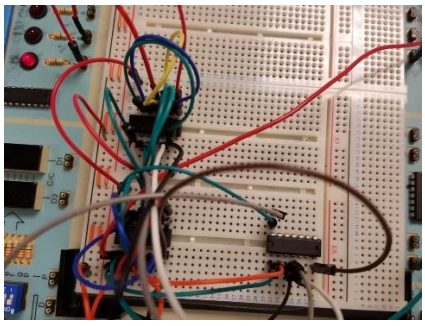
Design Problem 1

Design an inverter circuit using two 74195 quad latches (two parallel 4-bit registers). Four of the parallel slide switches input to the first register. When the clock (or "enable") ticks, data from the switches is stored in the first register. The data outputs of the register are inverted and that data is stored in the second 4-bit register.



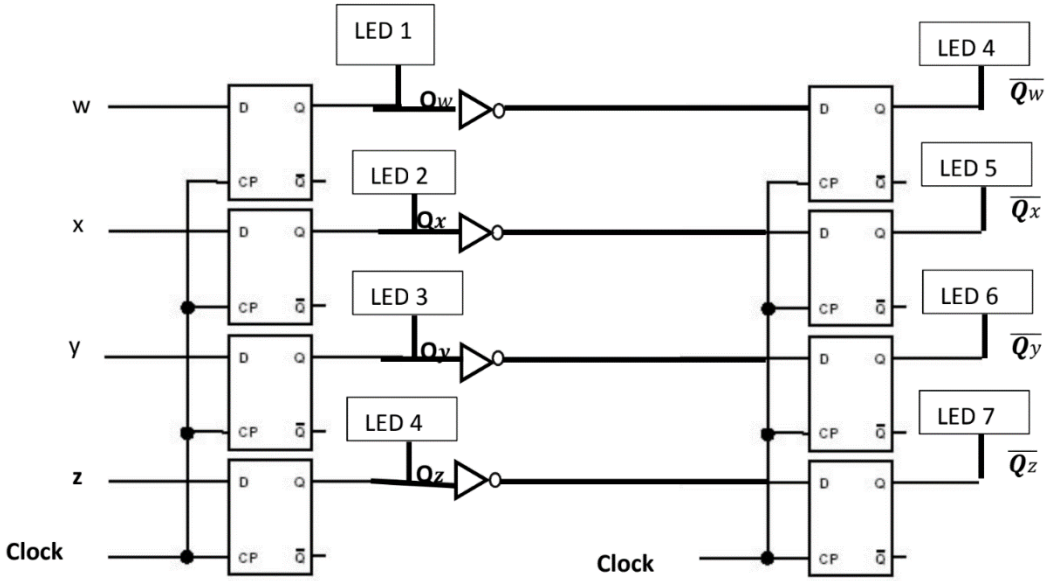






Design Problem 2

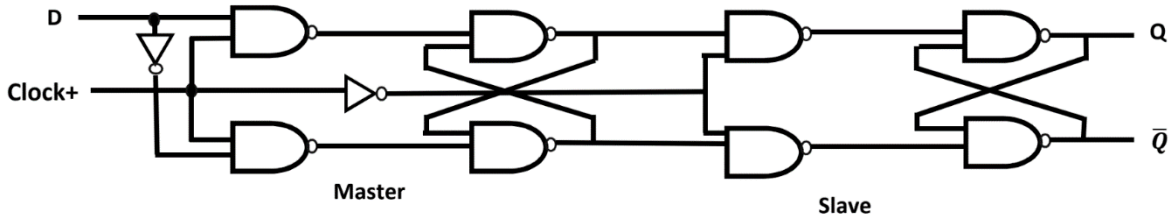
Use the eight LED's to display the output values of both registers. Clearly, the output of the second should be the inverted value of the first register. Use the two momentary or pulse switches as the clocks for the two registers.



Section 4: Diagrams of Logic Circuits Assembled

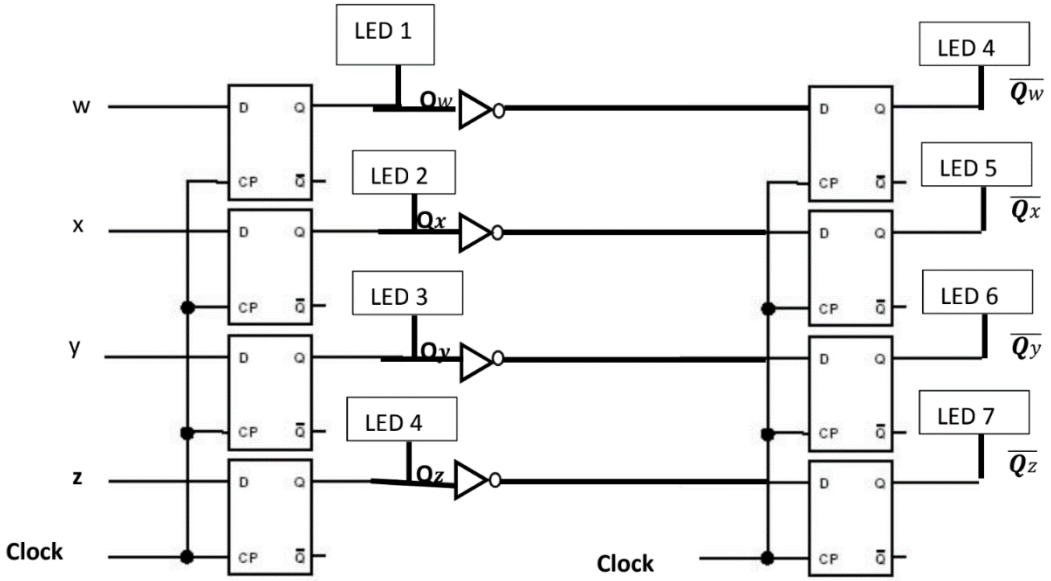
Design Problem 1

Master-Slave D FF



Design Problem 2

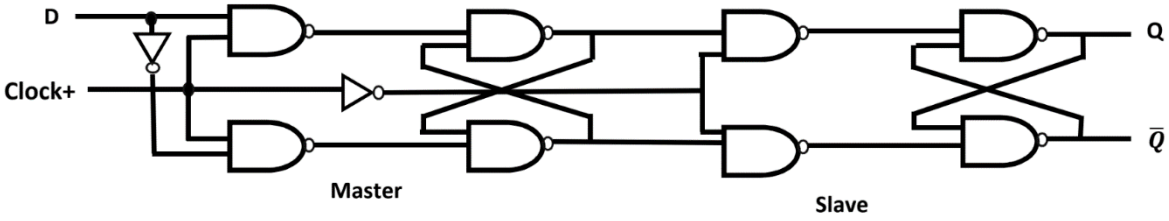
Inverter Circuit Using Two 74195 Quad Latches



Section 5: Statements of Results

Design Problem 1

Master-Slave D FF



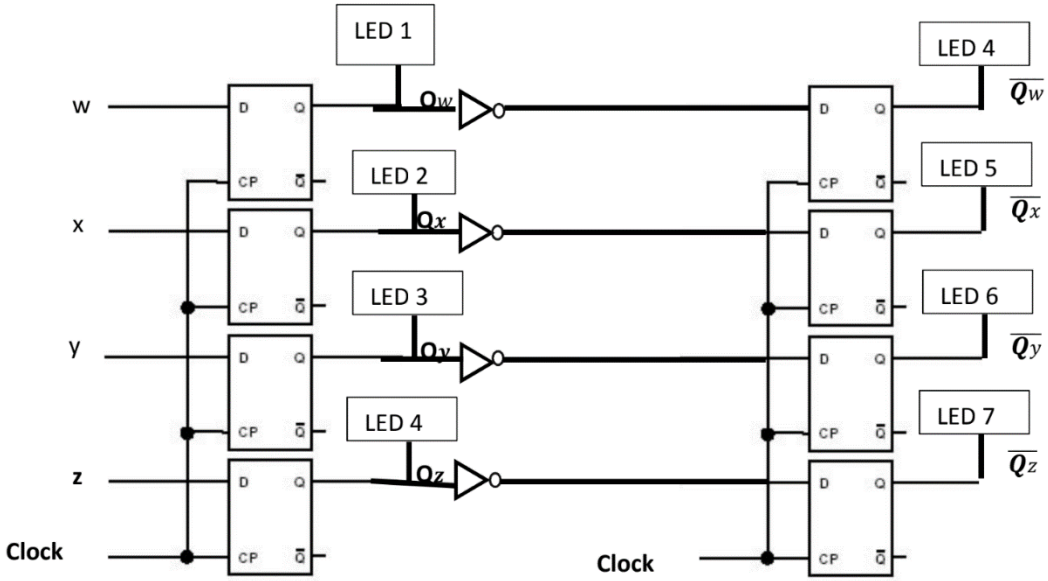
For the first design, we were tasked with creating a master-slave D FF with only 2 NAND gates, one inverter chip, pulse switch as the clock, and LED's connected to both master and slave outputs. Before creating the actual circuit on the protoboard, we designed a master-slave D FF on paper (Section 4) and listed the pins each wire with be connected to. Then we constructed the designed circuit on the protoboard by placing the chips vertically from each other; however, we did not match the wire colors for each input since there was an insufficient quantity of matching

color wires in the kit for this experiment. Additionally, another issue we encountered was placing the wires in the wrong pins. Since we were only using 2 NAND chips and an inverter, a lot of wiring was pinned to the first and second NAND chips and the inverter. Each NAND chip has 4 NAND gates and the inverter chip has 6 inverter gates. Despite these issues, we fixed our circuit and the output matched the expected result of the design problem as the lab TA checked it.

Design Problem 2

For the second design, we were tasked with designing an inverter circuit using two 74195 quad latches (two parallel 4-bit registers). We designed how we were going to make the circuit on paper first, before creating it on the protoboard. We set up the circuit the same way as design problem 1, by placing the chips vertically from each, except they are quad latches instead of NAND chips. Moreover, there was a different complication in this design problem. While wiring the registers to the inverter, clock, power, and ground, the registers were not connected from pin 9 to switch 0. Pin 9 is serial out on both shift registers, which delays data by one clock at a time for each stage. Without connecting both registers to switch 0 from pin 9, the clocks and output of the registers would not show properly. Despite this complication, we were able to complete the inverter circuit and the output matched the expected result of the design problem as the lab TA checked it.

Inverter Circuit Using Two 74195 Quad Latches



Section 6: Discussion of Results

The circuit designs we were instructed to create in lab followed the same process of design. We had to first design the sequential logic circuit on paper and then create the circuit on the protoboard. If we did not follow this process, the outcome of the circuit will not match the correct results wanted. Through creating the circuit on the protoboard, we encountered a problem that occurred in both design problems. There was a lot of wiring necessary to connect the chips together; thus, the wires sometimes were not connected to the correct pins, allowing for error in our design. Furthermore, design problem 2 had a different error than design problem 1, where we had to wire pin 9 of both registers to switch 0, which allowed the shifting of data each clock tick. Other than connecting some of the wires to the wrong pins, we had no other discrepancies and the results matched the expected outcomes. Both my partner and I learned that having one flaw in your design could corrupt your project's function.

Section 7: Summary and Conclusions

The lab exercise allowed us to apply conceptual knowledge about sequential logic circuits learned in class to build a real circuit and see it light up the LEDs to check that they are correct. Not only did we apply conceptual knowledge, but we understood the necessity to have a process

before creating the circuit. It is essential to draw the circuit diagram on paper first before creating it on the protoboard. Moreover, through the lab process, we learned that there are various potential mistakes we can make it if we do not perform the lab carefully. For example, since we were not careful enough on both design circuit problems, we connected a wire to a wrong pin, which led to the entire circuit not functioning correctly. Through this mistake we experienced the phenomena of sequential logic circuits, logic gates have an order to work, and without order logic gates would not work. Therefore, the lab exercise allowed us to familiarize ourselves with sequential logic circuits, apply our conceptual knowledge of circuits, and learn about common mistakes in creating sequential circuits.