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THE EQUIVALENT CIRCUIT OF A TRANSISTOR WITH A LIGHTLY DOPED COLLECTOR OPERATING IN SATURATION

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Abstract—This paper analyses the circuit behaviour of saturated transistors that have the base more heavily doped than the collector. The emphasis is on the small-signal response, although the switching characteristics can also be derived from the results. It is shown that, by making reasonable assumptions, the minority carrier density can be found throughout the collector region, and hence the total stored charge in the collector can be calculated. This leads to a small-signal equivalent circuit for the saturated transistor, the accuracy of which is compared with measurements. Finally the relevance of the results to the problem of making transistors with good forward AGC characteristics is discussed.

Résumé—Cet article analyse le comportement en circuit des transistors saturés dont la base est plus fortement dopée que le collecteur. On souligne surtout la réponse à petit signal cependant que les caractéristiques de commutation peuvent aussi être dérivées des résultats. On démontre qu'en faisant certaines hypothèses raisonables, la densité de porteur minoritaire peut être trouvée dans toute la région du collecteur et ainsi la charge totale emmagasinée dans celui-ci peut être calculée. Ceci mène à un circuit équivalent à petit signal pour le transistor saturé dont l'exactitude est déterminée par une comparaison aux mesures. Finalement, l'importance des résultats dans le problème de la fabrication des transistors ayant de bonnes caractéristiques AGC est discutée.

Zusammenfassung—Die Arbeit analysiert das Verhalten von Transistoren, deren Basis stärker dotiert ist als der Kollektor. Das Hauptgewicht der Erörterungen liegt auf dem Kleinsignalverhalten. Das hier entwickelte Ersatzschaltbild liefert allerdings auch das Schaltverhalten. Ausgehend von vernünftigen Annahmen wird gezeigt, dass die Minoritätsträgerdichte auf die ganze Kollektorzone verteilt ist. Die Berechnung der im Kollektor gespeicherten Ladung führt auf ain Ersatzschaltbild für das Kleinsignalverhalten des Transistors, dessen Brauchbarkeit durch Vergleich mit Messungen sichergestellt wird. Schliesslich wird diskutiert, ob sich das gewonnene Ersatzschaltbild zur Herstellung von Transistoren mit guter Vorwärtskennlinie heranziehen lässt.

NOTATION

A	area of emitter
$C_{b'c}$	capacitance appearing between the equivalent circuit points c' and b' as a result of saturation
f_T(base)	cut-off frequency due to charge stored in the base
f_T(collector)	cut-off frequency due to charge stored in the collector
i_n	electron current density in the collector
I_n	total electron current in the collector ($\simeq I_C$)
i_p, I_p	hole current density, hole current, in the collector
i_{ns}^*, I_{ns}^*	electron current density, and current, in the collector for $V_{c'b'} = 0$
i_{ns}, I_{ns}	electron current density, and current, in the collector at the onset of saturation—see equation (7a)
N_d	concentration of donor ions in the collector
$p(0)$	hole density in the collector at the edge of the collector depletion layer
$p(W)$	hole density in the collector region at the collector contact
p, n	hole and electron concentrations

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p_0	equilibrium hole density in the collector
q_c	total minority carrier charge per unit area stored in the collector
q_b	total minority carrier charge per unit area stored in the base
Q_c	total minority carrier charge stored in the collector
$r_{b'c}$	resistance appearing between the equivalent circuit points c' and b' as a result of saturation
$r_{cc'}$	collector series resistance
$r_{cc'0}$	collector series resistance prior to saturation
τ_p	lifetime of holes in the collector
u	$eV_{cc'}/kT$
$V_{c'b}$	potential drop across the collector base junction
V_{cb}	potential drop between the external collector contact and the internal base point b'
W	effective width of collector region

1. INTRODUCTION

THE CIRCUIT behaviour of saturated transistors is frequently of interest, particularly in switching circuits and RF amplifiers where AGC is obtained by saturating the transistor (forward AGC). EBERS and MOLL[1] have given a theory and equations for the performance of saturated devices in which the collector region is much more heavily doped than the base. This paper is intended to provide theory and equations for the performance of saturated transistors in which the collector region is wide and much less heavily doped than the base, many transistors made today being of this type.

In order to develop a theory for transistors of this type it is necessary to make approximations, the most crucial being about the heating of carriers. This paper deals with the case where hot electron effects in the collector region may be neglected. This is in contrast to the situation considered by VAN DER ZIEL and AGOURDIS[2] who implicitly assumed a narrow collector region so that the carriers are so hot that they attain the limiting drift velocity.

KIRK[3] has considered the same case as the one treated here, but he does not establish a precise model. He shows that in saturation a boundary layer associated with the collector–base junction migrates towards the collector contact and that the potential on the base side of the boundary is close to the base potential. From this he supposes that the boundary represents the collector edge of the effective base region and that the transistor simply behaves as though the base width had been correspondingly increased. This supposition is incorrect. Even in saturation there is still a collector space-charge layer at the collector base junction, as with any forward biased junction. Although the voltage drop across this layer is small, its effect on carrier concentrations is generally very large, owing to their exponential dependence on voltage.

In this paper the presence of the space-charge layer is not neglected. It is shown that the assumption that the base is much more heavily doped than the collector means that the carrier distribution in the base is unaffected by saturation, so that the characteristics of the saturated transistor can be found from considering the conditions in the collector region only. Only the quasi-neutral collector region is considered because the collector space-charge layer is very thin under forward bias, and charge storage in it can generally be neglected.

The method of analysis is to derive expressions for the variation of minority carrier density with distance through the collector, from which a value for the total stored charge in the collector is derived. By considering the change in carrier density with the voltages and currents applied to the device, a small signal equivalent circuit is built up in much the same way as the equivalent circuit for a normal transistor is found from the voltage and current variations of carrier density in the base. The pulse response could be found in a similar way, but this is not discussed in detail here.

The predictions of the small signal response of the transistor arising from this equivalent circuit are tested by comparing the measured and calculated values of the current dependence of f_T and the admittances of the transistor. Finally there is a brief discussion of the application of the theory and formulae to the design of transistors with good forward AGC characteristics.

2. PHYSICAL MODEL OF THE SATURATED TRANSISTOR

Many of the assumptions made in this paper were outlined in the introduction, but they will now be discussed in detail, with reference to an *npn* transistor.

(*a*) The base is much more heavily doped than

the collector region, which is assumed homogeneous with a donor concentration (N_d).

(b) The collector region is wide enough for the whole collector–base voltage (V_{cb}) to be dropped across it without producing significant heating of the electrons. The electron mobility in silicon is not markedly affected up to fields of 2000 V/cm[4] so that this assumption implies that the collector region has an effective width W (in μ) $> 5V_{cb}$. [It should be noted that the model considered by VAN DER ZIEL and AGOURDIS[2] requires the converse condition which is approximately that W (in μ) $< V_{cb}$. For values of W between these limits it would be necessary to use numerical computation.]

(c) Owing to assumption (b), saturation occurs as a result of the collector–base junction becoming forward biased. The voltage across the junction is then small enough for carrier heating in the space-charge layer to be negligible so the carrier densities on either side of the space charge layer are related by the normal Boltzmann equation. Owing to assumption (1) the hole density on the collector side of the layer $p(0)$ is much greater than the electron density on the base side, which is practically unaffected by saturation. Thus

$$p(0) = p_0 \exp(eV_{c'b'}/kT) \qquad (1)$$

where p_0 is a constant, and the transit time of electrons across the base is largely unaffected by saturation. So the characteristics of the saturated transistor are determined by the carriers in the collector region.

(d) Almost complete charge neutrality exists in the collector region, i.e. $n = p+N_d+\epsilon$ where $\epsilon/N_d \ll 1$.

(e) The steady state hole current, I_p, in the collector is negligible. This implies that the hole lifetime τ_p is sufficiently large, and that no holes enter the collector from the n^+ contact. Thus the hole distribution in the collector is related to the voltage by the Boltzmann equation. In practice it is only necessary that the hole current be negligible compared with the electron current, and a figure of τ_p greater than about 50 nsec is sufficient for an average high frequency transistor.

(f) The geometry is one-dimensional. It is natural to make this assumption in order to simplify the analysis, but in view of the assumption that the collector region is thick [assumption (b)] it is necessary to consider the degree of approximation involved. In many transistors the emitter is small and there is pronounced lateral spreading of the current in the collector, so that one might expect a one-dimensional analysis to be seriously in error.

The error may be assessed by considering two other elementary current flow patterns, cylindrical and spherical, as in Appendix 1. It is found that for currents not greatly in excess of the saturation current (I_{ns}) the region of stored charge in the collector is thin compared with the lateral dimensions of the emitter so that current flow in this region is essentially one-dimensional. The remainder of the collector acts simply as a series resistance so that its geometry is immaterial. All that is necessary to convert the cylindrical and spherical cases to one-dimension is to define an effective value of collector width W, which is to a first approximation independent of current. However, the high current density in the collector near the base makes it more difficult to satisfy assumption (b) that there is no carrier heating.

The current flow in the collector of an actual transistor is generally a combination of the cases considered and may be assumed one dimensional in the current range of practical interest (near the onset of saturation). However the reduced symmetry results in a small variation of potential over the junction and the theory presented here will not be obeyed exactly.

3. DISTRIBUTION OF MINORITY CARRIERS IN THE COLLECTOR REGION

The starting point for the calculation of the hole distribution in the collector is the normal pair of equations for the hole and electron current density when both diffusion and drift of carriers takes place.

$$i_n = eD_n\left(\frac{\partial n}{\partial x}\right) + e\mu_n En \qquad (2)$$

$$i_p = -eD_p\left(\frac{\partial p}{\partial x}\right) + e\mu_p Ep \qquad (3)$$

putting $n = p+N_d$, and $i_p = 0$ [assumptions (d) and (e)] gives

$$i_n = -2eD_n(1+N_d/2p)\partial p/\partial x \qquad (4)$$

and hence, by integration

$$x = \frac{-2eD_n}{i_n}\left[p - p(0) + \frac{N_d}{2}\ln\left(\frac{p}{p(0)}\right)\right] \quad (5)$$

Equation (5) gives the relation between p and x in terms of the collector current density i_n and the hole concentration at the collector edge of the collector. It remains to find $p(0)$ in terms of the applied currents and voltages. This can be done by using assumption (e) that $i_p \to 0$ which allows p to be related to voltage by the Boltzmann equation. Mathematically it is convenient to let $x = W$ in equation (5) (where W is the effective width of the collector region, see Appendix 1), since the voltage is known directly at that point ($= V_c$). However the same results can be obtained by choosing any value of x for which $p \to 0$. Thus from equation (3)

$$V_{cb'} - V_{c'b'} = -\int_0^W E\,dx = \frac{-kT}{e}\int_0^W dp/p$$

$$= \frac{-kT}{e}\ln\left(\frac{p(W)}{p(0)}\right).$$

So from equation (5), assuming $p(W) \to 0$

$$W = \frac{eD_n}{i_n}\left[\frac{2p(0)}{N_d} + \frac{e(V_{cb'} - V_{c'b'})}{kT}\right]. \quad (6)$$

It is now convenient to introduce the saturation current (the current for $V_{c'b'} = 0$) as a parameter (I_{ns}^*)

$$I_{ns}^* = e\mu_n N_d V_{cb'}/W.$$

Thus from equation (6)

$$\frac{p(0)}{N_d} = \frac{e}{2kT}[V_{cb'}(I_n/I_{ns}^* - 1) + V_{c'b'}]. \quad (7)$$

Normally the hole current to the base is very small so

$$I_E \simeq I_C = I_n.$$

Equation (1) can be used to substitute for $V_{c'b'}$ to obtain a non-explicit equation for $p(0)/N_d$ in terms of measurable quantities. However, in saturation, $V_{c'b'}$ may be taken as just less than the diffusion voltage, e.g. $-0{\cdot}6$ V for a typical silicon transistor. This leads to a simplified form of equation (7) which is useful well in saturation

$$\frac{p(0)}{N_d} = \frac{u}{2}\left(\frac{I_n}{I_{ns}} - 1\right) \quad (7a)$$

where

$$u = e(V_{cb'} - V_{c'b'})/kT$$

and

$$I_{ns} = I_{ns}^*/(V_{cb'} - V_{c'b'})/V_{cb'}.$$

Equations (5) and (7) can be used to find the hole distribution as a function of distance in the collector, the results in two particular cases being shown in Fig. 1. It is seen that the hole charge in the collector is concentrated near the collector–base junction and can be so large that the resistivity of the collector is heavily modulated in this region.

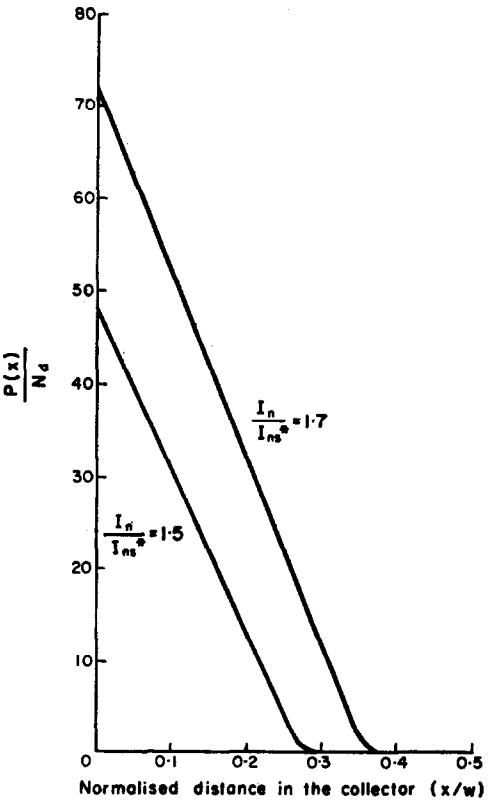

FIG. 1. Hole distribution in the collector of a saturated one-dimensional ~~n–p–n~~ transistor for $I_n/I_{ns}^* = 1{\cdot}5$, $I_n/I_{ns}^* = 1{\cdot}7$, $V_{cb'} = 6$ V, $V_{c'b'} = -0{\cdot}6$ V, $kT/e = 25$ mV.

The charge is kept close to the collector junction by the field produced by the electron current flowing through the collector. The charge spreads across the region as the electron current increases.

4. TOTAL MINORITY CARRIER CHARGE STORED IN THE COLLECTOR

The total charge stored in the collector is clearly a quantity of importance in the circuit behaviour of the saturated transistor as this charge has to be supplied to the terminals of the transistor by the circuit.

The charge can be simply found by multiplying equation (4) through by $p\mathrm{d}x$ and integrating; one obtains then the charge per unit area q_c

$$q_c = \frac{e^2 D_n}{i_n}[p(0)^2 + N_d \cdot p(0)], \tag{8}$$

and the total charge (Q_c)

$$Q_c = \frac{e^2 \cdot D_n \cdot A^2}{I_n}[p(0)^2 + N_d \cdot p(0)]$$

where A is the emitter area.

This equation, in conjunction with equation (7a), gives the charge stored as a function of current and voltage. Well into saturation, when $p(0) \gg N_d$, we find

$$Q_c = \frac{I_n W^2}{4D_n}\left[1 - \frac{I_{ns}}{I_n}\right]^2. \tag{9}$$

Equation (9) can be used to determine the performance of switching transistors in saturating circuits. However, our main concern here is with the explanation of the mechanism of forward AGC, and this is a small-signal effect and requires a more detailed examination of small-signal behaviour.

5. SMALL SIGNAL EQUIVALENT CIRCUIT

Owing to the assumptions made in Section 2, only the collector region is affected by saturation, so only the collector part of the equivalent circuit is altered. It is shown in this section that the collector circuit is changed in the following ways.

(*i*) By the addition of an extra conductance and capacitance in parallel with the collector depletion capacitance.

(*ii*) By a reduction of the collector series resistance.

(*iii*) By a modification of the collector current generator.

(*iv*) By the appearance of a new element, a voltage generator in series with the collector series resistance.

These elements are found, together with expressions for their values, by a method which has been used to build up the emitter–base equivalent circuit of an unsaturated device. This method is the quasi-steady-state approach[5] and finds the elements by considering the changes in applied voltages and currents. The frequency limitation on the circuit is that the input signal does not change appreciably within the relaxation time of the charge pattern. In practice this usually means that the circuit holds up to frequencies of about $f_{T/2}$, where f_T is the cut-off frequency of the saturated transistor.

(*a*) *Additional admittance across the collector–base junction*

The first element that will be considered is the extra collector capacitance. This comes about in exactly the same way as the emitter diffusion capacitance; the voltage $V_{b'c'}$ across the collector junction alters $p(0)$ and this in turn alters the total stored charge.

$$\therefore C_{b'c'} = \left[\frac{\partial Q_c}{\partial V_{c'b'}}\right]_{I_s} = \left[\frac{\partial Q_c}{\partial p(0)}\right]_{I_s} \cdot \left[\frac{\partial p(0)}{\partial V_{c'b'}}\right]$$

so from equations (8) and (1)

$$C_{b'c'} = \frac{W^2}{uD_n} \cdot \left[\frac{p(0)}{N_d} \cdot \frac{I_{ns}}{I_n}\right] \frac{1 + 2p(0)/N_d}{r_{cc'0}} \tag{10}$$

where $r_{cc'0}$ is the collector series resistance prior to saturation and is given by

$$r_{cc'0} = \frac{V_{cc'}}{I_n} = \frac{W}{q \cdot \mu_n \cdot N_d \cdot A}.$$

By inserting equation (7a) for $p(0)/N_d$ in equation (10), an explicit equation is found for $C_{b'c'}$ in terms of measurable quantities.

The leakage current associated with the capacitance is small because the hole current I_p is given by Q_c/τ_p and τ_p is supposed large. The

small signal a.c. resistance produced by this current is $r_{b'c'}$ which equals $C_{b'c'}/\tau_p$. If $p(0)/N_d \gg 1$ then from equations (1) and (8)

$$r_{b'c'} = kT/2eI_p. \tag{11}$$

(b) Reduction in collector series resistance

The next element of the equivalent circuit is the collector series resistance $r_{cc'}$ given by

$$r_{cc'} = \left[\frac{\partial V_{cc'}}{\partial I_c}\right]_{V_{eb'}} = -\left[\frac{\partial V_{c'b'}}{\partial I_n}\right]_{V_{eb'}}$$

$$= -\left[\frac{\partial V_{c'b'}}{\partial p(0)}\right] \cdot \left[\frac{\partial p(0)}{\partial I_n}\right]_{V_{eb'}}.$$

So from equations (1) and (7) [after writing $V_{c'b'} = (kT/e)\ln[p(0)/p_0]$ in equation (7)].

$$r_{cc'} = \frac{r_{cc'0}}{1+\dfrac{2p(0)}{N_d}} \tag{12}$$

which, in conjunction with equation (7a) gives an explicit expression for $r_{cc'}$. As might be expected from the physical picture given earlier, the resistance decreases as a result of saturation.

From equations (10) and (12) the collector time constant (t_c) is

$$t_c = r_{cc'}C_{b'c'} = \frac{W^2}{uD_n} \cdot \frac{p(0)}{N_d} \cdot \frac{I_{ns}}{I_n}. \tag{13}$$

(c) Change in the collector current generator

The change in the normal collector current generator as a result of saturation can be found by calculating the new value of the cut-off frequency f_T. This is not the most direct way of finding the alteration in the generator, but f_T is a very important parameter for estimating the behaviour of a transistor under forward gain control and it is useful to go into the calculation of f_T in more detail.

The f_T of an unsaturated device is given by

$$\frac{1}{2\pi f_T(\text{base})} = \frac{dq_b}{di_n},$$

supposing the collector depletion capacitance and transit time to be zero.

The f_T of the saturated device is given by

$$\frac{1}{2\pi f_T} = \frac{dq_b}{di_n} + \frac{dq_c}{di_n}$$

$$= \frac{1}{2\pi f_T(\text{base})} + \frac{1}{2\pi f_T(\text{collector})}.$$

From equation (8)

$$\frac{dq_c}{di_n} = \frac{e^2D_n}{i_n} \cdot \frac{d}{di_n}[p(0)^2 + N_d \cdot p(0)]$$

$$+ e^2D_n \cdot \frac{d}{di_n}\left(\frac{1}{i_n}\right)[p(0)^2 + N_d p(0)].$$

So, using the value for $[\partial p(0)/\partial I_n]_{V_{eb'}}$ found from equation (7) in the derivation of equation (12)

$$\frac{1}{2\pi f_T(\text{collector})} = \frac{W^2}{u \cdot D_n}\left[\frac{p(0)}{N_d} \cdot \frac{I_{ns}}{I_n}\right]$$

$$\times \left[1 - \frac{1}{u}\frac{p(0)}{N_d} \cdot \frac{I_{ns}}{I_n}\left(1 + \frac{N_d}{p(0)}\right)\right].$$

From equation (13), it is seen that the first term is the collector time constanf t_c, so

$$\frac{1}{2\pi f_T} = \frac{1}{2\pi f_T(\text{base})} + t_c - \frac{W^2}{D_n}$$

$$\times \left(\frac{1}{U} \cdot \frac{p(0)}{N_d} \cdot \frac{I_{ns}}{I_n}\right)^2 \frac{1+N_d}{p(0)}. \tag{14}$$

The first two terms represent the usual formula for f_T when collector resistance and capacitance are present—the third term is therefore due to a change in the current generator. Putting

$$t_g = -\frac{W^2}{D_n} \cdot \left(\frac{1}{U} \cdot \frac{p(0)}{N_d} \cdot \frac{I_{ns}}{I_n}\right)^2 \cdot \left(1 + \frac{N_d}{p(0)}\right)$$

it can be shown that the generator has the value,

$$g_e\left(1 - \frac{j\omega t_g}{1+j\omega t_c}\right) \cdot V_{b'e} \tag{15}$$

where $g_e = eI_n/kT$.

It is of interest to compare the values of t_c and t_g.

From equations (13) and (7a)

$$t_c = \frac{W^2}{2D_n}\left(1 - \frac{I_{ns}}{I_n}\right). \tag{16}$$

If $p(0) \gg N_d$, which is the range where t_s is significant

$$t_s \simeq -\frac{W^2}{4D_n}\left(1-\frac{I_{ns}}{I_n}\right)^2 \qquad (17)$$

$$\therefore \quad t_c+t_s \simeq \frac{W^2}{4D_n}\left[1-\left(\frac{I_{ns}}{I_n}\right)^2\right]. \qquad (18)$$

Equation (18) may also be derived directly from equation (9) by differentiation. From equations (18) and (14) we have

$$\frac{1}{2\pi f_T} = \frac{1}{2\pi f_T(\text{base})} + \frac{W^2}{4D_n}\left[1-\left(\frac{I_{ns}}{I_n}\right)^2\right]. \qquad (19)$$

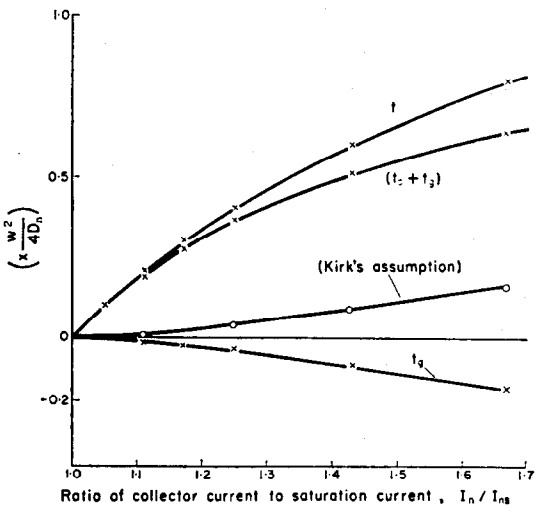

FIG. 2. The variation of $t_c(=r_{cc'}C_{b'c'})$, t_s and t_c+t_s (the total extra transit time due to saturation) with I_n/I_{ns}.

Equations (16)–(18) are plotted in Fig. 2, from which it is seen that the effect of t_s is small until saturation is well advanced. Thus the lowering of the f_T is largely due to t_c, the $r_{cc'}C_{b'c}$ product.

(d) Voltage generator in series with collector contact

There now remains an additional circuit element which does not appear in the usual equivalent circuit of a transistor, and this is a voltage generator $\mu_B \cdot V_{b'c}$, in series with the collector series resistance. If this voltage generator were not present any voltage applied between the c and b' terminals would largly appear across the collector–base junction. In fact this voltage is absorbed mainly in the collector resistance as a result of feedback effect caused by a change in the width of the heavily modulated region. Suppose for example that the voltage is increased between collector and base, then the collector junction becomes less forward biased and so $p(0)$ falls and hence the width of the stored charge region decreases. The width of the unmodulated region then increases and so the potential drop across this region also increases and opposes the initial voltage increase. This effect is represented in the equivalent circuit by the voltage generator.

It can be seen that the value of the voltage generator is given by the relation

$$\mu_B = \left[\frac{\partial V_{cc'}}{\partial V_{cb'}}\right]_{I_n} = 1\Big/\left(1+\left[\frac{\partial V_{c'b'}}{\partial V_{cc'}}\right]_{I_n}\right)$$

$$\therefore \quad \mu_B = 1\Big/\left(1+\left[\frac{\partial V_{c'b'}}{\partial p(0)}\right]_{I_n}\cdot\left[\frac{\partial p(0)}{\partial V_{cc'}}\right]_{I_n}\right)$$

$\therefore$ from equations (1) and (7)

$$\mu_B = \frac{1}{1+\dfrac{N_d}{2p(0)}}. \qquad (20)$$

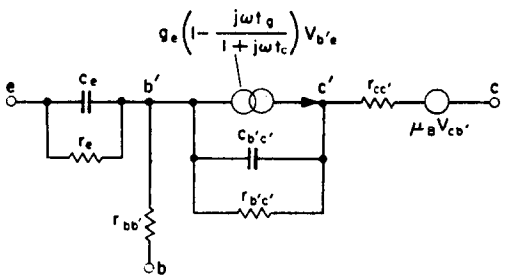

FIG. 3. Equivalent circuit of a saturated transistor with a lightly doped collector (a practical transistor will have, in addition, parasitic elements such as capacitance between the terminals).

This completes the small signal equivalent circuit of this model of a bottomed transistor, the diagram being shown in Fig. 3. The values of the elements are given by equations (10), (11), (12), (14) and (15) in conjunction with equation (7a).

6. MEASUREMENTS AND DISCUSSION

In order to check the model and equivalent circuit that has been described it was decided to

compare the measured and calculated values of the output admittances as a function of current, and those of the variation of f_T with current.

The first problem was to choose the transistors for this comparison. It is observed that although the theory predicts a sharp fall in f_T with current after bottoming (see Fig. 4) many transistors show

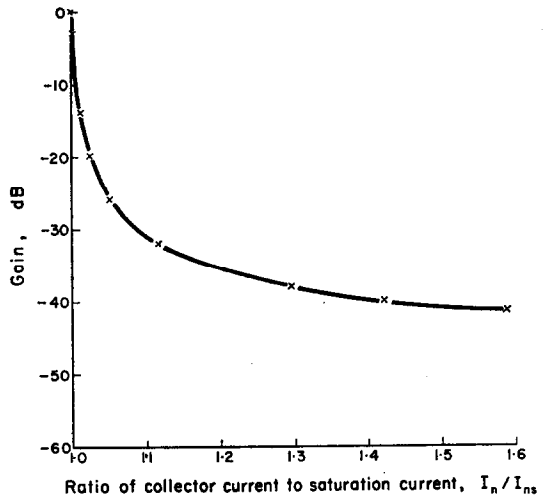

FIG. 4. Ratio of f_T/f_T(base) for a silicon n–p–n transistor as a function of I_n/I_{ns}, from equation (19) assuming $W = 20\ \mu$ and f_T(base) = 1000 Mc/s.

a very gradual fall in f_T. However, this is not surprising because, as discussed in Section 7, there are a great many reasons why practical transistors can depart from the idealized behaviour described by the theoretical model, and all of these tend to smooth out the f_T vs. current curve. So it is clear that the theory should be checked on transistors showing a sharp fall in f_T. Three such devices, n–p–n diffused based germanium transistors, were therefore selected for this comparison of theory with experiment. Their f_T vs. current characteristics are shown in Fig. 5.

The first check was that the form of the measured f_T vs. current agreed with theory. From equation (19) it is seen that a linear dependence of $1/f_T$ on $1/I_n^2$ is predicted and the results of plotting $1/f_T$ vs. $1/I_n^2$ on these devices are shown in Fig. 6. It is seen that reasonably good straight lines are obtained, in accord with theory. It is of interest to compare these results with those postu-

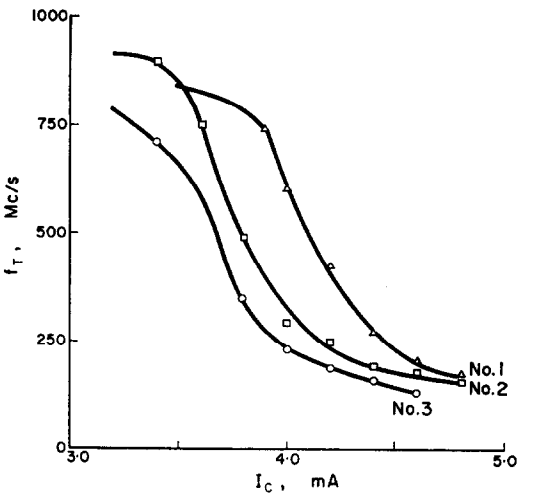

FIG. 5. Measured f_T vs. I_c for three n–p–n germanium transistors.

lated by KIRK.[3] As may be seen from Fig. 1 there is a region of the collector in which the electron distribution resembles that in the base of a transistor, as Kirk supposed. From equation (4) it may be seen that in the region where $2p \gg N_d$ the electron current may be treated as a diffusion current. When the width of this region is much greater than that of the base the error made by Kirk in adding the two widths together to find an effective base width is unimportant, so that one might expect his simple expression for f_T to be approximately correct. However, it is not. The changes in charge with current are unlike those in the base of a transistor, an increase in current

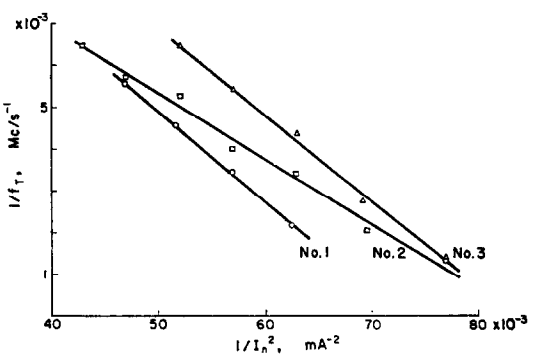

FIG. 6. $1/f_T$ vs. $1/I_n^2$ for three n–p–n germanium transistors.

producing an increase in the width of the 'base' as well as an increase in charge density (see Fig. 1). The increase in charge is therefore much greater than Kirk's simple expression indicates, and the f_T is much lower. This is shown in Fig. 2.

It was shown in Section 5 that the f_T reduction is mainly due to a feedback effect caused by a combination of the collector series resistance and the admittance which appears across the collector–base junction when the transistor is saturated. In order to check this theory, it would be best to compare the measured and calculated values of the collector admittance as well as those of the collector resistance. Unfortunately it was not possible to do this directly with the apparatus available, so it was decided to make two sets of measurements which would provide some comparison of the predicted and measured values of the collector impedance. The first of these measurements was that of h_{0b} at 1592 c/s, and the second was that of y_{0b} at 3 Mc/s (the currents through the devices being such that the transistors were definitely saturated). The measurement of h_{0b} gives $r_{b'c'}$ the real part of the collector admittance, and y_{0b} involves, in addition, the capacitive part of the admittance. Both measurements are affected by the voltage generator $\mu_b V_{cb}$ and the calculation of y_{0b} also involves knowing $r_{bb'}$ and r_e and τ_p.

Table 1

I_e, mA	h_{0b}(meas), μmho	h_{0b}(calc), μmho	y_{0b}(meas), μmho	y_{0b}(calc), μmho
Tr No. 1 (23/29)				
4·5	8·0	13·3	$38+j\ 70$	$116+j115$
5·0	9·3	17·8	$100+j113$	$163+j154$
5·5	12·0	20·1	$111+j141$	$195+j179$
6·0	17·0	24·9	$118+j188$	$226+j197$
Tr No. 2 (3)				
4·0	2·85	8·6	$40+j\ 62$	$82+j\ 84$
4·5	5·96	10·6	$109+j107$	$111+j110$
5·0	8·57	13·6	$164+j149$	$153+j144$
5·5	12·0	16·1	$213+j188$	$190+j173$
6·0	15·5	19·6	$260+j234$	$243+j209$
Tr No. 3 (4)				
4·5	15·6	17·2	$j230$	$j151$
5·0	22·4	26·0	$j336$	$j240$
5·5	30·3	32·1	$j410$	$j259$
6·0	39·5	38·2	$j485$	$j312$

The results are shown in Table 1 and the details of the calculations are given in Appendix 2. It may be seen that the measured and calculated values agree almost everywhere within a factor of two. In view of the uncertainties in the additional parameters that are brought into some of the calculations a factor of two agreement may be regarded as satisfactory.

7. APPLICATIONS TO THE DESIGN OF TRANSISTORS WITH GOOD AGC CHARACTERISTICS

A 'good' forward AGC characteristic for a transistor is one in which the gain decreases smoothly with increasing current (practically, a uniform decrease of about 10 dB for each 30 per cent increase in current is desirable). There are several reasons for this, the most important being that experimentally and theoretically[6] there is a relation between good cross modulation performance in the gain control region and the smoothness of the gain control curve. The calculations in this paper cannot in general provide explicit expressions for the gain because the frequency of operation is often much higher than the f_T, so that the equivalent circuit is no longer correct. However, from work on both unsaturated and saturated transistors it is found that f_T gives a good indication of the gain above f_T, and we can use the calculated f_T to predict the approximate gain control curve.

From equation (19) it is clear that the variation of f_T for a given fractional change in current can be made small by making W small. Thus devices with a thin high resistivity collector region should give a reasonably smooth AGC characteristic, although the maximum value of $1/f_T$ (collector) would be small. This result can also be deduced from a physical picture of the charge pattern calculated for the collector region. The stored minority carrier charge heavily modulates the collector region so that the voltage drop between collector and base is almost entirely due to the collector current flowing across the unmodulated part of the collector region. If the collector region is thin then an increase in collector current requires only a small decrease in the width of the unmodulated region to keep the collector–base voltage constant,

and so the width of the modulated part changes only slightly and hence the stored charge and f_T only change slightly. This leads to a more promising method of obtaining a smooth gain control characteristic.

Suppose the resistivity of the collector region is graded in the way shown in Fig. 7, so that there is

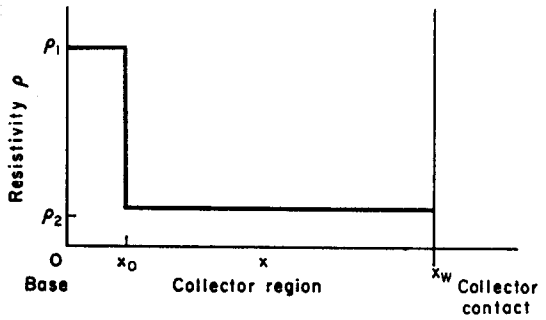

FIG. 7. Resistivity vs. distance in the collector of a hypothetical transistor.

a thin high resistivity region near the collector–base junction. At the onset of saturation when charge is stored in the collector very close to the collector junction the discontinuity in the resistivity at x_0 does not affect the charge distribution, but merely results in a low value of W, the effective collector width being only slightly greater than x_0. The transistor behaves as though it had a low saturation current and a low W at the onset of saturation. Now the high resistivity region is thin so the minority carriers penetrate through to the discontinuity at higher currents and remove the effect of the high resistivity region. The transistor now behaves as though it has a high saturation current and a value of W given by the full width of the collector region. The resulting AGC curve is thus a combination of two curves, as sketched in Fig. 8. By grading the resistivity in a more suitable manner a smooth curve of almost any profile should be obtainable.

Experiments with transistors of this sort have been successful, although the best results are experimentally difficult to reproduce.[7] Nevertheless it is easy to get a substantial smoothing of the AGC curve, as diffusion inevitably results in a gradation of resistivity near the collector–base junction.

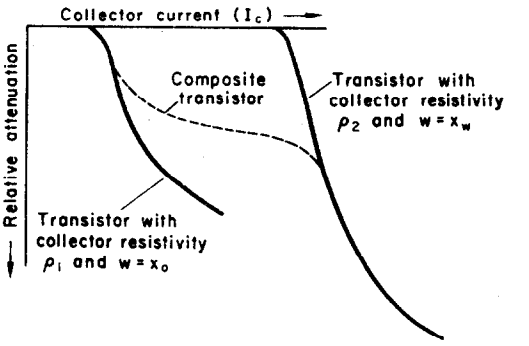

FIG. 8. AGC curve (dotted line) for a transistor with the resistivity profile shown in Fig. 7.

Rather similar results are obtained by reducing the emitter dimensions so that carrier heating occurs. As the transistor approaches saturation the resistivity of the collector region increases where the current density is highest which is adjacent to the base under the emitter. However the analogy is not exact as the incremental resistivity is now much greater than the chord value.

8. CONCLUSIONS

A model has been derived for the calculation of the circuit properties of saturated transistors in which the collector region is wide and much more lightly doped than the base. The general theory shows that the minority carriers are injected into the collector region and are kept close to the collector–base junction by the field produced by the current flowing through the lightly doped collector. As the transistor becomes more heavily saturated the width of the modulated region increases and the total charge stored increases, but it is noted that the effective transit time (dQ_c/dI_c) is not related to the width of the modulated region by the normal formula owing to the change in width with current. By considering the variation of the stored charge with applied voltages and currents a small signal equivalent circuit is deduced. This shows that saturation causes a conductance and capacitance $(C_{b'c'})$ to appear in parallel with the current generator, a slight modification in the current generator, a reduction in collector series resistance, and a voltage generator to appear in series with the collector

series resistance. As saturation proceeds the f_T of the device falls mainly because of increased feedback through $C_{b'c'}$ due to the presence of collector series resistance. The value of $C_{b'c'}$ and the parallel conductance can be quite large but the components do not appear directly with their true values in impedance measurements because the voltage generator partially opposes voltages applied between collector and base.

These qualitative results should apply to all transistors with a thick lightly doped collector, but the quantitative results that have been derived for the elements of the equivalent circuit are only valid for transistors that approach closely the idealized model that has been analyzed. Measurements of three such transistors show that the predicted relation between f_T and current is obeyed, and that parameters such as h_{0b} and y_{0b} can be found as functions of current to within a factor of about two or less.

The theory shows that to obtain a smooth gain control characteristic it is necessary to design the transistor so that it does not conform to the simple model analyzed here. This can be done by reducing one, or both, of the lateral dimensions of the emitter so that the effective collector width is small enough to produce heating of the electrons as the transistor approaches saturation. It can also be done by making the saturation as non-uniform as possible, by reducing the symmetry of the device geometry or doping, or alternatively by longitudinally varying the doping density in the collector region. Preliminary experiments along these lines have shown good results.

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APPENDIX

1. Relation between cylindrical, spherical and planar geometries of collector region

Assuming that the edge of the stored charge region is where the voltage is equal to that the junction at the point of saturation (when $I_n = I_{ns}$) it may be shown that the thickness (x') of the stored charge region is given by

$$\ln(1+x'/r_1) = \left(\frac{I_n}{I_{ns}} - 1\right)\ln(r_2/r_1) \quad \text{(A.1)}$$

(cylindrical case)

$$x'/r_1 = \frac{I_n}{I_{ns}}\left(\frac{1}{1+\left(\frac{I_n}{I_{ns}}-1\right)r_1/r_2}\right) - 1 \quad \text{(A.2)}$$

(spherical case)

where r_1 = radius of collector–base junction and
r_2 = radius of collector contact.

These results are valid for any angle subtended at the origin.

For the one-dimensional case

$$x/W = \left(1 - \frac{I_{ns}}{I_n}\right). \quad \text{(A.3)}$$

A comparison of equations (A.1) and (A.3) shows that the effective value of W to give $x' = x$ is

$$W \simeq r_1\left(\frac{I_n}{I_{ns}}\ln(r_2/r_1)\right), \text{ if } \left(\frac{I_n}{I_{ns}} - 1\right)\ln(r_2/r_1) \ll 1$$

$$\simeq r_1 \ln(r_2/r_1) \quad \text{(cylindrical case)}$$

From equations (A.2) and (A.3)

$$W = r_1\left(\frac{I_n}{I_{ns}}\right)\left[1 + \frac{I_n}{I_{ns}}\left(\frac{r_1}{r_2 - r_1}\right)\right]^{-1}$$

$$\simeq r_1, \text{ if } \left(\frac{I_n}{I_{ns}} - 1\right) \ll 1. \quad \text{(spherical case)}$$

2. Derivation of h_{0b} and y_{0b}

The parameters h_{0b} and y_{0b} are respectively the output admittance of the grounded base device with the input open circuited and short circuited. It can be seen from the equivalent circuit that when the input is open-circuited the current generator is not activated and the output admittance is just $1/(r_{b'c'} + j\omega C_{b'c'})$ or

$$h_{0b} = \frac{1 + j\omega\tau_p}{r_{b'c'}}.$$

When the input is short circuited the current generator is activated and it can be shown that the output admittance is then

$$\left[1+\frac{1}{\left(\frac{r_e}{r_{bb'}}+\frac{1}{h_{fe}}\right)}\right]\left[\frac{1}{r_{b'c'}}+j\omega C_{b'c'}\right]$$

or

$$y_{0b}=\left[1+\frac{1}{\left(\frac{r_e}{r_{bb'}}+\frac{1}{h_{fe}}\right)}\right]\left[\frac{1+j\omega\tau_p}{r_{b'c'}}\right]$$

The parameter h_{0b} was measured at the low frequency of 1592 Hz and at currents such that the transistor was well into saturation, hence the $\omega\tau_p$ term can be neglected and the measured value of h_{0b} should be given by [see equation (11)]

$$h_{0b}=\frac{1}{r_{b'c'}}=\frac{2qI_p}{kT}.$$

The parameter y_{0b} was measured at 3 MHz and in this case $\omega\tau_p$ cannot be neglected and to determine y_{0b} the full expression must be used.

In order to compare the measured and calculated values of h_{0b} and y_{0b} it was necessary to measure $r_{bb'}$, h_{fe}, τ_p and I_p. The quantities $r_{bb'}$ and h_{fe} were found by conventional Y parameter measurements while τ_p was found by measuring the switching time of the collector diode. The hole current was found from the relation

$$I_p=\int_{I_{ns}}^{I_n}\left[\frac{1}{h_{fe}}-\frac{1}{h_{fe}(I_{ns})}\right]\cdot dI_c.$$